1994 Seminar Reference Book

DATA TRANSMISSION
POWER DRIVE CIRCUITS
TEXAS INSTRUMENTS
DATA DESIGN
DATA CONVERSION
MIXED SIGNAL

94

LINEAR
MIXED-SIGNAL
DESIGN SEMINAR

Seminar Reference Book

TEXAS INSTRUMENTS

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94

LINEAR
MIXED-SIGNAL
DESIGN SEMINAR

TEXAS
INSTRUMENTS

1994
LINEAR MIXED-SIGNAL
DESIGN SEMINAR

Written by members of the Technical Staff, Linear Products Division
Texas Instruments.

Simon Ramsdale	**Derrick Robinson**
Liam Goudge	**Tim Ardley**
Elwyn Davies	**Dave Cox**
Bridget Barrett	**Ralf Asmussen**
Alun Webber	**Geoffrey Arnold**
David Cotton	**Julie Holland**
Mick Maytum	**Ben Mullet**
Charles Wray	

Contributions from John Walliker and Julian Daley of UCL.

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SECTION 2 POWER SUPPLY

SECTION 3 DATA CONVERSION

SECTION 4 DATA TRANSMISSION

SECTION 5 POWER DRIVE CIRCUITS

Introduction

TEXAS
INSTRUMENTS

Linear Design Seminar Structure

The 1994 Texas Instruments' Linear/Mixed Mode Design Seminar is intended to review a selection of T.I.'s latest Linear and Mixed-Mode products; and demonstrate how these can be used to address a range of problems and needs frequently experienced by design engineers.

Texas Instruments' Linear product mission, is to help make the connection between the real (analogue) world, and the digital world where most electronic processing is done. The structure of the seminar mirrors the main functional blocks of a simple, generic electronic system.

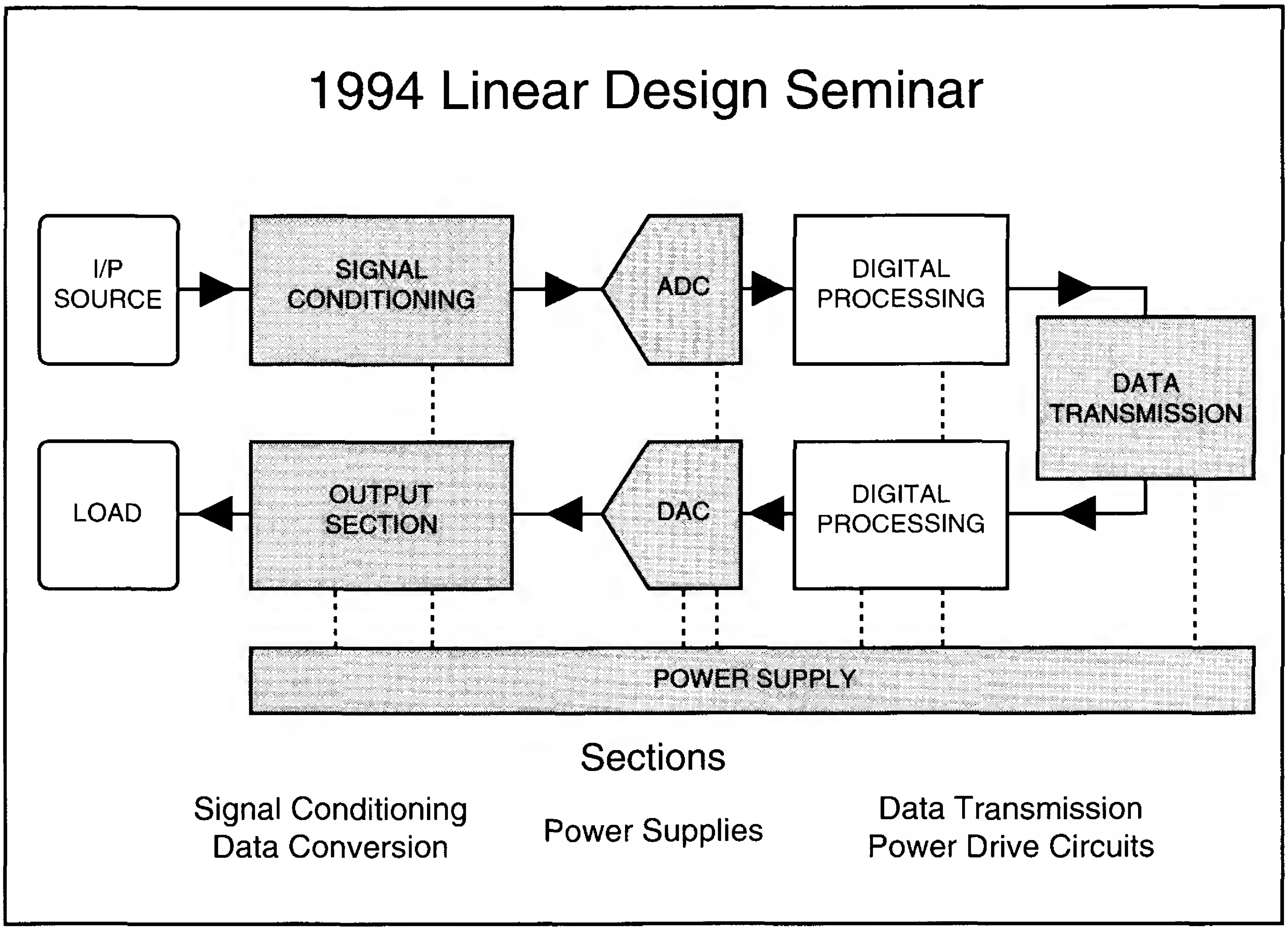
1994 Linear Design Seminar
I/P SOURCE
SIGNAL CONDITIONING
ADC
DIGITAL PROCESSING
DATA TRANSMISSION
LOAD
OUTPUT SECTION
DAC
DIGITAL PROCESSING
POWER SUPPLY
Sections
Signal Conditioning
Data Conversion
Power Supplies
Data Transmission
Power Drive Circuits

Figure i.1 - 1994 Linear Design Seminar

There are five sections in the seminar:

SIGNAL CONDITIONING
DATA CONVERSION
DATA TRANSMISSION
POWER SUPPLIES
POWER DRIVE CIRCUITS

In the **SIGNAL CONDITIONING** section, first the silicon technology options for op-amps are examined, together with their particular strengths and weaknesses. Recent introductions illustrate how specific application needs have been addressed. The use of Texas Instruments' new 3V range of signal conditioning devices, single-supply devices, and a range of plastic encapsulated op-amps suitable for high temperature use, will be discussed. Finally, there will be a review of how light sensing and imaging is simplified, by integration of precision analogue elements using standard mixed-mode technologies.

In the **DATA CONVERSION** section, this year's focus is on the use of serial ADCs (including 3V devices) with microcontrollers, and analogue interface devices for use with DSP. In the Digital-to-Analogue domain, the section will conclude with an short update on Video Palette devices.

In the **DATA TRANSMISSION** section, major single ended and differential transmission standards are discussed. Discussion will focus on the physical layer of the EIA/TIA-232-E, RS-422A and SCSI standards, and devices operating within these specifications. In addition the Meterbus standard, a low-power twisted-pair line intended for cost-effective utility metering will also be reviewed.

In the **POWER SUPPLY** section, a number of devices designed for use in power supply management will be described. Topics will include Low-Drop-Out Regulators (particularly for 3.3V operation), switching regulators, and supply voltage supervision.

In the **POWER DRIVE CIRCUIT** section, we shall examine different levels of integration of power switches, and examine the process by which the most appropriate device can be chosen to drive different low voltage loads stepper motors, DC motors, solenoids and incandescent lamps.

A common theme running through this seminar is that the most effective solution to a "linear" application need may not simply be a classical analogue component, or a custom device. Increasingly we find that integrated application-specific catalogue devices offer the best choice. These demand access to both precision analogue and high speed, high-density logic technologies. The broad range of Texas Instruments silicon technologies, and continued investment in innovation and world-wide volume production facilities position us particularly well to introduce such devices and support them.

Section 1
Signal Conditioning

Section Contributions by:

Simon Ramsdale
Derrick Robinson
Liam Goudge

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1 Introduction

This section of the 1994 Linear Design Seminar discusses the use of some of TI's latest signal conditioning products.

1.1 Signal conditioning

Signal conditioning is fundamentally modifying the input signal so that it has suitable characteristics for the next stage of the system to process it.

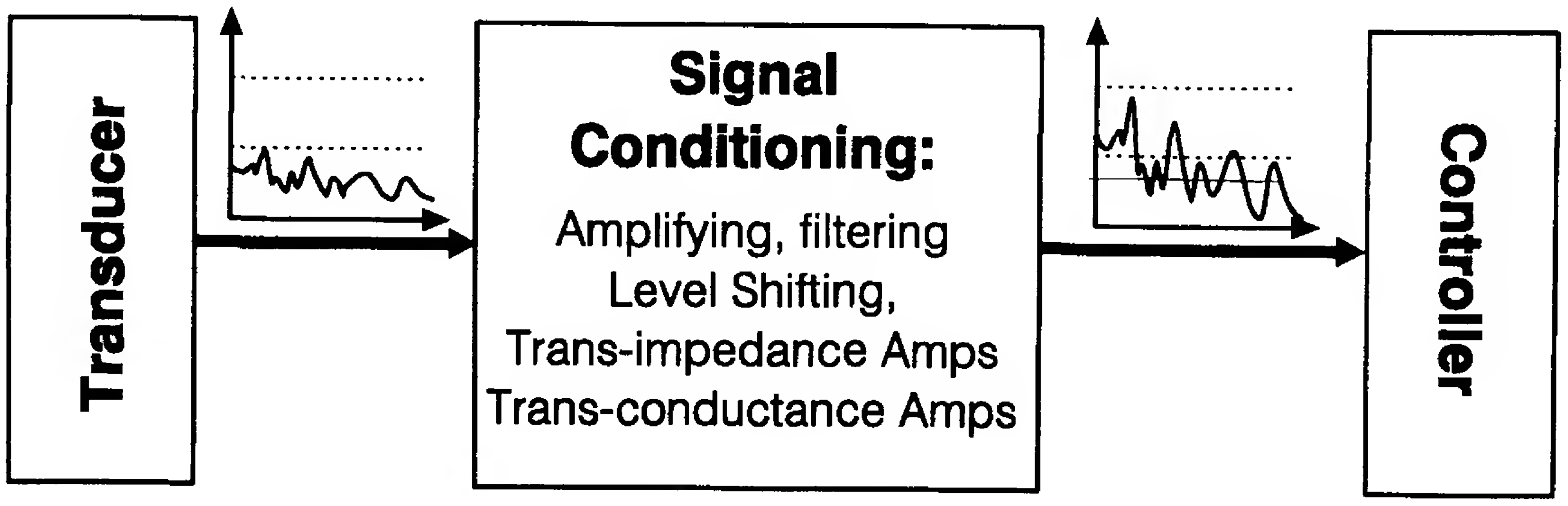
The output of a transducer/sensor will quite often have unwanted characteristics. For example:

too wide a spectrum of signals at its output
signal too small
output referred to the negative rail.

Signal conditioning will be used to change these characteristics and make the output closer to the required signal.

Signal Conditioning

The Dominant component used in signal conditioning systems is the op amp.


Transducer
Signal Conditioning:
Amplifying, filtering
Level Shifting,
Trans-impedance Amps
Trans-conductance Amps
Controller

Dual Supply Op Amps
Single Supply Op Amps
High Speed Op Amps
3-V Op Amps
High Temperature Op Amps

Figure 1.1 - Signal conditioning

The major component in Analogue Signal Conditioning is the op amp. Due to its uncommitted inputs it can be configured to provide a wide range of basic functions. These basic functions can then be used to amplify, filter and vary the common-mode signals present on the signal.

Operational amplifiers are fundamentally voltage amplifiers, and commonly use voltage feedback; they can however be configured to convert current to voltage and voltage to current.

For example, opto-sensors normally convert light power into current. Op amps configured as trans-impedance amplifiers are used to convert the current to voltage.

The type of sensor will determine the characteristics of the op amp. In opto-sensor applications and other high impedance transducer applications the op amp has to have a very large input impedance and therefore this reduces the range of devices. In these applications the choice of silicon device technology will greatly affect the performance of the system.

In other applications the available power supply will determine the choice of op amp. Texas Instruments manufacture op amps that have been designed for dual power supplies, single power supplies and some that can easily work from both. The latest class of op amps are those that are capable from working from a 3-V rail.

1.2 Technology overview

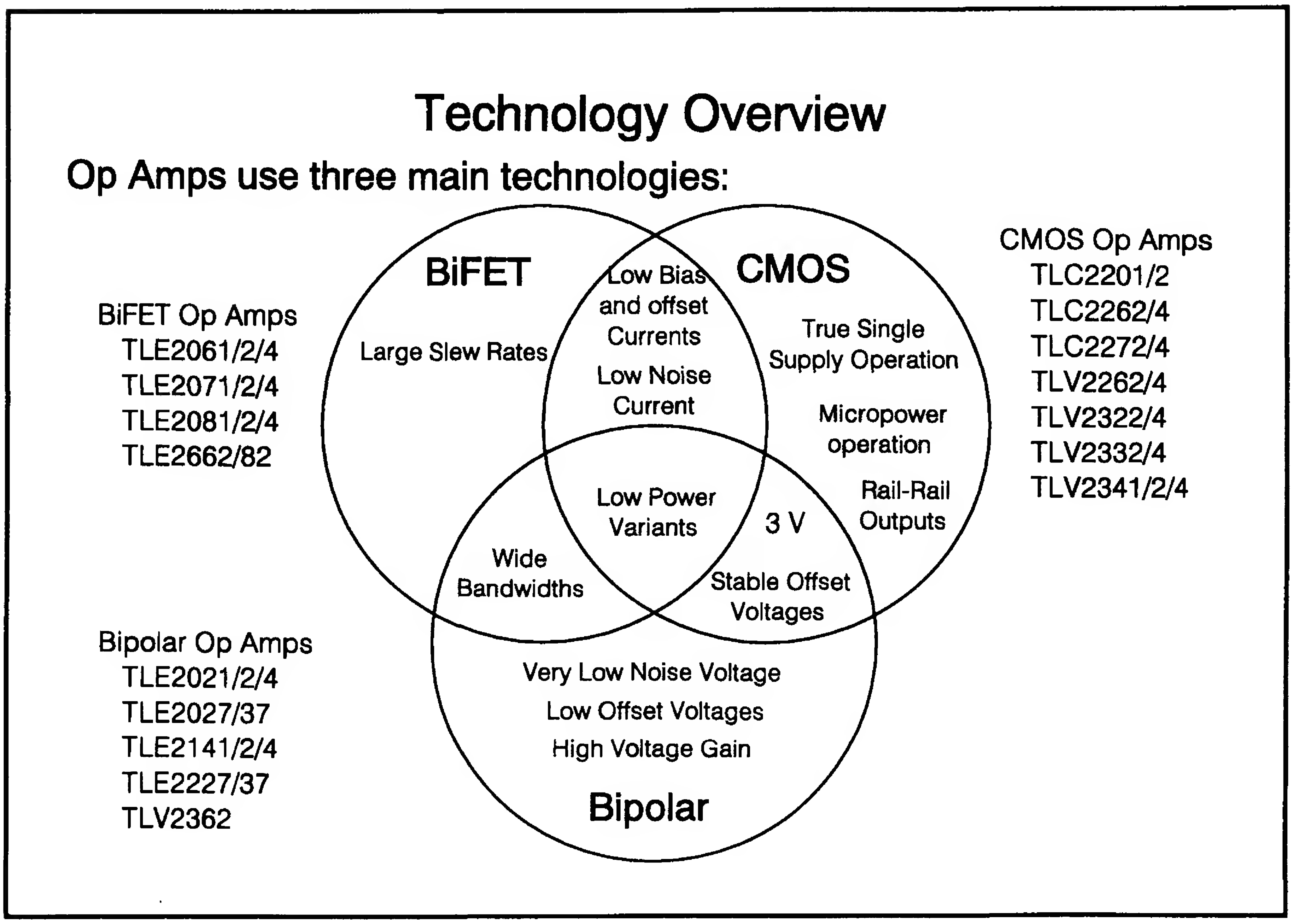

Technology Overview
Op Amps use three main technologies:
BiFET
CMOS
Bipolar
BiFET Op Amps
TLE2061/2/4
TLE2071/2/4
TLE2081/2/4
TLE2662/82
CMOS Op Amps
TLC2201/2
TLC2262/4
TLC2272/4
TLV2262/4
TLV2322/4
TLV2332/4
TLV2341/2/4
Bipolar Op Amps
TLE2021/2/4
TLE2027/37
TLE2141/2/4
TLE2227/37
TLV2362
Large Slew Rates
Low Bias and offset Currents
Low Noise Current
True Single Supply Operation
Micropower operation
Rail-Rail Outputs
Low Power Variants
3 V
Wide Bandwidths
Stable Offset Voltages
Very Low Noise Voltage
Low Offset Voltages
High Voltage Gain

Figure 1.2 - Technology Overview

As stated above, when interfacing to certain sensors the choice of technology will greatly affect the performance of the overall system.

Op amps are manufactured using three main technologies; Bipolar, BiFET and CMOS. In the future BiCMOS devices will become more popular due to the capability of combining the advantages of bipolar and CMOS devices.

1.2.1 Bipolar operational amplifiers

Advantages

Bipolar is still by far the most popular technology. This is due to its very fast NPN and PNP transistors (using a complementary NPN/PNP process like Excalibur) which allow manufacturers to make devices with bandwidths in excess of 10 MHz.

Bipolar input stage op amps have much better long term stability than BiFET and CMOS can offer. This is due to the majority of current flowing through the transistors is via the silicon bulk.

Bipolar op amps also offer lower noise voltages than BiFET or CMOS; this results directly from the noise voltage in a bipolar transistor coming from the emitter resistance. This resistance is far lower than that normally attained by either JFETs or MOSFETs, and so results in the bipolar input op amps having lower noise than devices made in other technologies.

Very good matching between input transistors enables bipolar op amps to have very low offset voltages and also very low drift with time and temperature.

Disadvantages

One disadvantage of bipolar op amps is their relatively large input bias currents, these can at times be as high 100s of nano-amperes. This results in them having large noise currents (100s of femto-amperes per root hertz). These large bias and noise currents exclude them from virtually all high impedance applications. Even though negative feedback will increase their input impedance (≈ 10s of mega-ohms) to giga-ohms and so making their closed-loop input impedance far higher than that of the sensor, their bias and noise currents will create input errors that swamp the input signal.

For high impedance sensor applications either BiFET or CMOS devices should be used.

1.2.2 BiFET operational amplifiers

Advantages

BiFET op amps combine P-type JFETs on the input stage with bipolar transistors. This gives BiFET op amps their very high input impedance (of the order of tera-ohms) and their very low input bias currents (10s of pico-amperes).

BiFET op amps will not normally have the very high gains that can be attained with bipolar op amps, but as a result of this they will normally have much better slew rates. The slew rate of a normal bipolar op amp is normally related to its unity-gain bandwidth by:

$$S.R. \quad = \quad 0.3 \times B_1 \ \ldots\ldots\ldots\ldots\ldots$$

$$\boxed{\begin{array}{l} A_{VD} = g_m \times X_{CC} = {}^{g_m}\!/_{2\pi f C} \\ B_1 = \dfrac{1}{2\pi}\dfrac{g_m}{C_C} \quad g_m = \dfrac{I_E}{2V_T} \\ S.R. = {}^{I_E}\!/_{C_C} \end{array}}$$

The JFETs have a lower trans-conductance which results in them having a much greater slew rate than what bipolar op amps will normally have. E.g. the NE5524 has a 10 MHz unity-gain bandwidth but its slew rate is 6 V/µs, while the TL071 has a unity-gain bandwidth of 3 MHz and a slew rate of 13 V/µs. So for a given bandwidth BiFET op amps have a much greater slew rate than their bipolar counterparts. This makes especially well suited to sample and hold, and precision peak detectors and rectifiers.

Disadvantages

The main disadvantage of BiFET op amps are their relatively poor offset voltages. Low offset voltage junction isolated BiFET op amps have offsets of the order of 500 µV, while their bipolar counterparts would have offsets of the order of 50 µV.

In addition to their poor offset voltages BiFETs also suffer from poor offset voltage stability. This is due in part to integrated circuit JFETs being 'lateral' devices. That is, the current flowing through the channel is lateral; making BiFETs susceptible to stress and strain effects on the die due to temperature changes and to thermal stress in assembly.

TI's 'Excalibur' process (enhanced bipolar) has reduced the high levels of offset voltage drift normally attributed to BiFET op amps.

BiFETs as well as having larger offset voltages than their bipolar counterparts also have higher noise voltages. This is due to JFETs having a lower trans-conductance than bipolar transistors. This leads to relatively large JFET channel resistance, which is the largest contributor to JFET's noise voltage.

1.2.3 CMOS operational amplifiers

Although originally considered to be too unstable for many linear functions, CMOS amplifiers are now well accepted as a real alternative to many bipolar, BiFET and even dielectrically isolated op amps.

Texas Instruments was the first company to offer a complete family of devices designed using a CMOS process, LinCMOS™, specifically developed for linear circuits. The first products were released in 1983, and LinCMOS™ and succeeding generations are being widely used today to realise a whole range of linear functions - from op amps to ADCs.

Advantages

All LinCMOS™ devices use PMOSFETs on their input. This provides them with lower noise and a common-mode input range down to the negative rail - making them ideal for single supply operation where quite often the input will be referred to the negative rail (ground).

The use of CMOS in op amps has enabled TI to build a range of micro-power op amps (10 µA/channel). LinCMOS has also allowed TI to produce a range of op amps capable of working from 1.4 V. The low voltage and micro-power operation makes these devices ideal for portable systems.

The low voltage operation of LinCMOS™ has allowed TI to be one of the first manufacturers to build a whole family of 3-V products that will operate over the whole industrial temperature range!

PMOS transistors on the input stage results in LinCMOS op amps having high input impedance and low offset and bias currents. Bias currents can be in the fA range, but difficulty in testing means that these levels of performance are rarely specified. A typical LinCMOS™ op amp has a bias current at 25°C of 100 fA. However, the bias currents will double for every 10 C increase in temperature. The very high input impedances and very low bias currents make them ideal for high impedance transducer interfaces. This is especially true when interfacing piezo-electric sensors to modern 5-V systems. BiFETs cannot interface to ground referred transducers and so are unsuitable for single 5-V systems.

ESD is something that is perceived to be a problem with CMOS, but not with devices designed using LinCMOS™. All devices produced using LinCMOS™ are designed to withstand 2 kV ESD - something many popular bipolar devices cannot claim. Protection circuits found in LinCMOS™ devices are discussed in the System Protection section.

Disadvantages

Although LinCMOS™ is ideal for low supply voltage applications, most CMOS parts will not operate with supply voltages greater than 16 V. This is a limitation in some wide supply, instrumentation applications.

The best CMOS devices can achieve offset voltages as low as 200 µV which is better than most BiFET parts but does not compete with the best bipolar designs. Typical CMOS op amps will have an offset voltage specification of 1 mV. The stability of CMOS devices is however, improved over BiFET designs.

Chopper stabilised op amps however are designed using CMOS technology and achieve the ultimate in dc precision. Maximum offsets as low as 1 µV are realisable.

Another disadvantage of some CMOS op amps is their relatively large noise voltages, typically around $30\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. However the latest Advanced LinCMOS™ op amps offer noise voltages around $9\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ which is lower than many bipolar op amps and about half of standard BiFET op amps!

1.3 Advanced packaging

Op amps have traditionally been supplied in two plastic packages; through hole dual-in-line and small outline surface mount.

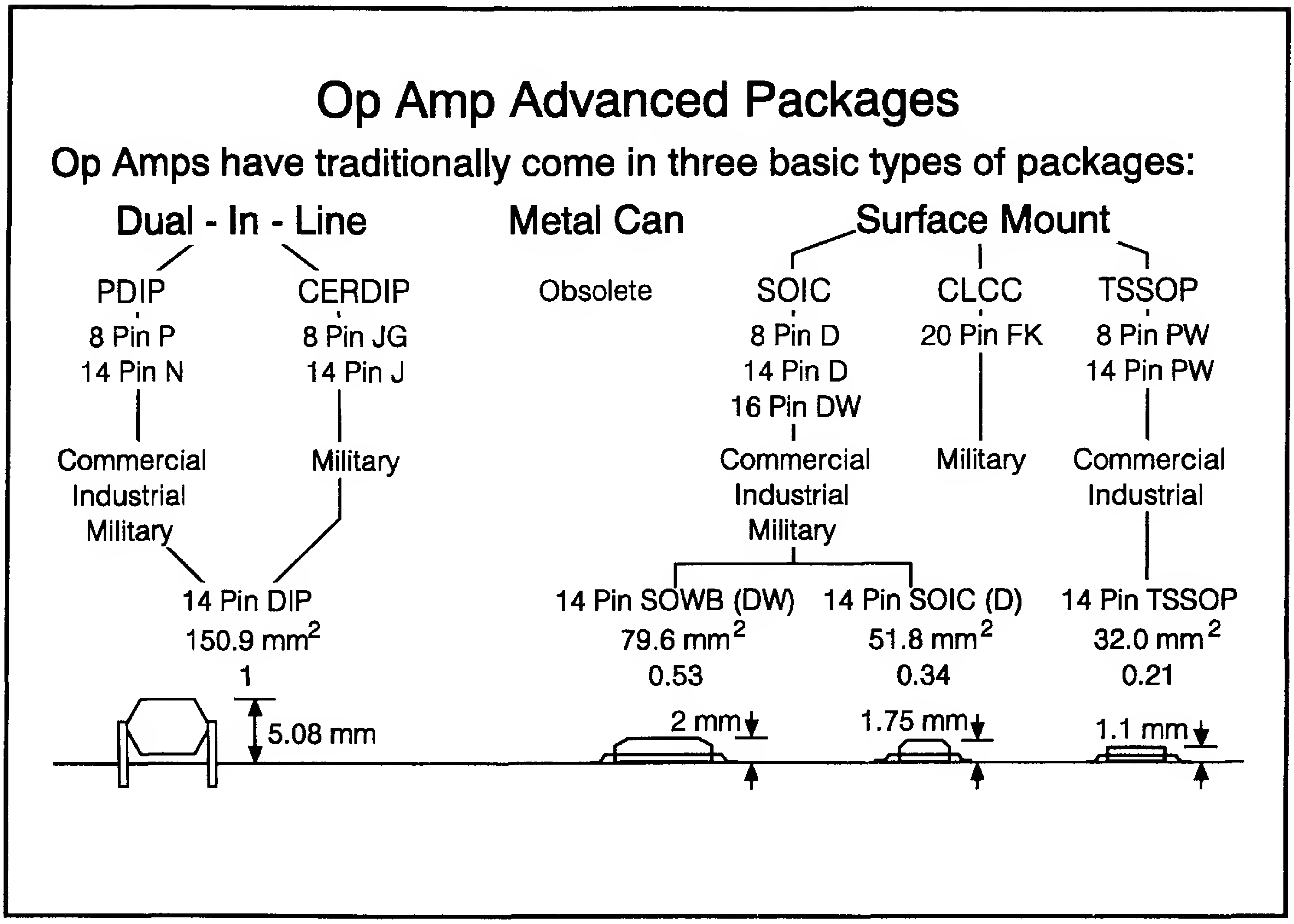
Ceramic and metal can packages have also been used where dc precision was needed and could not be achieved with plastic packages. These have been for a long time very costly alternatives to plastic packages which has restricted their use. So plastic packaged devices have become the norm in most applications; even some military applications are moving towards using plastic packaged devices.

DIP versus surface mount

With the increased levels of integration and increased levels of complexity the industry has been moving slowly to using more and more surface mounted packaging. The surface mount package is both smaller and can be attached to the board more efficiently than can some through hole devices. As a result of this, sales of surface mounted device have now clearly exceeded that of through hole devices.

In addition to the increases in levels of integration and complexity more and more systems are becoming portable. These include computing, telecoms, and instrumentation, and so the need to make the whole of the system fit into a smaller overall package has increased.

One way of solving this need is to integrate some basic functions onto more complicated ICs. However the need for op amps with different capabilities continues. So in order to provide op amps that will continue to meet the needs of the smaller, higher complexity applications TI has released a whole range of devices in the industries' smallest package - Thin Shrink Small Outline Package.



Op Amp Advanced Packages

Op Amps have traditionally come in three basic types of packages:

Dual - In - Line

PDIP
8 Pin P
14 Pin N
Commercial
Industrial
Military

CERDIP
8 Pin JG
14 Pin J
Military

14 Pin DIP
150.9 mm²
1

Metal Can

Obsolete

Surface Mount

SOIC
8 Pin D
14 Pin D
16 Pin DW
Commercial
Industrial
Military

CLCC
20 Pin FK
Military

TSSOP
8 Pin PW
14 Pin PW
Commercial
Industrial

14 Pin SOWB (DW)
79.6 mm²
0.53

14 Pin SOIC (D)
51.8 mm²
0.34

14 Pin TSSOP
32.0 mm²
0.21

Figure 1.3 - Op amp advanced packages

1.3.1 TSSOP

Figure 1.03 outlines the range of TI op amp packages. These range from the traditional through hole DIP and CerDIP, to the latest Surface Mount packages.

Considering a 14 pin package (quad op amp) a standard SOIC uses one third of the area of a DIP device, while a device in the new TSSOP occupies one fifth. This clearly shows the advantages of surface mount packages over DIP.

Another advantage of surface mount packages over DIP is the reduction in package height. A 14 pin DIP stands 5.08 mm clear from the PCB while TSSOP stands only 1.1 mm clear from the PCB. The dramatic reduction in board space and package height makes TSSOP essential for applications where board space is at a premium and/or where the PCB has to fit into as small possible box.

One example of where this is essential is in modern portable cellular phones. Size (width, length and thickness) and weight can be critical factors to the success of the phone.

2 Signal conditioning

2.1 Signal conditioning considerations

Any signal conditioning circuit will be required to meet some given system specifications. This is true even from the most simple circuits to the most complicated circuits.

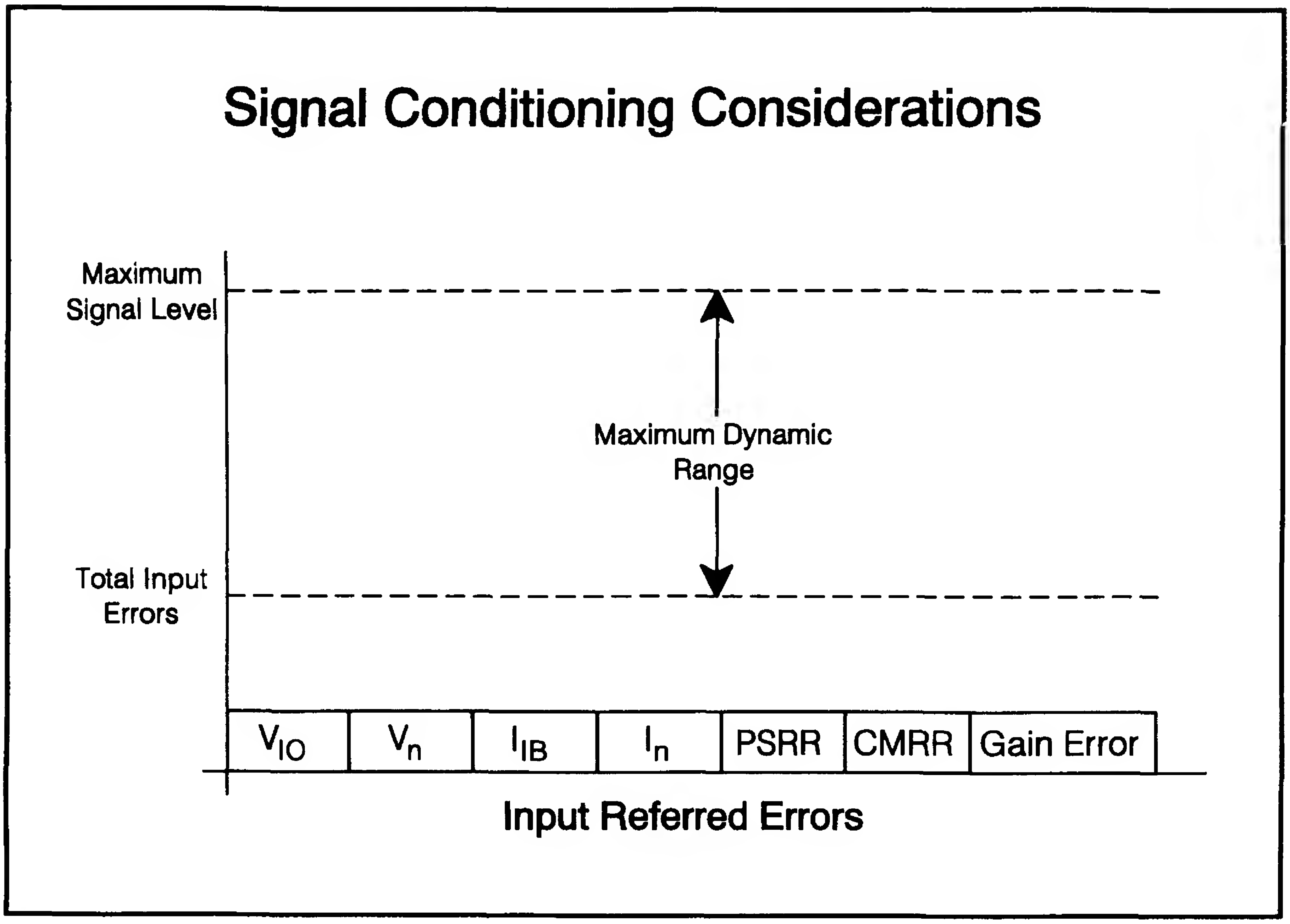
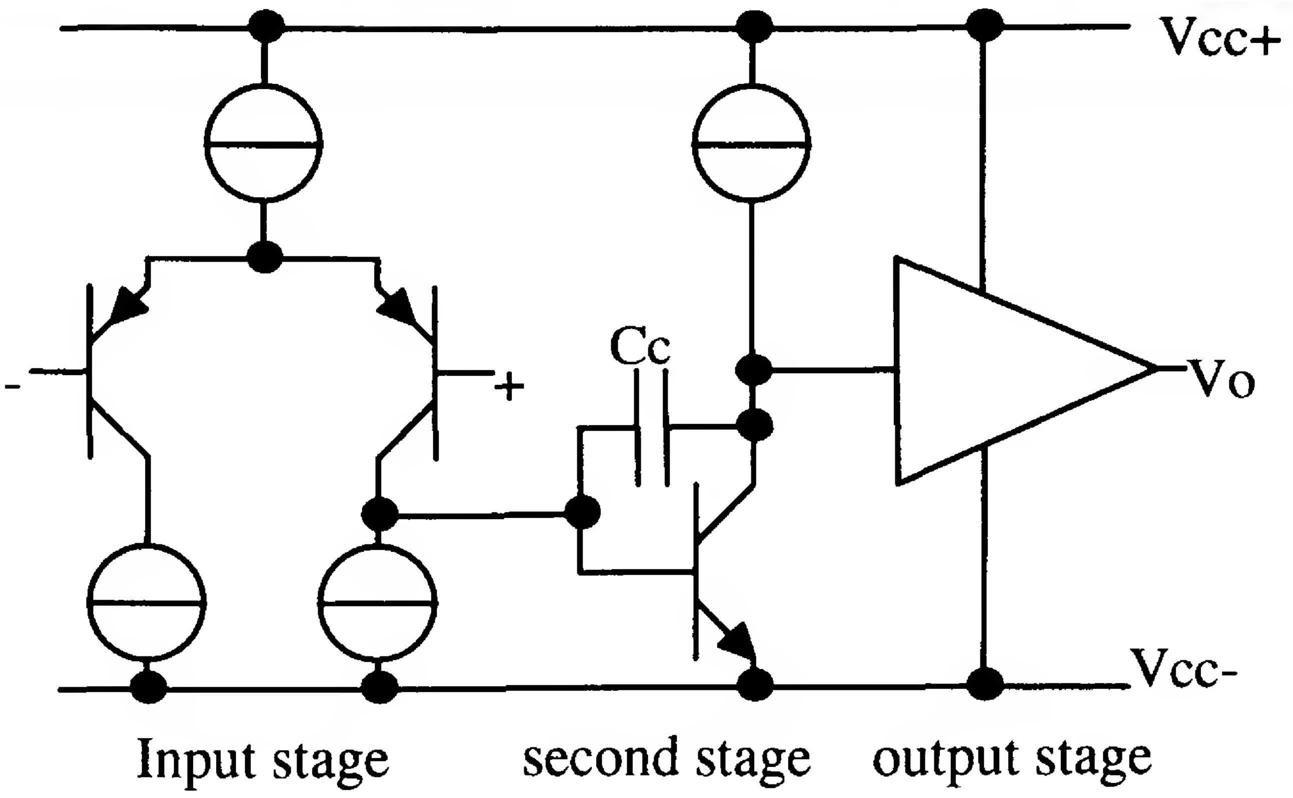

Signal Conditioning Considerations
Maximum Signal Level
Maximum Dynamic Range
Total Input Errors
V_{IO}
V_n
I_{IB}
I_n
PSRR
CMRR
Gain Error
Input Referred Errors

Figure 1.4 - Signal conditioning considerations

The dynamic range is one way of stating system specifications. It can also be used as a measure of system errors. In most applications the devices having the greatest effect on the performance of the whole system will be those in the input stage, since there is no way of recovering the errors that these devices introduce.

A basic internal configuration for an op amp is shown on the next page:



2.1.1 DC errors

The transistors in the input stage cannot be perfectly matched and so will have an offset between them. This offset voltage is affected by the supply voltage and the input voltage that is common to both of them. These effects are normally known as the Power Supply Rejection Ratio and the Common Mode Rejection Ratio, and can have large effects on the overall offset voltage of the device if too small. The input stage transistors also have current flowing through them and so draw input bias current. This will once again affect the accuracy of the device by adding another offset voltage equivalent to the product of the bias current and the equivalent source resistance as seen by the input. For a simple inverting amplifier configuration, this source resistance will be equivalent to the parallel combination of the source resistance and the feedback resistance.

Further input offset voltage errors arise from changes in junction temperature of the device as well as during the lifetime of the device.

Further errors will be introduced by the limited open loop gain. Most approximations in the open loop gain of an op amp assume it to be infinite. When designing systems requiring an accuracy better than 0.1%, the finite open loop gain can start to be a limiting factor in the performance of the op amp.

The dynamic range is one way of stating the system's performance. It can also be used as a measure of the system's errors. In most applications the devices having the greatest effect on the performance of the whole system will be those in the input stage, since there is not any way of recovering the errors that these devices introduce.

2.1.2 AC errors

The transistors in the input stage are not truly linear devices and will therefore introduce distortion as they are driven with sinusoid input signals. The output stage with finite output impedance and output drive capabilities will also introduce distortion.

The current flowing through the input stage transistors will generate noise due to their bias currents and their dynamic resistances, and will appear on the inputs as noise currents and noise voltages. Further input offset voltage errors will arise from the changes in junction temperature of the device and during the lifetime of the device, all these must be taken into account when trying to sum all of the input errors.

To ensure high frequency stability, the open loop gain of the op amp at these frequencies must be reduced to unity before the phase shift exceeds 180 C (for unity gain stability). The most common way of doing this is via dominant pole compensation. This is done by placing a capacitor, C_C, between the output of the input stage and the output of the second stage (see diagram above). This limits the gain-bandwidth product of the op amp, causing its open loop gain to decrease at a rate of 20 dB/decade. This limits the device's accuracy over frequency.

The limited gain-bandwidth product of the op amp also reduces its Power Supply Rejection Ratio and Common Mode Rejection Ratio over frequency. This increases the effect of higher frequency noise on the supplies, as well as the errors due to higher frequency common mode input signals.

The compensation capacitor also limits the rate at which the second stage's output voltage can change, introducing a slew rate limit on the device. This is another possible limit to ac accuracy. If the output signal's rate of change with time exceeds the device's slew rate capabilities then the output will be tied to the slew rate of the device and can cause the input to go into saturation generating further errors.

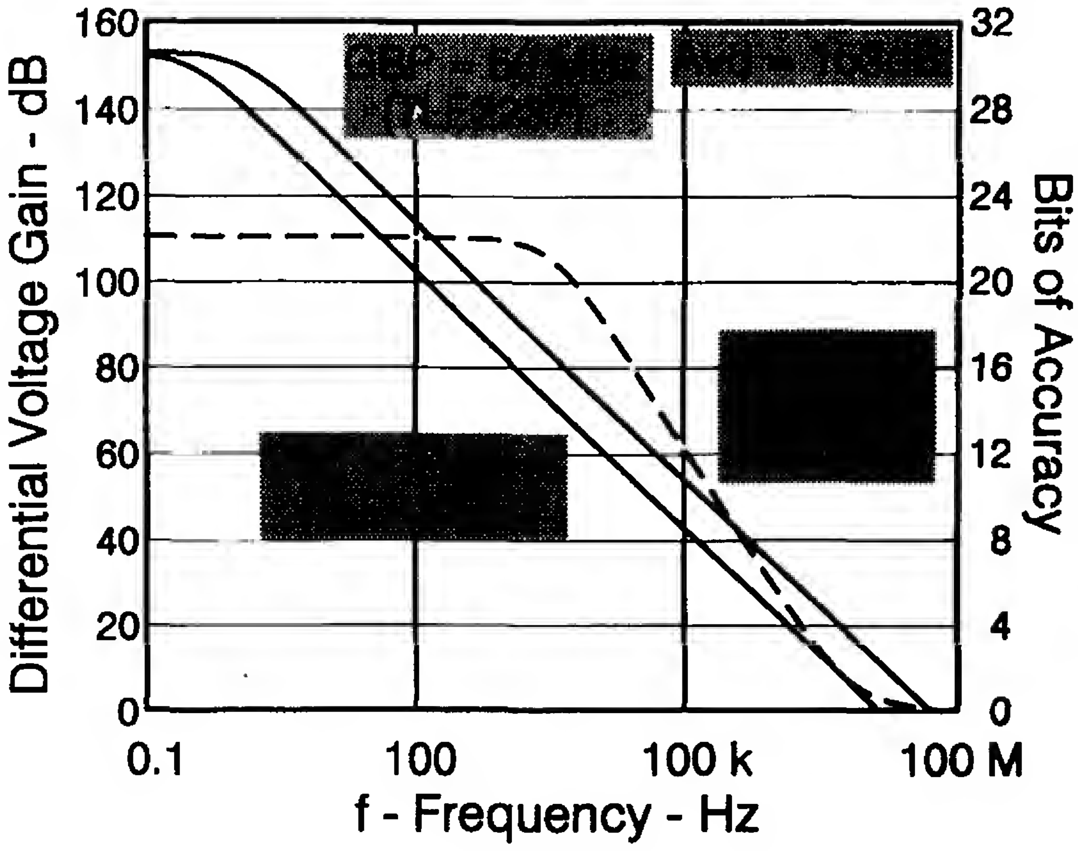
2.2 TLE2227 and TLE2237 - precision dual op amps

The TLE2227 and TLE2237 are among the most recent op amps to be developed and fabricated using the Excalibur technology. These devices have been optimised for precision and include a novel output stage that features a 'Saturation Recovery Circuit' which enables much improved small signal response and outstanding levels of distortion.

TLE2227 and TLE2237 - Precision Op Amps

Low Noise, High Speed with Precision in a Dual Op Amp

- Low Noise Voltage;
  3.3 nV/√Hz @ 10 Hz
  2.5 nV/√Hz @ 1 kHz
- Wide Bandwidth;
  TLE2227 .... 13 MHz
  TLE2237 .... 50 MHz
- Low Input Offset Voltage;
  100 μV (Typ)
  350 μV (Max)
- High Open Loop Gain
  45 Million



Applications

Instrumentation Amplifiers

Low noise filters

Figure 1.5 - TLE2227 and TLE2237 - precision op amps

2.2.1 DC performance

The parameters of most importance in a precision application are; Offset Voltage, Drift, Bias Currents and Open Loop Gain. The TLE2227, dual op amp, has an offset voltage of only 100 µV and a maximum offset voltage drift of 1 µV/°C and 1 µV/month. The TLE2237 (decompensated version of the TLE2227 for higher speed applications) has similar offset voltages and drifts to that of the TLE2227. Both devices have bias current cancellation circuitry to reduce bias currents to typically 15 nA enabling larger external resistors without impacting overall dc accuracy.

The curves in figure 1.05 shows the open loop gain of the devices. An outstanding parameter of both devices is their open loop gain, Avd; - at 153 dB, it is probably the highest in the world! This results in an improvement in the op amp's 'loop-gain' even when used in large closed loop gain applications, yielding an increase in overall performance.

Figure also shows the equivalent bits of accuracy of the TLE2237 with a gain of 10, and shows it of having a dc gain error accuracy of 22 bits.

2.2.2 AC performance

Both Devices have excellent unity gain bandwidths; 13 MHz for the TLE2227 and 50 MHz for the TLE2237, with Slew Rates for the TLE2227 of 2.5 V/µs and for the TLE2237 5 V/µs.

Low Noise - A large input stage, and clever design and layout techniques has given the device an extremely low noise voltage specification - 3.3 $nV/\sqrt{Hz}$ at 10 Hz, and 2.5 $nV/\sqrt{Hz}$ at 1 kHz. The low frequency noise and the low frequency 1/f corner give these devices a very small low frequency noise figure, only 50 nV for the 0.1 Hz to 10 Hz bandwidth. The low overall noise is an obvious benefit to precision measurement systems and audio applications.

Low Distortion - Linked to an increase in ac performance both devices feature a Saturation Recovery Circuit which improves the small signal response and enables the device to be used at much higher frequencies with increased output swings - see figure 2.3.09 A further advantage is the extremely low levels of distortion even when driving loads as low as 600 Ω, which has enabled the device to be used in low noise applications such as Audio systems.

Applications - The excellent ac performance and low noise makes the TLE2227 and TLE2237 ideally suited to Audio and Telecom applications. Their low offsets and excellent overall precision has enabled the parts to be used in Instrumentation, Measurement and Test equipment.

2.3 LVDT accelerometer

The wide bandwidths of the TLE2227 and TLE2237 make both devices well suited to high speed signal conditioning. In some applications their outstanding dc precision will also be required.

2.3.1 Accelerometer

Accelerometers, as their name implies, measure acceleration and can be made out of different materials. Accelerometer sensors use a seismic mass that is restrained by a spring and which is also damped. When acceleration is applied to the sensor case the mass will move relative to the case.

There are many types of accelerometers:-

Capacitive, piezoelectric, potentiometric, servo, and reluctive to name some. This application considers the reluctive type of accelerometer.

2.3.2 Linear Variable Differential Transformer (LVDT)

The LVDT is effectively a transformer with a movable core, which is the seismic mass, and primary and secondary windings. The primary will normally be driven by a sine wave. The secondary consists of two windings that are wound in opposition to each other. So when the core is in the middle of the transformer, the secondary windings cancel one another out producing zero output. As the core is moved the reluctance of the transformer changes, producing an output at the secondary.

The LVDT primarily measures displacement or change in displacement. Driving it with a sine wave is one way of overcoming many of the dc offset errors normally encountered when interfacing to resistive sensors. If displacement is required, then synchronous rectification of the output of the transducer will be required.

The frequency response of LVDTs are available in a wide range of sizes and excitation frequency range (50 Hz to 25 kHz). This application uses an excitation frequency of 25 kHz so that it is above the audible frequency range. The choice of LVDT will be determined by the magnitude of acceleration likely to be encountered, mass of system being tested. The LVDT has a linear response over a restricted displacement range. If the displacement becomes too large the output of the LVDT will saturate due to its reluctance decreasing. Other sources of error will be due to strain of the retaining springs. Whilst in the linear range it is possible to get LVDTs with accuracies of about 0.1%.

This application uses one TLE2227 and one TLE2237. One half of the TLE2227 is configured as a Wien Bridge Oscillator. Both of the TLE2237's op amps and the remaining TLE2227 op amp are configured as a three op amp instrumentation amplifier. this converts the differential output of the LVDT to a ground referenced single-ended output.

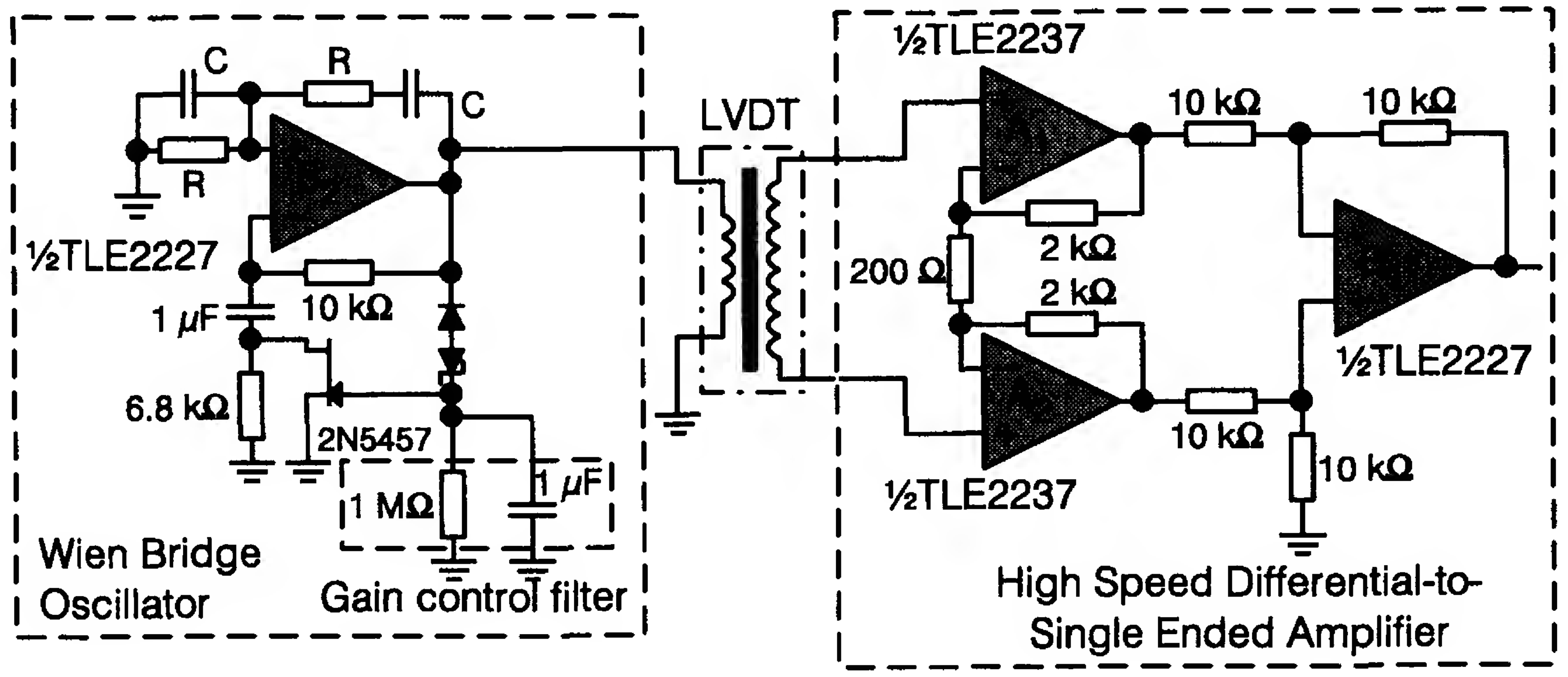
2.3.3 Wien bridge oscillator

The Wien bridge oscillator is well known for its low distortion. The serial and parallel combination of resistors and capacitors is used produce 180° phase shift about the op amp at its key frequency. However in order for oscillations to exist the closed-loop gain around the op amp needs to equal 3. If the gain is greater than 3 then the oscillations will grow until saturation of the op amp's output occurs. If the gain is less than 3 then the oscillations will never start, or will die out. In order to make sure that the oscillations do start, but do not saturate the op amp's output automatic variable gain needs to be used.

One established way of doing this is to use a lamp; this goes from the inverting input down to ground. At power up the resistance of the lamp is very low giving the op amp a very large closed-loop gain allowing the oscillations to build up. As the amplitude of the oscillation builds up, heat will be dissipated in the lamp causing its resistance to increase and so reduce the op amp's closed-loop gain.

LVDT Accelerometer

Wideband and low input error accelerometer


C
R
C
R
C
½TLE2227
1 µF
10 kΩ
6.8 kΩ
2N5457
1 MΩ
1 µF
Wien Bridge Oscillator
Gain control filter
LVDT
½TLE2237
10 kΩ
10 kΩ
200 Ω
2 kΩ
2 kΩ
½TLE2227
10 kΩ
10 kΩ
½TLE2237
High Speed Differential-to-Single Ended Amplifier

$$f = \frac{1}{2\pi RC} = 25\ \text{kHz}$$

C = 1.5 nF
R = 4.22 kΩ

Figure 1.6 - LVDT Accelerometer

Another way of doing this is to use a VDR to control the gain. the circuit shown in figure 1.06 uses a NFET as a VDR. At power-up the NFET will be hard on giving the op amp a large closed-loop gain. As the amplitude of the oscillation builds up, the JFET will be gradually turned off until the gain equals 3. The gate voltage of the JFET needs to be filtered and slowed down so that its channel resistance is not affected by each individual cycle. The schematic shown uses a time constant of 1 s.

2.3.4 Instrumentation amplifier

The first stage of the instrumentation amplifier is used to introduce a gain of 10. This allows the second stage to have unity differential gain, thus reducing the matching requirements of the resistors about the second stage. The very large common-mode rejection ratio of the TLE2227 means that most of the common-mode errors introduced by the second stage will be due to mismatches in the resistors.

The TLE2237 is used in the first stage of the instrumentation amplifier. Decompensation of the TLE2237 (minimum closed-loop gain = 5) gives it with a gain bandwidth product of the order of 5 times greater than the TLE2227. This makes it ideal for applications where gains greater than 5 over a wider bandwidth are required. Even with a closed-loop gain of 10, the TLE2237 will still have a excess loop-gain of 2000 at 25 kHz!. Its Common-mode rejection ratio will still exceed 60 dB.

2.4 TLE2071/2/4 and TLE2081/2/4 high speed BiFETs

The latest members of Texas Instruments' vast family of BiFETs are the TLE207X and TLE208X. These are high speed, low noise BiFETs. In common with all the most recent releases of Texas Instruments' BiFETs they are constructed using the Excalibur technology.

Texas Instruments was one of the first semiconductor manufacturers to supply BiFETs . One of Texas Instruments' great strengths in their Linear product range is its family of BiFETs. In the mid-eighties, this was reinforced by the introduction of the TL030s and TL050s. The introduction of TI's 'Excalibur' process has enabled further progress in BiFETs. TI has now released 3 families of Excalibur BiFETs: low power TLE2060s, guaranteed low noise TLE2070s and high speed TLE2080s.

TLE2071/2/4 and TLE2081/2/4 High Speed BiFETs

High Speed, Low Noise and Distortion Families

- High Gain-Bandwidth Product
  10 MHz
- High Unity-Gain Slew Rate
  40 V/µs
- Low Noise Voltage
  11.6 nV/√Hz
  17 nV/√Hz (Max.)   TLE207X
- Low Noise Current
  2.8 fA/√Hz

Applications
  High Performance Audio
  Filters
  Sample and Hold

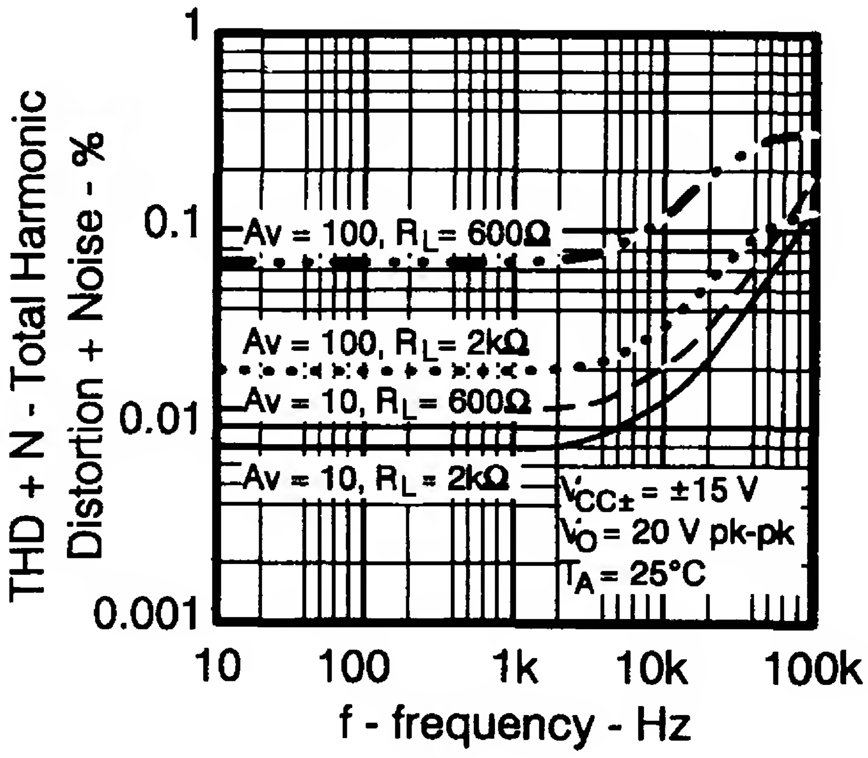


Figure 1.7 - TLE2071/2/4 and TLE2081/2/4 high speed BiFETs

The TLE2070s and TLE2080s have been developed to meet the higher requirements of today's new applications. This covers audio applications as well as high speed control applications. The strength of all BiFETs is their very high slew rate. Both families have taken this a stage further with 10 MHz unity gain bandwidths and large 40 V/µs slew rates. The specifications are improved by their low noise voltages, typically 11.6 nV/√Hz. The TLE2070s have a guaranteed noise voltage of 17 nV/√Hz making it ideal for high speed low noise transducer interfaces.

The very low Total Harmonic Distortion (THD) figures make it ideal for audio applications, replacing the TL070s which have become standard members in many high performance audio systems. The low noise and high speed make the TLE2070s well suited to industrial control applications. The high slew rate is equally well matched by its very fast settling time. The TLE2072 takes just 400 ns to settle within 10 mV of its final state value for a 10 V, and just 1.5 µs to within 1 mV.

2.5 TLE2072 audio preamplifier

The TL072 has, in many audio systems become the mainstay op amp. This is due to its good unity-gain bandwidth and slew rate. However in today's modern audio systems, which are requiring higher dynamic ranges, the noise voltage of the TL072 is becoming too high.

The TLE2072 provides a natural replacement for the TL072. The TLE2072 offers a 3-fold increase in bandwidth and slew rate over the TL072. This enables the TLE2072 to be used at higher gains over wider frequencies than the TL072.

The TLE2072 also offers a maximum noise voltage of only 17 $nV/\sqrt{Hz}$, which is equivalent to the TL072's typical noise voltage. This is another way in which the TLE2072 improves the performance of the system. Figure 1.07 showed the distortion plus noise performance of the TLE2072 when driving typical heavy audio loads.

2.5.1 Audio pre-amplifier

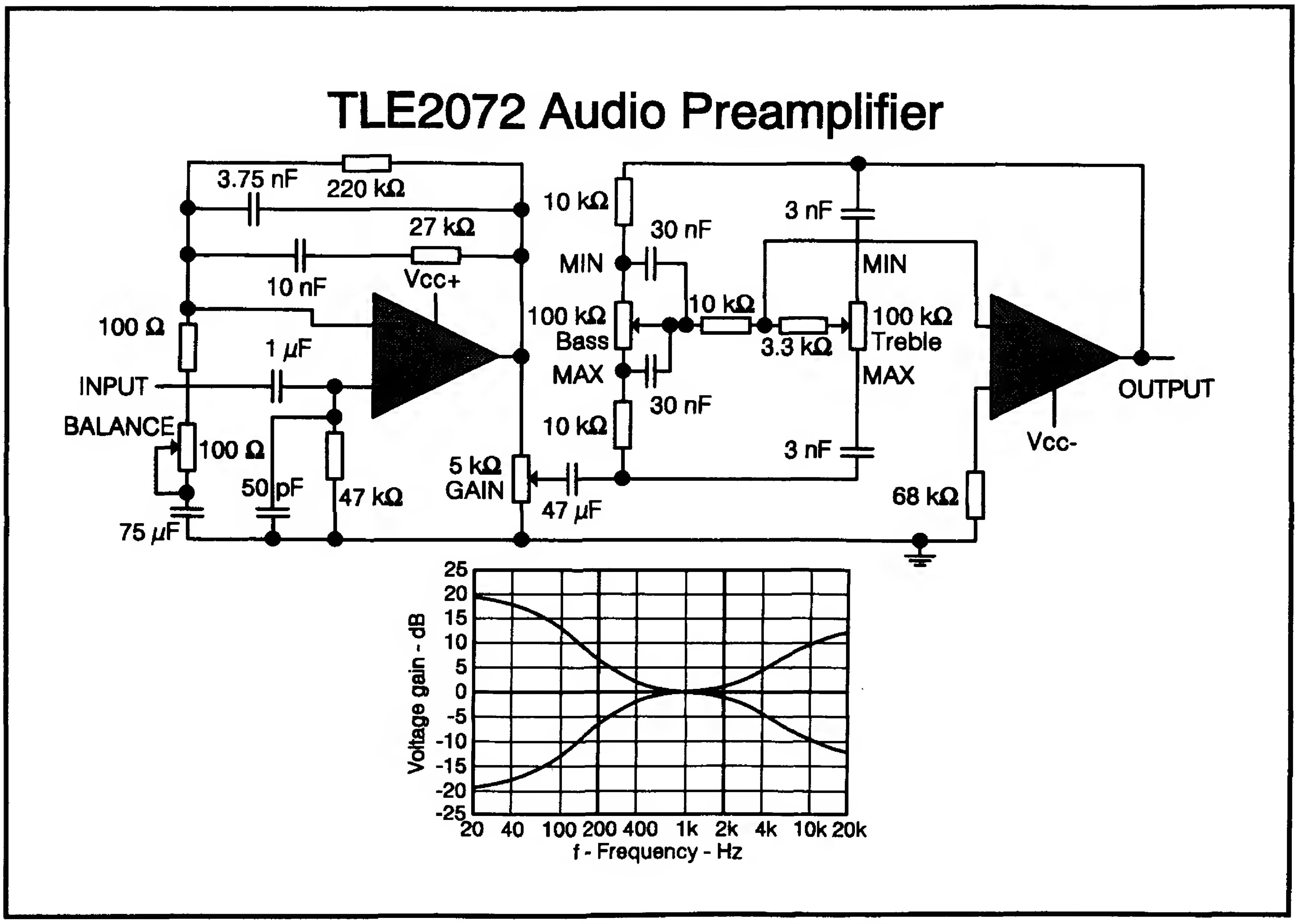

TLE2072 Audio Preamplifier
3.75 nF
220 kΩ
27 kΩ
10 nF
Vcc+
100 Ω
1 µF
INPUT
BALANCE
100 Ω
50 pF
47 kΩ
75 µF
5 kΩ
GAIN
47 µF
10 kΩ
MIN
100 kΩ
Bass
MAX
10 kΩ
30 nF
30 nF
10 kΩ
3.3 kΩ
3 nF
3 nF
MIN
100 kΩ
Treble
MAX
OUTPUT
Vcc-
68 kΩ
Voltage gain - dB
25
20
15
10
5
0
-5
-10
-15
-20
-25
20 40 100 200 400 1k 2k 4k 10k 20k
f - Frequency - Hz

Figure 1.8 - TLE2072 Audio Preamplifier

One typical use of BiFETs in audio systems is in the pre-amplifier. The pre-amplifier is used to provide further amplification of the input signal as well as providing some modification of its harmonics. the application showed in figure 1.08 is used to modify the bass (low frequency) and treble (high frequency) components. It has been designed to provide up to ±20 dB of gain on the bass and treble signals. The curve shown in figure 1.08 shows the extremes in the bass and treble gain.

The pre-amplifier also incorporates some gain control, but the majority of the gain control will be set elsewhere in the system.

2.6 High performance bandpass filter

When designing bandpass filters it is quite often easier to convert them into a low pass equivalent. This then makes it possible to make a lowpass prototype which can then be converted into a prototype bandpass filter with unity centre frequency. This can then be converted into the required filter.

The filter here uses a TLE2082 op amp, and makes use of its good unity gain bandwidth and high stability. The filter is to be a Chebyshev filter and have the following specifications:-

Centre frequency f_0 = 1 kHz
Pass Bandwidth BW = 300 Hz
Stop Bandwidth SBW = 3000 Hz
Pass attenuation α_{MAX} = 1.5 dB
Stop attenuation α_{MIN} = 40 dB

2.6.1 Chebyshev Filter

Chebyshev filters have an equal ripple passband frequency response, and a monotonic stopband roll-off. The location of its poles are based around an ellipse, giving it its equal ripple passband, whereas the Butterworth filter has its poles based around a circle. However the location of their poles for similar order filters will have the angle from the y-axis in the complex plane.

The maximum attenuation in the passband follows Lissajou's patterns, giving it the equal ripple. The transfer function of the Chebyshev filter follows this equation:-

$$|T_n(j\omega)| = \frac{1}{1+\varepsilon^2 C_n^2(\omega)}$$

Where $C_n(\omega) = \cos(n \cos^{-1} \omega) \qquad |\omega| \leq 1$

And n is the order of the filter and ε determines the depth of ripple. For values of ω greater than 1 the cos functions become imaginary or follow cosh functions.

2.6.2 Determining Prototype

The order of filter required can be determined from nomographs or from the following equation:-

$$n = \frac{\cosh^{-1}\left[\left(10^{\alpha_{\min}/10}-1\right)/\left(10^{\alpha_{\max}/10}-1\right)\right]^{1/2}}{\cosh^{-1}(SBW/BW)}$$

$$= \frac{\cosh^{-1}\left[\left(10^{40/10}-1\right)/\left(10^{1.5/10}-1\right)\right]^{1/2}}{\cosh^{-1}(3000/300)} = 1.92$$

This should be rounded up to the nearest whole number, to give 2.

The poles of the prototype filter can either found from filter tables, or found using the following equations:-

The ripple in the passband is 1.5 dB, resulting in an ε of:-

$$\varepsilon = \left[10^{\alpha_{max}/10} - 1\right]^{1/2} = 0.642$$

The location of the prototype filter's poles will be at:-

real part $-\Sigma_k = \sin\theta_k \sinh a$ .... and

imaginary part $\pm\Omega_k = \cos\theta_k \cosh a$

Where $a = \frac{1}{n}\sinh^{-1}\left(\frac{1}{\varepsilon}\right)$ and $\theta_k = k\frac{180°}{n} \pm \frac{90°}{n}$ ....for k = 0 to n-1

This sets a values for a of 0.613 and θ_k of 45°, and 135° which is greater than 90° and is ignored.

This gives the prototype low pass filter the following poles:- -0.46 ± 0.844

2.6.3 Bandpass Prototype

The prototype low pass filter's poles form a complex conjugate pair, and using a complex algorithm, they will get converted into two further complex conjugate poles.

Let $q_c = \frac{f_0}{BW}$ ....Where BW is the pass bandwidth

$C = \Sigma^2 + \Omega^2$ .... Σ and Ω are the real and imaginary .... parts of the prototype low pass poles

$$D = \frac{2\Sigma}{q_c}$$

$$E = 4 + \frac{C}{q_c^2}$$

$$G = \sqrt{E^2 - 4D^2}$$

$Q = \frac{1}{D}\sqrt{\frac{1}{2}(E+G)}$ ....Q is the quality factor of the new filters

$$K = \frac{\Sigma Q}{q_c}$$

$$W = K + \sqrt{K^2 - 1}$$

$f_{02} = Wf_0$.................................Upper centre frequency of new filter

$f_{01} = f_0/W$............................ Lower centre frequency of new filter

Inserting the values for Σ, Ω, f_0 and BW yields:-

$q_c = 3.33$ $C = 0.925$

$D = 0.277$ $E = 4.08$

$G = 4.05$ **Q = 7.29**

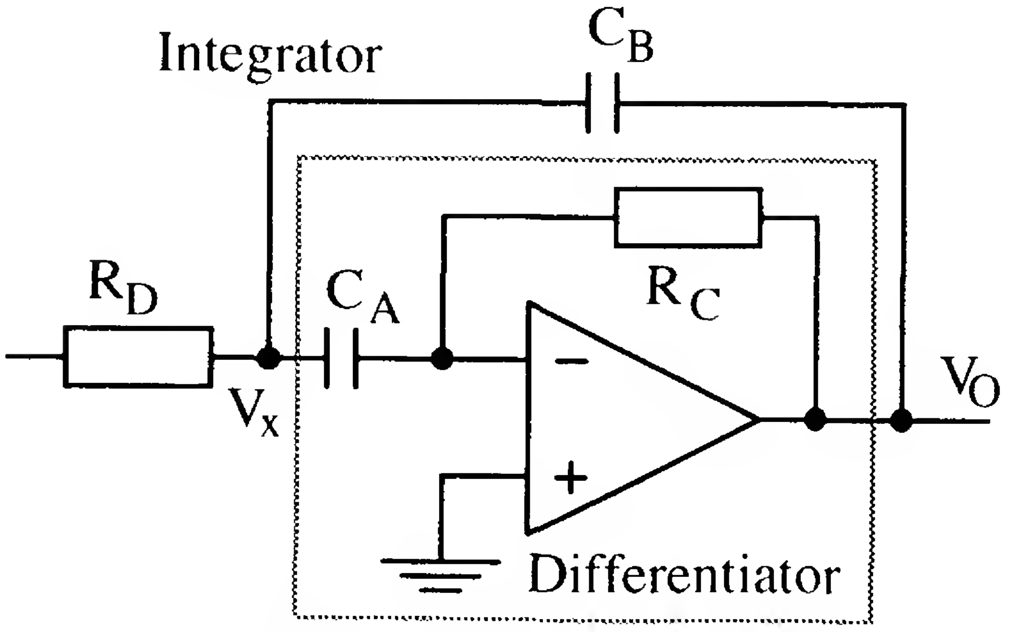
$K = 1.01$ $W = 1.13$

$f_{02} = 1135 \qquad f_{01} = 881$

So the two second order Chebyshev bandpass filters will have their centre frequencies at 1135 Hz and 881 Hz, with a quality factor, Q, of 7.29.

2.6.4 Delyiannis-Friend Bandpass Filter

One accepted way of producing bandpass filters is the Delyiannis-Friend circuit. This circuit can be considered to consist of an inner differentiator and an outer integrator.



The relationship between V_x and V_O is:-

$$V_O = -R_C C_B s V_x$$

Using Thevenin's Law and superposition the equation relating V_{IN} to V_O becomes:-

$$\frac{V_O}{V_{IN}} = \frac{(-1/R_D C)s}{s^2 + (2/R_C C)s + 1/R_D R_C C^2} \text{ ....Where } C_A = C_B = C$$

This means that

$$f_0 = \frac{1}{2\pi C\sqrt{R_D R_C}} \qquad Q = \frac{1}{2}\sqrt{\frac{R_C}{R_D}}$$

$$BW = \frac{2}{R_C C}$$

This provides the filter with orthogonal tuning; by altering both capacitors together the centre frequency can varied with altering the Q of the filter. So that resistors R_C and R_D can be altered to set the Q or bandwidth of the filter, and then the capacitors can be adjusted to set the centre frequency.

Analysing the actual component values and setting R_D and w_0 to 1 yields:-

$$R_C = 4Q^2 \qquad C = 1/2Q$$

This shows that the gain at the centre frequency is actually equal to $2Q^2$. To account for this and to give the circuit unity gain at its centre frequency a potential divider must be placed on its input. In order to maintain the same relationships between the capacitors and resistors, the potential dividing resistors must have the following relationship:-

$$R_A = Q^2/5 \qquad R_B = \frac{Q^2}{Q^2 - 5}$$

By using orthogonal tuning , the values of the capacitors can be defined, and from these the values for R_A, R_B, and R_C and be set.

High Performance Bandpass Filter

Fourth Order Cascaded Delyiannis-Friend Chebyshev Filter

f_O	1 kHz	f_1	881 Hz
BW	300 Hz	f_2	1135 Hz
SBW	3 kHz	Q	7.287
α_{MIN}	40 dB		
α_{MAX}	1.5 dB		

Prototype Filter	
$R_A = Q^2/5$	$C_A = 1/2Q$
$R_B = \frac{Q^2}{Q^2-5}$	$C_B = 1/2Q$
$R_C = 4Q^2$	

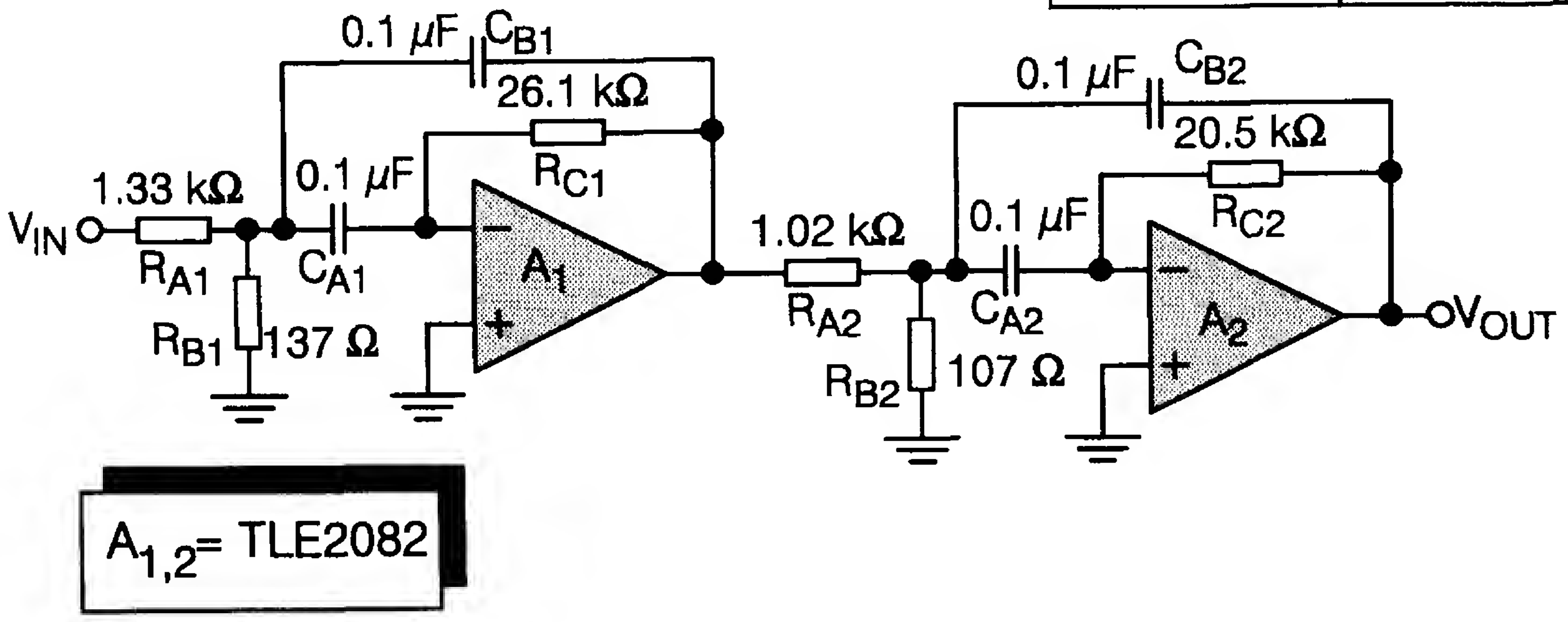


Figure 1.9 - High performance bandpass filter

The relationship between the prototype capacitor values and the final filter's values is:-

$$C_{NEW} = \frac{1}{2\pi \times f_0 \times k_M} C_{PROT} \qquad R_{NEW} = k_M x R_{PROT}$$

Setting C_{NEW} to 0.1 µF, defines k_M and so sets R_{NEW}. Using these factors set the resistor values shown in figure 2.3.17.

One important thing to bear in mind is the relatively large closed loop gain used about the op amp. If the device is provide low distortion and gain and signal accuracy over the frequency range chosen then the device must have a large bandwidth. The effective gain around the op amp is close to 100, and so if the op amp is maintain low distortion at its centre frequency then its gain-bandwidth product needs to be of the order of 10 MHz. The TLE2082 has a bandwidth of 10 MHz and an equally high slew rate to match its bandwidth, allowing it to perform to its full without it being the limiting factor in the circuit.

2.7 TLE2301 power op amp with 3-state output

Most op amps have an output current capability of the order of 5 - 20 mA. In most applications the smallest resistance that the op amp will have to drive will be around 1 kΩ, so driving this load from a ±15-V supply only requires 13 mA (most op amps will lose around 2 V from either rail).

The 1 kΩ load will normally only be encountered while providing the conditioning of the input signals. They will seldom be asked to drive the system's load. Op amps are used in abundance to provide filtering and amplification in audio systems, but they cannot be used to drive the speakers (impedance of 4 to 8 Ω). Power amps are normally used to drive these loads.

2.7.1 Power Amps

Power amps are normally specially designed amplifiers, and cannot be easily configured to provide the wide variety of functions that normal op amps are capable of doing. Their high output drive capability and their configuration differentiate them from normal op amps.

Power amps are frequently used in the output stage of audio systems (a lot of power amps have been designed solely for this purpose). Here their high output drive capability and low distortion are essential. There are, however, a number of applications that also require a high output drive capability; analogue motor drivers and mains line communications.

2.7.2 TLE2301 power op amp

TLE2301 Power Op Amp With 3-State Output

1 A Output drive and 3-state output provides easy interface to heavy loads

- High Output drive capability
  > 1 A
- 3-State output
  Zo(on) = 1 Ω
  Zo(off) > 100 kΩ
- High Speed
  8 MHz

Applications

Mains line driver

Audio medium power amp

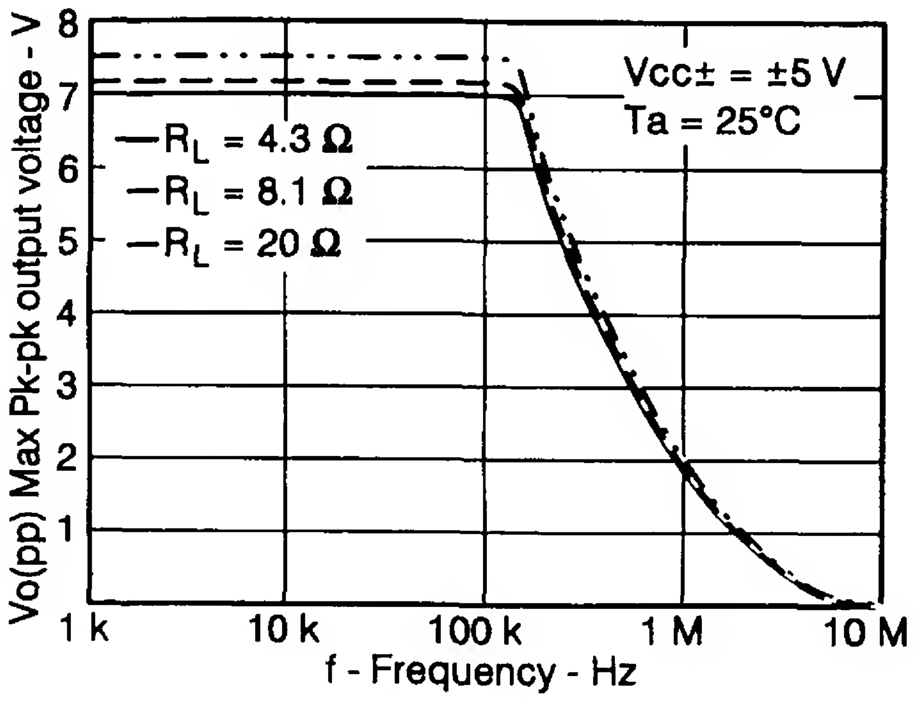


Figure 1.10 - TLE2301 power op amp with 3-state output

The TLE2301 was designed for the latter application, however it can be used in all three and more applications. In order to be used in these applications the power op amp must three basic characteristics:

High output drive capability

In order not to cause clipping in these applications the power amp must have a certain level of current drive capability. The level of output drive capability will determine what class of applications it can be used in. The TLE2301 was designed to have a minimum short circuit output current of 1 A. This allows the TLE2301 to drive 4 Ω loads, depending on power dissipation and ambient temperature range and places it in the medium power audio range.

Wide bandwidth

The audio bandwidth extends up to around 20 kHz, while the mains line communications bandwidth extends to 150 kHz. So if the op amp is reliably amplify the input signals without adding too much distortion it must have sufficient loop gain at the higher frequencies. The TLE2301 has a unity-gain bandwidth of 8 MHz, which enables it to be used as a real op amp even at 150 kHz.

Low distortion

The op amp's bandwidth limits its distortion at high frequencies, however it must have low inherent distortion at the base frequencies to be used in audio or mains line communication systems. In audio low distortion is essential to maintain the high fidelity of the signal, for mains line communication systems low distortion is essential to reduce out of band interference. The European specification, EN50065-1, places strict limitations on these out of band signals.

Another feature of the TLE2301 which is essential for mains line communication systems is its **3-state** output capability.

3-state output

Most op amps' output stages have been designed so that they can sink and source current. The most common way of doing this is to use a class AB output configuration. This helps to limit the distortion introduced by the op amp when actually going from sinking to sourcing current.

However when driving the mains line and using half duplex method of communication it is essential for the op amp to be disconnected form the line, otherwise severe attenuation and loading of the op amp could occur when two drivers try to drive the line simultaneously.

the TLE2301 has a 3-state feature which places the op amp in a power down mode as well as putting its output in a high impedance state. The output impedance of the TLE2301 is normally around 1 Ω, but when it is placed into the 3-state mode its output impedance increases to 100 kΩ. This results in minimal attenuation of the incoming signal.

This feature can be used in audio systems with good effect; at power on most op amps' outputs can swing from one rail to the next (power on bounce). Placing the power amp's output in to a high impedance state (or in effect disconnecting the power drive of the op amp from the load) removes this power on bounce.

The most frequent way of disconnecting the output of the power amp from the load is to put a POWER MOSFET in-between load and the power amp's output. This can introduce distortion and involves extra design work. The TLE2301 overcomes these problems in one integrated circuit.

2.8 TLE2301 mains line driver

In this application the TLE2301 is used in a circuit that has been designed around the requirements of a domestic electricity meter operating over the utility band (5 kHz to 95 kHz) as defined in European Standard EN50065-1.

A more detailed discussion on the TLE2301 being used as a mains line driver is contained in the TI application report: "Using the TLE2301 Power Operational Amplifier for Signal Transmission on the Mains Network". See sample and literature request form for more information.

2.8.1 Frequency band

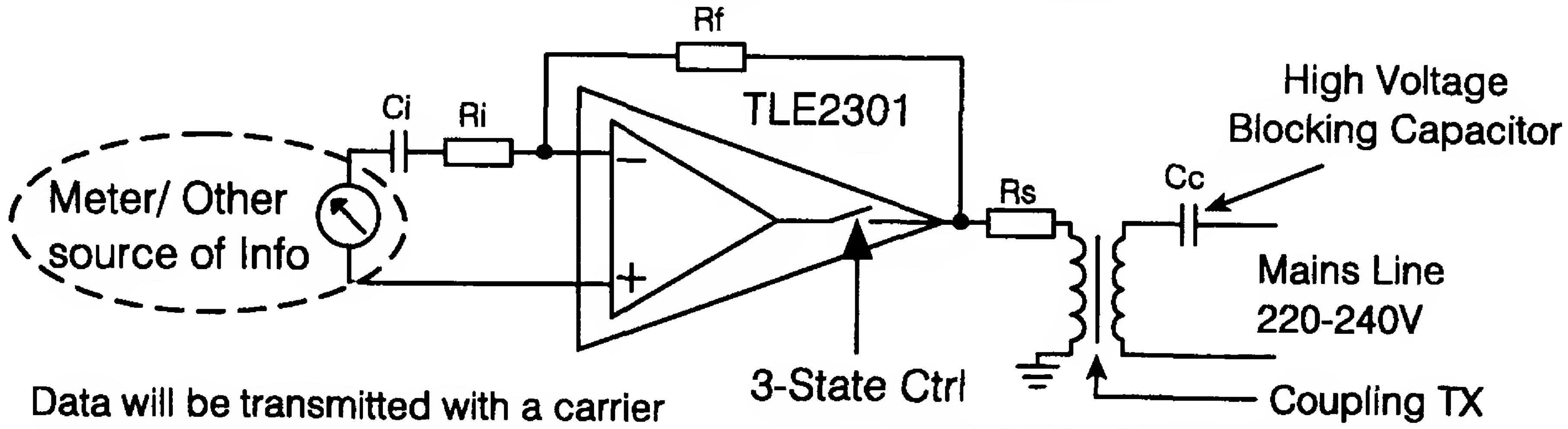
This circuit was designed for a sub-band, ranging from 40 kHz to 90 kHz. This sub-band is sufficiently wide to support multi-channel operation, say 10 channels of 5 kHz width, or more if the channel widths are smaller. To avoid transmission spill-over into the next band, a guard band of 5 kHz is allowed. So, the upper frequency of this circuit is set to 90 kHz and the lower frequency is chosen for an economical coupling network which still has sufficient bandwidth to support multi-channel operation.

2.8.2 Circuit configuration

The design methodology for this illustration is to minimise power dissipation in the TLE2301 by maximising the use of the available output voltage swing of the amplifier. The amplifier's output can swing to within 2 V of the supply rail before saturation begins. With a chosen supply of ±5 V, the maximum voltage swing is 6 V_{PP}. To ensure that the amplifier's output is not likely to clip under heavy loads, the maximum output voltage swing has been reduced by 0.5 V, giving a usable voltage swing of 5.5 V_{PP}.

TLE2301 Mains Line Driver

1 A Output Current, Wide Bandwidth, and 3-state Output Op Amp



Data will be transmitted with a carrier frequency ranging from 3 kHz up to 149 kHz.

This frequency range is split in to two main bands:

9 - 95 kHz: Utility Apps

95 - 149 kHz Consumer Apps.

The TLE2301 has been tested to EN50065-1 specs and found to be well above the minimum levels).

The blocking capacitor has a large impedance at 50 Hz, but a very low impedance at these frequencies.

Figure 1.11 - TLE2301 mains line driver

Assuming that the input signal to the transmitter stage has an amplitude of 2.8 V_{PP} (1 V_{RMS}), as might be expected if the transmission signal is digitally synthesised by circuitry operating solely from the +5 V supply. The gain of the amplifier stage is appropriately set to:

$$\text{gain} = \text{voltage swing}/V_{IN} = 5.5\ V_{PP}/2.8\ V_{PP} = 1.96$$

An inverting amplifier configuration is chosen for this example, as the input signal source is assumed to have a relatively low impedance in relation to the gain setting resistors.

A non-inverting amplifier configuration could be used when the input signal needs to be terminated with the high impedance, but the reader should take care that the amplitude of the input signal does not exceed the common mode input range ($-4\ V < V_{ICM} < +1.8\ V$ at $V_{CC} = \pm 5\ V$) for low gain implementations.

2.8.3 Component calculations

Input capacitor

The incoming signal is ac-coupled to remove any incoming dc offset and to provide only unity gain for the amplifier's input offset voltage. The value of 100 nF is chosen for this input capacitor as it has very little influence on the amplifier's signal gain over the frequency band.

Gain resistors

The gain setting resistors are chosen for a gain of 1.96, i.e.:

choosing $R_F = 4.7\ k\Omega$ and $R_I = 2.4\ k\Omega$

$$\text{gain} = R_F/R_I = 4.7\ k/2.4\ k = 1.96$$

The resistor values are low enough to ensure that the circuit will not suffer from stray capacitance and signal pick-up problems, but not too low as to significantly load the mains impedance when the amplifier is in its high impedance state.

Coupling capacitor

With such a wide frequency band, the quality factor of the coupling filter needs to be low in order to avoid unacceptably large attenuation at the band edges and to achieve a good coupling performance which is insensitive to a wide range of loads. For a bandpass filter of this configuration, the quality factor is proportional to the reciprocal of the coupling capacitance, i.e.:

$$Q \propto 1/C_C$$

For low Q, the value of C_C needs to be large.
Counterbalancing this need for a large value of C_C are two considerations. Firstly, the capacitance should not be so large as to allow significant 50 Hz mains current through the transformer ($I = 2\pi f C_C V$). Secondly, the coupling capacitor is required to be of class X or Y (see applications report), in order to meet the safety standards and these types of capacitor can be expensive, physically large, restricted in capacitance value and limited in the number of manufacturers.

As a reasonable compromise between all these factors, a coupling capacitor of 470 nF is chosen. This value is multi-sourced, moderately priced, limits the mains current through the transformer to less than 36 mA(rms) and has just sufficient capacitance to form the desired low Q filter.

Transformer leakage inductance

The centre frequency of the filter is not the same as the mid-band frequency of 65 kHz. Bandpass filters show a symmetrical shape only when plotted against the logarithm of frequency, so the centre frequency is given by:

$$f_o = \sqrt{(f_{LOWER} \times f_{UPPER})} \qquad = \sqrt{(40 \times 90)}\ \text{kHz}$$
$$= 60\ \text{kHz}$$

The leakage inductance of the transformer, as viewed from the winding connected to the coupling capacitor, is derived from $2\pi f_O = 1/\sqrt{(LC)}$. The required leakage inductance of the transformer is therefore:

$$L = 1/[\,(2\pi f_O)^2 \times C_C\,]$$
$$= 1/[\,(2\pi \times 60\ \text{kHz})^2 \times 470\ \text{nF}\,]$$
$$= 15\ \mu\text{H}.$$

Series resistor

The series resistor, R_S, is included to limit the turn-on current, the amplifier's offset current and the signalling current through the filter.

With dual supply rails, there is always a potential problem of large turn-on currents as the amplifier powers up. If one supply rail turns on before the other, the output of the TLE2301 amplifier could saturate near to the applied supply rail (3-state output can also help in removing this phenomenon), causing a large current to flow through the transformer winding ($R_{WINDING} = 0.1\ \Omega$ for the P2820 transformer) . The power supply would need to be of sufficient rating to ensure that its rails could rise to the minimum operating voltage of the amplifier, at which point the amplifier is guaranteed to have returned to stable operation.

With a series resistor of 3.3 Ω and assuming the output saturates at the maximum voltage excursion of 3 V, this turn-on current is limited to less than device's 1 A rating ($I_{TRANSIENT} = 3\ V_{PK}/3.3\ \Omega = 0.91$ A). Further reduction of this turn-on current by raising the value of the series resistor would deteriorate the filter's performance into low signalling impedances on the mains network.

Alternatively, this turn-on current could be blocked by means of a series capacitor but for this frequency band the capacitor would have to be large in value, ≥3.3 μF, so as not to adversely affect the filter. A non-polarised capacitor of this value is relatively expensive and the resistor is still required to fulfil other functions.

The second function of the series resistor is to limit the dc current flow through the transformer winding due to the dc offset at the amplifier's output, which is caused by its input offset voltage. For a worst case input offset of 20 mV, the output offset is also 20 mV as the dc gain of the circuit is unity. Offsets due to input bias currents are negligible since the values of the gain setting resistors are low. The dc current through the transformer is therefore less than 7 mA (20 mV/3.3 Ω). This low level of dc current does not appreciatively increase the power dissipation of the amplifier nor noticeably diminish the harmonic performance of the transformer.

The final function of the series resistor is to limit the signalling current in the event that the mains impedance might appear as solely reactive, i.e. without a resistive component. As a rough estimate, the peak signal current from the amplifier is:

$$I_{OPK} = V_{OPK} / R_S$$
$$= (5.5\ V_{PP}/2) / 3.3\ \Omega$$
$$= 833\ mA_{PK}$$

Again, the value of the series resistor is sufficient to limit the peak signal current below the device's maximum rating. This calculation does not take into account other resistive impedances in the signal path which would further reduce the peak signal current from the amplifier.

Transformer turns ratio

The last parameter that needs to be defined is the turns ratio, n, of the transformer. The turns ratio is set so that the transmission level is just within the acceptable limits specified in the EN50065-1 standard when the circuit is driving into the artificial mains network. The maximum permitted transmission level falls from 125.1 dB at 40 kHz down to 120.3 dB at 90 kHz.

Since the high frequency roll-off of our simple filter into the artificial mains network does not fall as fast as the limits, the turns ratio is chosen for an intersection of the respective curves at 90 kHz. In this way, our transmission level is always equal to or less than the specified limits.

The calculation for the turns ratio is not straightforward due to the presence of numerous complex impedances. The simplest method for deriving the turns ratio is to model the circuit with an analogue simulation program, such as PSpice®. From these simulations, the turns ratio of 1.67:1 was found to achieve the required circuit performance.

2.8.4 Circuit model

All model component values are derived with respect to viewing the circuit from the load side of the transformer. Impedances on the amplifier side of the transformer are represented with a transformed value of $1/n^2$ times their actual value, and in the text will be referred to as 'component$_{\text{-REFLECTED}}$'.

Where:

V_{AMP}	is the output of the op amp referred to the load side of the transformer.
$R_{S\text{-REFLECTED}}$	is the reflected value of the series resistor
$R_{T\text{-AMP}}$	is the reflected value of the transformer's amplifier-side winding resistance.
$L_{T\text{-AMP}}$	is the reflected value of the transformer's amplifier-side leakage inductance.
$L_{T\text{-LOAD}}$	is the load-side leakage inductance of the transformer.
$L_{T\text{-SHUNT}}$	is the shunt inductance of the transformer.
$R_{T\text{-LOAD}}$	is the load-side winding resistance.
C_C	is the coupling capacitance.
R_{CC}	takes into account the losses of the coupling capacitor.

Component models

The power amplifier is modelled as a voltage source with negligible source impedance. However, the source impedance of the power amplifier could become significant when high frequency and/or high gain configurations are implemented. The formula for calculating the amplifier's closed loop source impedance is:

$$
\begin{aligned}
Z_{AMP\text{-}CL} &\approx Z_{AMP\text{-}OL} \times \frac{f_O}{B_1} \times \frac{R_I + R_F}{R_I} \\
&\approx 1 \times \frac{60 \times 10^3}{8 \times 10^6} \times \frac{2.4 + 4.7}{2.4}\ \Omega \\
&= 0.02\ \Omega
\end{aligned}
$$

where $Z_{AMP\text{-}OL}$ = open loop output impedance = 1 Ω

and B_1 = unity gain bandwidth = 8 MHz

The transformed value of the output voltage of the TLE2301 is:

$$
\begin{aligned}
V_{AMP} &= V_{O\text{-}RMS} / n \\
&= [5.5V_{PP} / (2\sqrt{2})]/1.67 \\
&= 1.16\ V_{RMS}
\end{aligned}
$$

The series resistor has a reflected value of:

$$
\begin{aligned}
R_{S\text{-}REFLECTED} &= R_{S\text{-}ACTUAL} / n^2 \\
&= 3.3 / 1.67^2 \\
&= 1.18
\end{aligned}
$$

From the gauge of wire that is used in winding this transformer, the value of $R_{T\text{-}LOAD}$ is anticipated to be 0.1 Ω.

As the transformer's winding resistance is proportional to the square of the number of turns, the actual value of $R_{T\text{-}AMP}$ will be n^2 times greater than $R_{T\text{-}LOAD}$. When viewed from the load side of the transformer, this increase in resistance is counterbalanced by the transformation factor. The reflected value of $R_{T\text{-}AMP}$ is:

$$
\begin{aligned}
R_{T\text{-}AMP} &= (R_{T\text{-}LOAD} \times n^2) / n^2 \\
&= R_{T\text{-}LOAD} \\
&= 0.1\ \Omega
\end{aligned}
$$

A similar relationship also exists for the leakage inductances, where the reflected value of $L_{T\text{-}AMP}$ is equal to $L_{T\text{-}LOAD}$. The sum of these leakage inductances was previously calculated to be 15 µH, so:

$$
\begin{aligned}
L_{T\text{-}AMP} &= L_{T\text{-}LOAD} \\
&= 7.5\ \mu H
\end{aligned}
$$

The shunt inductance for this type of transformer is anticipated to be:

$$
\begin{aligned}
L_{T\text{-}SHUNT} &\approx 50 \times L_{T\text{-}LOAD} \\
&= 375\ \mu H
\end{aligned}
$$

The coupling capacitor exhibits some loss, represented as a resistive component, R_{CC}, in the model. Manufacturers specify this loss in terms of the parameter tanδ, which shows an increase with frequency for metallised paper capacitors.

For a metallised paper capacitor at 65 kHz, the value of tanδ is 0.025, giving a resistive component of:

$$
\begin{aligned}
R_{CC} &= \tan\delta / (2\pi f.C_C) \\
&= 0.025 / (2\pi \times 65\ kHz \times 470\ nF) \\
&= 0.13\ \Omega
\end{aligned}
$$

In summary, the circuit model has the following values:

$$\begin{aligned}
V_{AMP} &= 1.16\ V_{RMS} \\
R_{S\text{-}REFLECTED} &= 1.18\ \Omega \\
R_{T\text{-}AMP} &= R_{T\text{-}LOAD} = 0.1\ \Omega \\
L_{T\text{-}AMP} &= L_{T\text{-}LOAD} = 7.5\ \mu H \\
L_{T\text{-}SHUNT} &= 375\ \mu H \\
C_C &= 470\ nF \\
R_{CC} &= 0.13\ \Omega
\end{aligned}$$

2.8.5 Power dissipation

Worst case

With the component values selected, the power dissipation within the components can be checked to ensure that none of the components are over-stressed. The easiest method of deriving the currents and voltages throughout the circuit is with the simulation program.

The communications system may be sited very close to highly reactive loads, e.g. EMC filters or power factor correctors. In the extreme case, these reactive loads may appear with a negligible resistive component. The signalling current from the communications circuit is then only limited by its own resistive components. As a simple means of simulating this situation, a load of 0 Ω is used.

With a worst case load of 0 Ω, the simulation indicates a maximum signalling current of 780 mA rms through the coupling capacitor. The power dissipation in this capacitor, due to the signal current, is:

$$\begin{aligned}
P_{CC} &= I_{LOAD}^2 \times R_{CC} \\
&= 0.78^2 \times 0.13 \\
&= 79\ mW
\end{aligned}$$

This value of power dissipation in the coupling capacitor is below the design safety limit of 250 mW.

Assuming that the core losses are negligible, the power dissipation in the transformer is:

$$\begin{aligned}
P_T &= 2.I_{LOAD}^2.R_{T\text{-}LOAD} \\
&= 2 \times 0.78^2 \times 0.1 \\
&= 121\ mW
\end{aligned}$$

The signalling current flowing through the series resistor is:

$$\begin{aligned}
I_{RS} &\approx I_{LOAD}\ /(\text{turns ratio}) \\
&= 0.78\ /\ 1.67 \\
&= 467\ mA_{RMS}
\end{aligned}$$

The power dissipation of the series resistor is:

$$\begin{aligned}
P_{RS} &= I_{RS}^2 \times R_S \\
&= 0.467^2 \times 3.3 \\
&= 720\ mW
\end{aligned}$$

The resistor will need a continuous power rating greater than 720 mW. The resistor will also need to withstand the turn-on transient with an instantaneous power dissipation up to 3.3 W (assuming ≤1 A peak current).

The peak signalling current from the amplifier is:

$$\begin{aligned} I_{AMP\text{-}PK} &= I_{RS\text{-}RMS} \times \sqrt{2} \\ &= 0.467 \times \sqrt{2} \\ &= 660\ \text{mA}_{(PK)} \end{aligned}$$

which shows that the large output drive of the amplifier is essential if the circuit is to correctly drive into highly reactive loads on the mains network.

Given a maximum quiescent current of 25 mA, the power dissipation in the amplifier under worst case conditions is:

$$\begin{aligned} P_{AMP} &= 2 \times V_{CC} \times I_{CC} + 2 \times V_{CC} \times I_{AMP\text{-}PK}/\pi - P_{CC} - P_T - P_{RS} \\ &= 2 \times 5 \times 25 + 2 \times 5 \times 660/\pi - 79 - 121 - 720 \ldots\ldots\text{mW} \\ &= 1.43\ \text{W} \end{aligned}$$

Device junction temperature

The TLE2301INE can use the PCB as a heatsink ($R_{\theta JA}$ of 34°C/W), and so at an operating temperature of 85°C, the TLE2301's junction temperature is:

$$\begin{aligned} T_J &= T_A + (R_{\theta JA\text{-}PCB} \times P_{AMP}) \\ &= 85°\text{C} + (34 \times 1.43) \\ &= 134°\text{C} \end{aligned}$$

which is safely below the maximum junction temperature of 150°C.

This example discusses some of the aspects that should be considered when using the TLE2301 as mains line driver. A more detailed discussion on the TLE2301 being used as a mains line driver is contained in the TI application report: "Using the TLE2301 Power Operational Amplifier for Signal Transmission on the Mains Network".

2.9 TLC247x integrated loudspeaker drivers for speech systems.

The TLC247x family is ideal for use in speech systems since it greatly simplifies the design of loudspeaker driving circuitry. In fact, an 8 Ω loudspeaker can be driven directly at up to 0.5 W_{pk} from analogue or PWM speech signals using this single chip solution.

Device	Corner frequency (kHz)	A_{vd} (V/V)
TLC2470	5	2
TLC2471	3.5	2
TLC2472	5	1
TLC2473	3.5	1

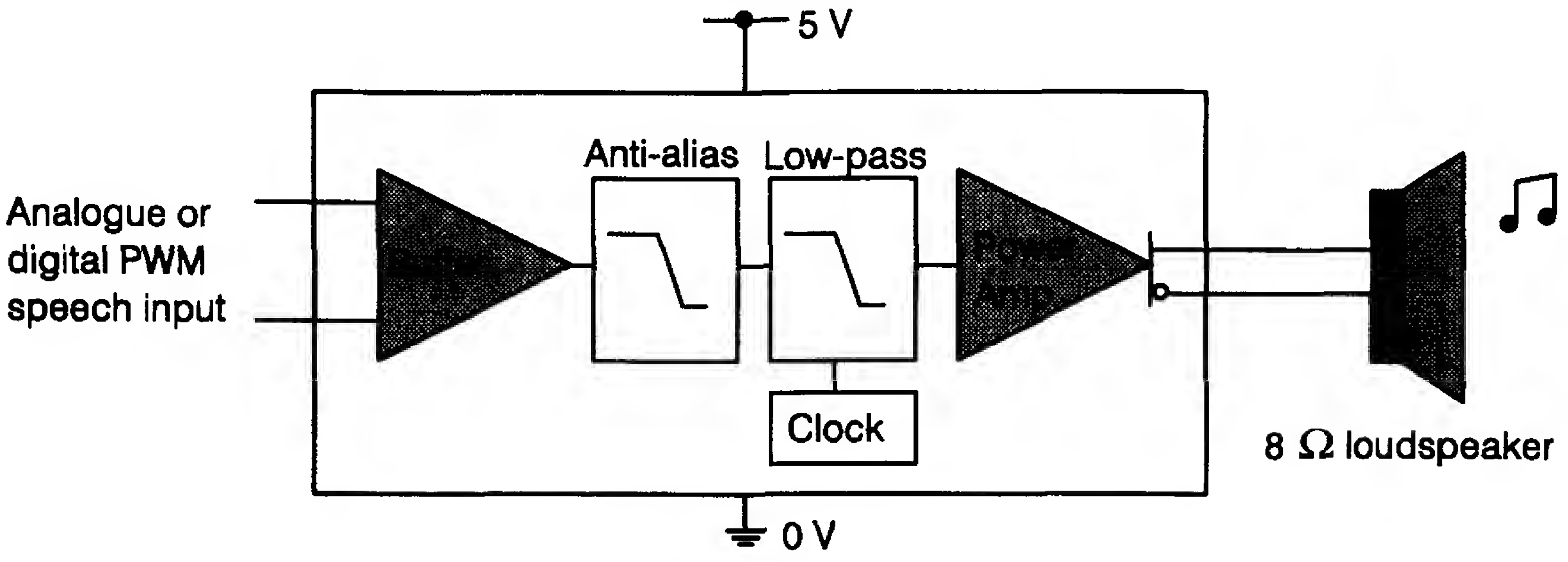
Input buffers, loudspeaker power drivers, filters and power-down circuitry are all integrated on chip; the only external components required to complete the audio system are typically a capacitor and a variable resistor. The resulting design is therefore smaller, simpler and more quickly completed.

Since the TLC247x family can be driven by either analogue or PWM signals (for digital speech), a DAC can be eliminated from a digital sound system bringing a large cost and board space saving.

Buffers at the input of the device can be used either in single-ended or differential mode. The latter is particularly useful for low-noise operation and accommodates differential

PWM signals from dedicated speech synthesisers such as the TSP50Cxx series from Texas Instruments.

TLC247x integrated loudspeaker drivers for speech systems



- Single supply +5 V
- Single chip solution
- Drives 8 Ω speaker to 0.5 W
- Auto power-down mode Icc=50 μA typ
- Analogue or digital speech PWM inputs
- Interface to TSP50Cxx speech synthesizers

Figure 1.12 - TLC247x integrated loudspeaker drivers for speech systems

Two amplification selections of the TLC247x are available allowing use of the full 5 V or just 2.5 V of input swing. This allows the elimination of external input signal biasing circuits.

Integrated switched capacitor filters remove high frequency noise, especially useful in PWM mode, and prevent aliasing between the input signal and the filter clock.

Two power amplifiers at the output enable the TLC247x to drive a standard 8 Ω loudspeaker at up to 0.5 W_{pk} without any additional external components. When used in PWM mode, the loudspeaker volume can be controlled using a single pin connection.

In portable equipment, battery life is maximised by the TLC247x's power-down function which switches the device automatically to a 50 μA standby mode when no input signal is present.

2.10 Hands-free telephone line monitor.

Figure (1.13) shows the TLC2470 in a simple application demonstrating how the integration of functions can simplify loudspeaker drive design. The circuit is a simple hands-free telephone line monitor and makes use of the TLC2470's differential input mode. When no speech is present on the line, the TLC2470 goes into an automatic power-down mode, where I_{cc}=50 μA typ, so conserving battery power. As soon as a call is made, the TLC2470 wakes up automatically and drives the loudspeaker with the line speech.

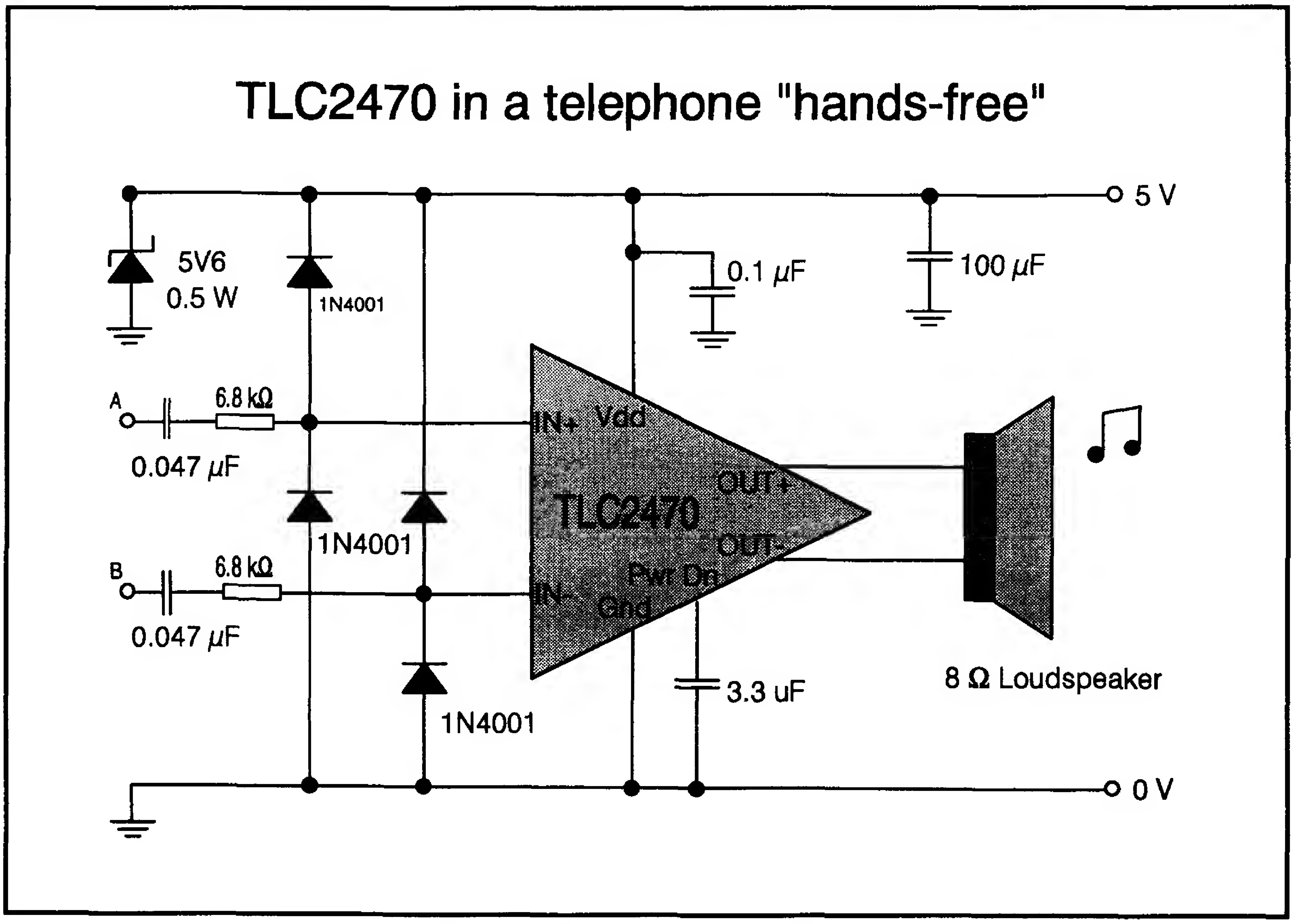


Figure 1.13 - TLC247x in a telephone 'hands-free'

The two 0.047 µF input capacitors are of the Class Y type, specified for 250 Vac operation; this is to ensure that the circuit is properly isolated from the telephone line. The value is chosen to roll off in combination with the input impedance of the TLC2470 at above the 5 kHz maximum frequency of interest. The 6.8 kΩ resistors on each line limit current through the 1N4001 diodes which provide proper clamping between the inputs and the power rails to limit line transients.

The 3.3 µF electrolytic capacitor at the Power-Down pin controls the power-down timing. With this recommended value, the device will switch when there is no input signal typically after 0.5 s.

It should be noted that this design is not approved for connection to the Public Switched Telephone Network.

2.11 Use of the TLC247x with a speech synthesiser.

The TLC247x family will interface directly to TI's TSP50Cxx family of speech synthesisers for speech system applications. The overall control of sounds, words and sequence comes from a general purpose micro-processor which sends encoded speech data to the synthesiser. The latter reproduces the original speech using an electronic vocal tract model and Linear Predictive coding. This gives an excellent trade-off between the memory required for sound storage and the final speech quality. Quality can be further enhanced by filtering of the speech in the output circuits which drive the loudspeaker. This could be done with op-amps and filters, however the TLC247x family gives a high-performance integrated solution to this.

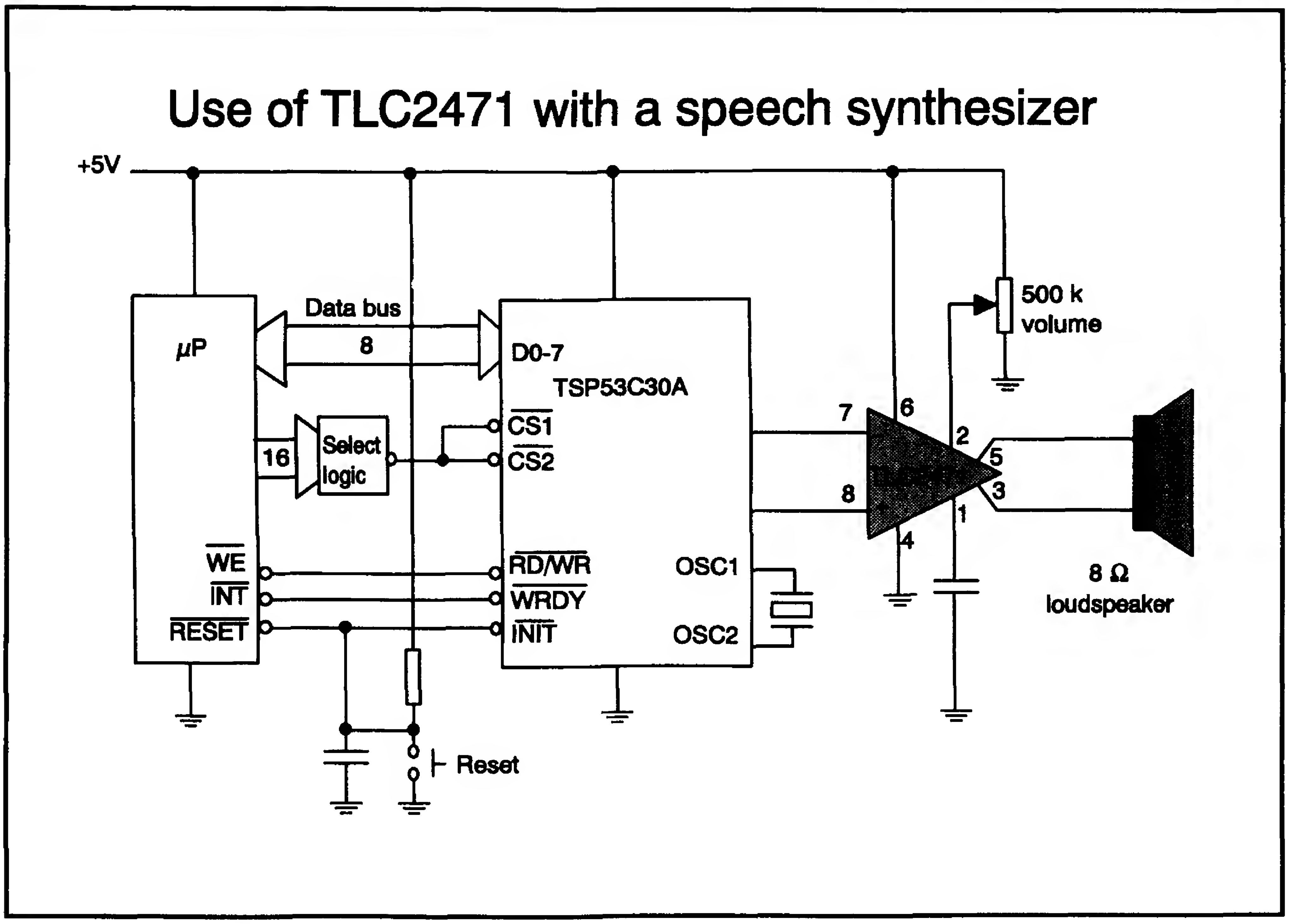

Use of TLC2471 with a speech synthesizer
+5V
µP
Data bus
8
16
Select logic
D0-7
TSP53C30A
CS1
CS2
WE
INT
RESET
RD/WR
WRDY
INIT
OSC1
OSC2
Reset
7
8
6
2
5
3
1
4
500 k volume
8 Ω loudspeaker

Figure 1.14 - Use of TLC247x with a speech synthesiser

3 Single supply signal conditioning

3.1 Single supply signal conditioning

When choosing the power supply there are several factors that must be taken in to consideration. One thing is the dynamic range.

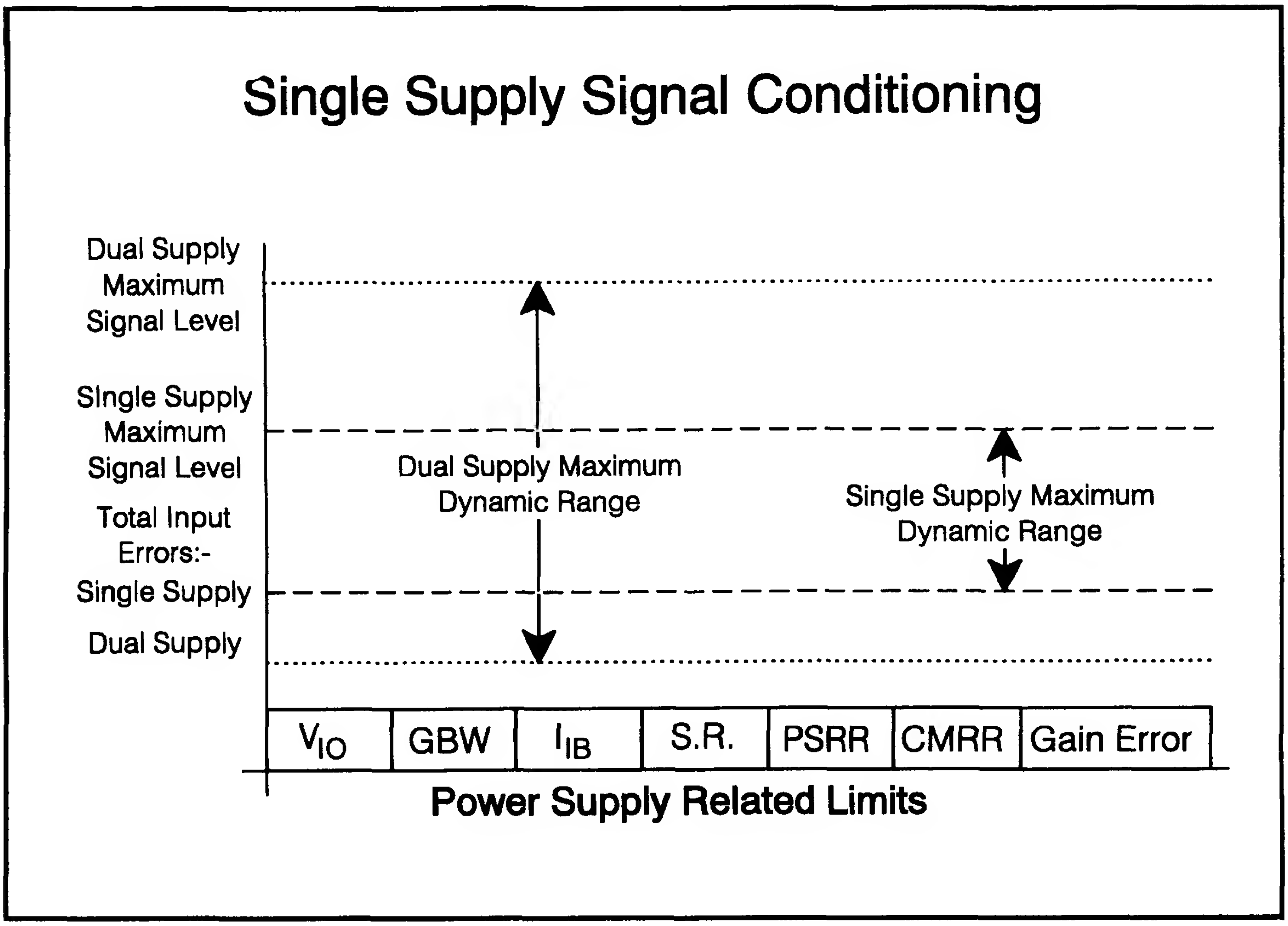

Single Supply Signal Conditioning
Dual Supply Maximum Signal Level
Single Supply Maximum Signal Level
Total Input Errors:-
Single Supply
Dual Supply
Dual Supply Maximum Dynamic Range
Single Supply Maximum Dynamic Range
V_IO
GBW
I_IB
S.R.
PSRR
CMRR
Gain Error
Power Supply Related Limits

Figure 1.15 - Single supply signal conditioning

If the supply voltage is reduced from ±15 V down to +5 V, then the available dynamic range has been reduced by about 80%, which is entirely due to the fact that the available output voltage swing has been reduced.

The reduction in power supply will have the greatest effect on devices that have been designed for operation at ±15 V. Reducing the supply voltage will have an impact on the quiescent current of the op amp. This can affect the whole operation of the op amp due to changes in the operating point of the op amp.

An op amp designed for ±15 V operation will have been designed for its inputs to stay around 15 V above its negative rail. If the supply voltage is reduced to +5 V, then its input will now be around 2.5 V above the negative rail, this will subject the op amp to large common-mode and large supply voltage changes which will impact the offset voltage of the device.

The change in supply voltage and quiescent current can also impact its ac performance:- slew rate and gain bandwidth product.

It is, therefore, quite often better to choose an op amp designed specifically for 5 V operation rather than choose an op amp which has very good specifications at ±15 V. The device designed for ±15 V might not even work at +5 V!

3.1.1 Power Supply Effects

The variances or changes in the applied power supply voltages will affect the characteristics of both the input and output stages.

Common-Mode Input Voltage Range

The limiting factor on an op amp's input voltage range is when its input stage starts to turn off. This can be when the current source to the differential input stage cannot provide any more current due to its finite saturation voltage. Or it can be when the input transistors themselves have been driven so hard that they have reached their finite saturation voltage. The latter state can quite often cause gain inversion, because as well as causing the inputs stage to turn off it can cause the next stage to turn off. The saturation limits of the input stage to an op amp is related to the actual supply voltage, and so as the supply voltage varies the op amp's common-mode input range will also track it. There are ways of overcoming this, and this is particularly relevant for single supply op amps where the inputs must be capable of swinging down to the negative rail.

Peak Output Voltage Range

There are a number of different output stage configurations. For low distortion and dual rail operation a class AB output stage is often used. This often results in the output stage being capable of swinging to only 1.5 V of the supplies. So as the supply voltage varies the maximum output swing will track it.

Single supply op amps will have a different output stage enabling them to swing to the negative rail. However most of these devices still do put a limit on their positive output swing. So even though the output can swing to ground (negative rail for single supply systems) the positive supply still tracks the supply voltage with a 1.5 V drop-out.

Supply Current

The biasing circuitry of the op amp will consist of a series of current mirrors, however, these ultimately be controlled by some resistor and reference. These will have some dependence on the supply voltage and so some variance in the supply current will be seen as the supply voltage varies. The variance in supply current will affect every current mirror and so will affect every parameter of the op amp; dc and ac.

Differential Gain

The differential gain of the op amp is heavily dependent on the supply current of the op amp so as the supply current varies the open loop gain will also vary. Most devices show a positive increase in gain with supply voltage increase.

Unity Gain Bandwidth

The unity gain bandwidth of an op amp is dependent on the gain of the op amp and on size of compensation capacitor. As the supply current increase the gain increases, and this will lead to the bandwidth increasing. As will the slew rate of the device

All these parameters and more are affected by the supply voltage, and so when operating devices specified for ±15-V operation special care must be taken if their supply voltage is reduced.

It is for some of these reasons that the single supply op amp was developed.

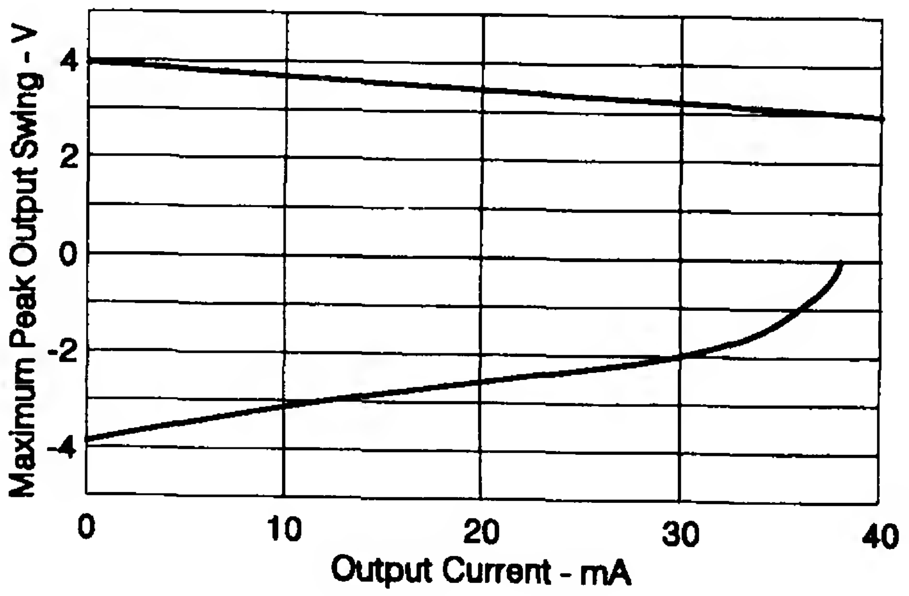
3.2 TLE2662/82 charge-pump + dual op amps

There are a lot of applications where it would be nice to have the performance of BiFET op amps from a single 5-V supply. The TLE2662 and TLE2682 devices from TI. combine a TLE2062 (TLE2082 for the TLE2682) dual op amp with a charge-pump, thereby providing you with a BiFET op amp capable of operating from a single 5-V supply.

TLE2662/82 Charge Pump + Dual Op Amps

Dual Rail High Performance Op Amps from a Single Supply

- Produces a dual rail for single supply systems.
- High Current Negative Rail Generator
  Upto -100 mA
- High Output Current Op Amps
  In excess of 25 mA
- MicroPower TLE2662
  Icc = 600 μA
- High Speed TLE2682
  B1 = 10 MHz



Applications
2-4 Wire Converters
Portable Instrumentation

Figure 1.16 - TLE2662/82 charge-pump + dual op amps

One advantage of most BiFETs is that their inputs will typically swing beyond the positive supply voltage. This has, in the past, made them useful for current sensing applications. Combining the TLE2062 and TLE2082 with a charge-pump results in two op amps with effective common mode input ranges that include both applied supply rails.

The inclusion of the charge-pump also allows it to sink current beyond the applied negative supply voltage; that is the output can sink in excess of 25 mA whilst maintaining an output voltage of less than 0 V.

The charge-pump can also be used to supply current, around 100 mA, to other circuitry. This makes the device well suited to portable systems where board space and weight are of premium importance.

The TLE2662 and TLE2682 provide high performance dual rail operation from a single rail in the same space that standard charge-pumps in surface mount take. For example the TLE2662/82 are available in a 16 pin wide body small outline package, the LT1054 which is just a charge is available in an 8-pin PDIP and 16-pin SOWB! The TLE2662/82 can be used to provide a negative rail for the rest of the system as well as providing the negative rail for itself.

3.2.1 TLE2662

The TLE2662 combines the features of the TLE2062 with the simplicity of a charge-pump, enabling it to operate from a single 5-V supply. The TLE2062 has gained wide acceptance in low quiescent power applications that require a large output current. These include 2-4 wire converters. The negative rail of the system can be switched off thereby drastically reducing the overall power consumption.

3.2.2 TLE2682

The TLE2682 provides a high speed BiFET that is capable of operating from a single supply. Even when being used in conjunction with the charge-pump the TLE2682 still maintains the 10 MHz bandwidth and 40 V/µs slew rate of the TLE2082. This makes the TLE2682 ideal for portable audio applications that require good ac performance whilst on the move.

The TLE2682 could once again have its negative rail switched off when not required, thereby increasing overall system operating time. As the computer systems move to multi-media applications the need for high quality audio amplifiers will increase. The TLE2682's need for only one supply rail makes it especially well suited to these applications.

3.3 Dual rail high performance from a single supply

An ideal application for the TLE2662/82 are where they are being used in a 5-V single supply system, and are therefore supplying their own negative supply.

Their charge-pump can be used in two modes (excluding shutdown mode):

Free or open loop operation - where no feedback around the charge-pump is applied.

Closed loop operation - A proportion of the negative supply voltage is fedback to pin 9 (FB/SD) and is directly compared with the reference (VREF pin 6) the regulation of the negative supply is improved. This is covered in more detail in the application information section of the datasheet on the TLE2662 and TLE2682 datasheets, which are included in the seminar databook.

The high input impedances of the TLE2662/82 op amps make them ideal for interfacing to high impedance transducers. In single supply applications where the sensor is referred to ground half of the output signal could be lost due to the output being limited to only positive swings. The charge-pump included in the TLE2662/82 allows their op amp's outputs to swing below ground, making it ideal for interfacing to transducers that are referenced to ground.

With an increase in single 5 V systems the dual supply capability of the TLE2662 and TLE2682, and their increased output swing capability, can be used to increase the dynamic range available from a single 5 V supply.

The TLE2662 and TLE2682 have an internal reference which is available as an output. The reference is available for use in other parts of the system and outlines another advantage of the TLE2662 and TLE2682 devices; it can provide both a negative rail and a reference for the whole of the system. N.B. the reference is only accurate to within about 6%.

3.3.1 Charge-pump

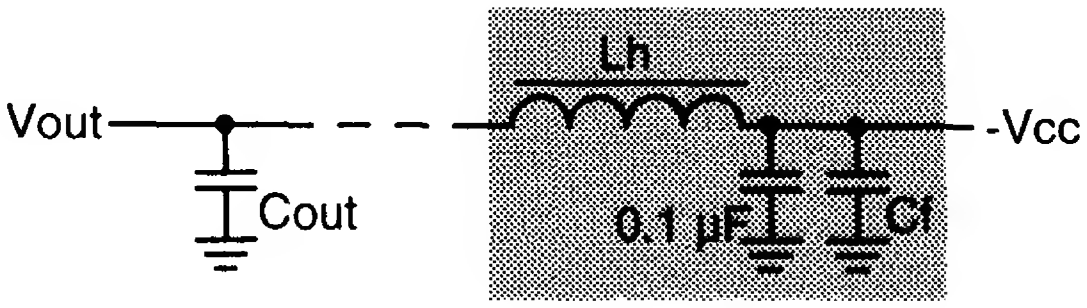
The negative output of the charge-pump of the TLE2662/82 is connected to the substrate of the device, this means that the device can be susceptible to start-up problems if the negative output of the device is brought above its ground pin. This can quite often happen driving loads that are not directly connected to ground.

One such example is an op amp; no general purpose op amp has a low impedance 0 V connection, so the charge-pump of the TLE2662 will see the op amp as a load referred to the positive rail. Whether or not this creates a problem depends on the load the op amp is trying to drive.

One way of removing any likelihood of problem is to use a fast recovery diode, such as the 1N4933 with its low forward voltage (0.2 V), to clamp the output of the charge-pump close to ground during start-up.

One advantage of charge-pumps are that they do not normally require the large bulky inductors of standard switching regulators. The charge-pump can however be more susceptible to ripple effects and switching noise. The noise will be present on both the negative rail and the ground. These effects will be increased as the load current is increased.

Increasing the output capacitance will reduce the level of noise and ripple, however other steps may need to be taken if the ripple is too large. Placing a small choke in series with the output after the output capacitor with an extra capacitor can help to reduce the problem (see below). The 0.1 µF capacitor is the standard decoupling capacitor as recommended by most manufacturers.



An additional way of reducing the noise on the ground and the negative rail is to disable the charge-pump. Applying a voltage of less than 0.45 V to the FB/SD pin turns off the internal switches. This results in the outputs of the op amps being free of noise during the period of time that the charge-pump is turned off. The rate of decay of the negative rail is dependent on the size of output capacitor and the loading of the output of the op amps.

For more details see the application information section in the TLE2662 and TLE2682 datasheets.

3.4 Single supply 2-4 wire converter

Driving transmission lines creates extra demands on any operational amplifier. These demands are clearly shown in an application where the op amp needs to drive a 600 Ω transformer coupled telephone line with the minimum of distortion.

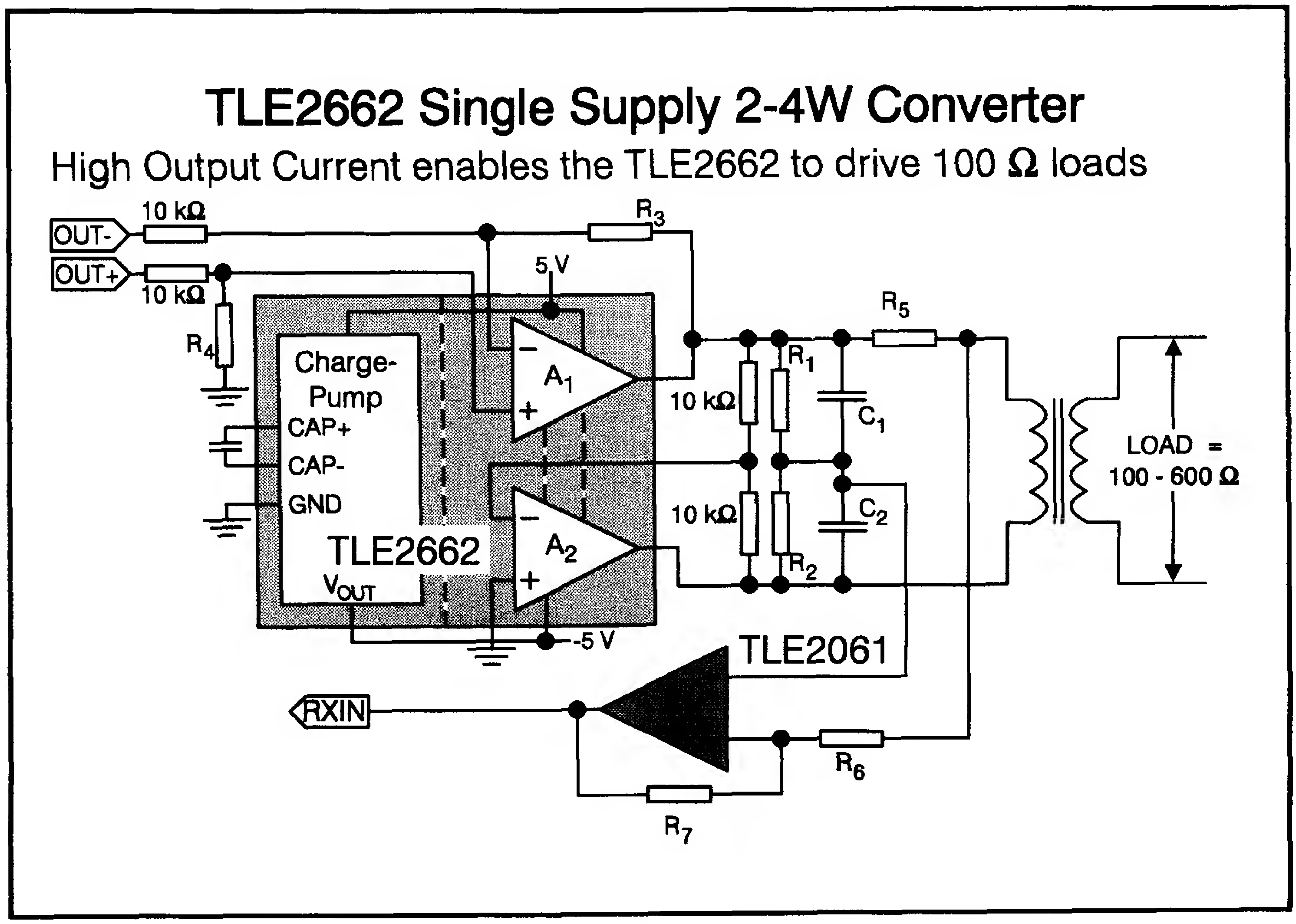

TLE2662 Single Supply 2-4W Converter
High Output Current enables the TLE2662 to drive 100 Ω loads
OUT-
OUT+
10 kΩ
10 kΩ
R3
5 V
R4
Charge-
Pump
CAP+
CAP-
GND
TLE2662
VOUT
A1
A2
-5 V
10 kΩ
10 kΩ
R1
R2
C1
C2
R5
LOAD =
100 - 600 Ω
TLE2061
RXIN
R6
R7

Figure 1.17 - TLE2662 single supply 2-4 wire converter

The schematic shown in figure 1.17 shows the TLE2662 being used as a differential telephone line driver. Amplifiers A1 and A2 are used to amplify the differential output, OUT+ - OUT-. while $B_1$is used for amplifying the received signal.

The telephone line is used to carry information in both directions, which minimises cable costs. This results in the primary of the isolating transformer acting as both input and output to and from the line. So when the modem is driving the line (via OUT+ and OUT-) some of the signal will be fed back to the input of the modem, Rin, by amplifier B_1. This signal is reduced by the R_1, R_2, C_1 and C_2 network: The output of A1 is fed to the non-inverting input of A2 and is subtracted from the primary voltage. Careful choice of R_1, R_2, C_1 and C_2 minimises any signal from the output of the modem being fed to Rin.

To maximise the drive, the line is driven differentially. A_1 acts as a differential to single ended amplifier. A_2 is configured as an inverting amplifier thus producing an inverted version of the output of A_1. As the system is duplex the output impedance of A_1 and A_2 must match the impedance of the line and transformer. However, in order to achieve low distortion the output impedance of A_1 and A_2 must be low. The **TLE2662** was designed for applications requiring such a high drive capability and at the same time a low quiescent power consumption. The TLE2662 is capable of operating from ±15 V down to

±3.5 V, and when driving a 100 Ω load from a ±5 V supply has a guaranteed minimum output swing of ±2.5 V. It provides this output with a very low level of distortion.

Any distortion produced by the op amp will be sent down the telephone line via the transformer and will also be fedback to the receiver at Rin. The limited bandwidth of the transformer' will help to reduce some of the distortion sent down the line, but it cannot reduce the distortion fedback to Rin. The distortion fedback to Rin is difficult to counteract, thus decreasing the quality of the telephone system.

To match the line's impedance, the TLE2662 has to have a series resistor R_5 on its output. R_5 will form a potential divider with the winding resistances of the transformer and the line impedance. Over the frequency range of interest, the matching transformer will add phase shift to the output to the line. So the choice of R_1, R_2, C_1 and C_2 should take this potential division and phase shifting into account. Looking from the line the impedance seen will be the winding resistances in series with R_5, and so R_s should equal the line impedance minus the winding resistances:-

$$R_s = Z_{line} - (r_p + r_s)$$ .... where $r_s + r_p$ are the primary and .... secondary winding resistances .... of the transformer

The actual impedance of the telephone line can vary enormously from the typical 600 Ω, ranging from 1200 Ω down to 100 Ω. The line impedance is greatly affected by the position of the 2 - 4 wire converter in the system, this will greatly affect the gain of A_1 and the values of R_5, R_1, R_2, C_1 and C_2. In this application, assuming ideal impedance of the line, the low output impedance of the TLE2662 means that the series resistor, R_5, will need to be around 510 Ω, ($r_s + r_p = 100\ \Omega$).

3.4.1 Echo cancellation

Any signal from the output of the modem fedback to the input of the modem can appear as an annoying echo. If this annoying echo is to be removed then the signal from A_1 and A_2 that is applied to the line must be removed from the output of B_1. This is normally done by feeding a proportion of the total output to the line back to the non-inverting input of B_1. This is done via resistors and parallel capacitors R_1, R_2, C_1 and C_2.

The absolute voltage at the non-inverting input of B_1 is given by:-

$$\begin{aligned} V_+ &= V_{O+}\frac{Z_2}{Z_1+Z_2} + V_{O-}\frac{Z_1}{Z_1+Z_2} \\ &= V_{O+}\frac{Z_2-Z_1}{Z_1+Z_2} \end{aligned}$$

Where Z_1 and Z_2 are the equivalent impedances of $R_1$and C_1, and R_2 and C_2 respectively. And V_{O+} and V_{O-} are the non-inverting and inverting outputs of the differential line driver.

The voltage on the transformer just after R_5, V_L, is equal to:-

$$\begin{aligned} V_L &= V_{O+}\frac{r_s + r_p + Z_L}{R_5 + r_s + r_p + Z_L} + V_{O-}\frac{R_5}{R_5 + r_s + r_p + Z_L} \\ &= V_{O+}\frac{r_s + r_p + Z_L - R_5}{R_5 + r_s + r_p + Z_L} \end{aligned}$$

.... Where Z_L is the line impedance

Amplifier A_3 subtracts V_L and V_+ from one another, via different inverting and non-inverting gains. So the voltage at Rin equals:-

$$V_{Rin} \quad = \quad V_{O+}\left(\frac{R_6+R_7}{R_6}\right)\frac{Z_2-Z_1}{Z_1+Z_2} - V_{O+}\left(\frac{R_7}{R_6}\right)\frac{r_s+r_p+Z_L-R_5}{R_5+r_s+r_p+Z_L}$$

Letting R_6 = 18 kΩ, and R_7 = 36 kΩ, sets a receiver gain of -2. A value of 18 kΩ reduces any effects of R_5 and Z_L on the gain of B_1. With a line impedance of 600 Ω, and r_s+r_p = 100 Ω, and R5 = 510 Ω, the output voltage of B_1 simplifies to:-

$$V_{Rin} \quad = \quad V_{O+}\left(3\frac{Z_2-Z_1}{Z_1+Z_2} - 2\frac{700-510}{510+700}\right)$$

The ideal value for the output of B_1in this case would zero, this makes:-

$$3\frac{Z_2-Z_1}{Z_1+Z_2} \quad = \quad 2\frac{700-510}{510+700}$$

$$Z_1 \quad = \quad \frac{325}{401}Z_2$$

This sets the resistor ratios for R_1 and R_2. The values for capacitors heavily depend on the frequency response of the line and transformer, and can be best determined via tests. If the frequency characteristics of the line and transformer are known then the reactive component of the line impedance, Z_L, should be taken into account, and this can be used to determine the values for C_1 and C_2.

3.5 TLC2272/4 dual and quad rail-to-rail op amps

Most op amps will have been designed to work in either single rail or dual rail applications. This will normally limit the common-mode input range and the output voltage swing.

BiFET op amps have been designed for dual supply rails and hence their outputs cannot swing to either rail, while their inputs can only typically swing to the positive rail. High performance bipolar op amps have been designed for dual supply applications, and so will not normally allow their inputs or outputs to go to either rail. Most single supply op amps have had their inputs and outputs designed so that they can swing to ground. This is at the expense of their outputs being able to sink and source current.

To get over the problems of output swing the TLC2272 and TLC2274 use a push-pull output stage.

TLC2272/4 Dual and Quad Rail-Rail Op Amps

Low Noise and Rail-Rail Output Swing Increases Dynamic Range

- Output swing includes both supply Rails
- Common Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Errors
  - Vio = 950 µV @ 25°C
  - Iib = 1 pA @ 25°C
- Low Noise
  - Vn = 9 nV/√Hz @ 25°C
  - In = 2.8 fA/√Hz @ 25°C

Applications

5-V and ±5-V system ADC Interface

High impedance transducer interface

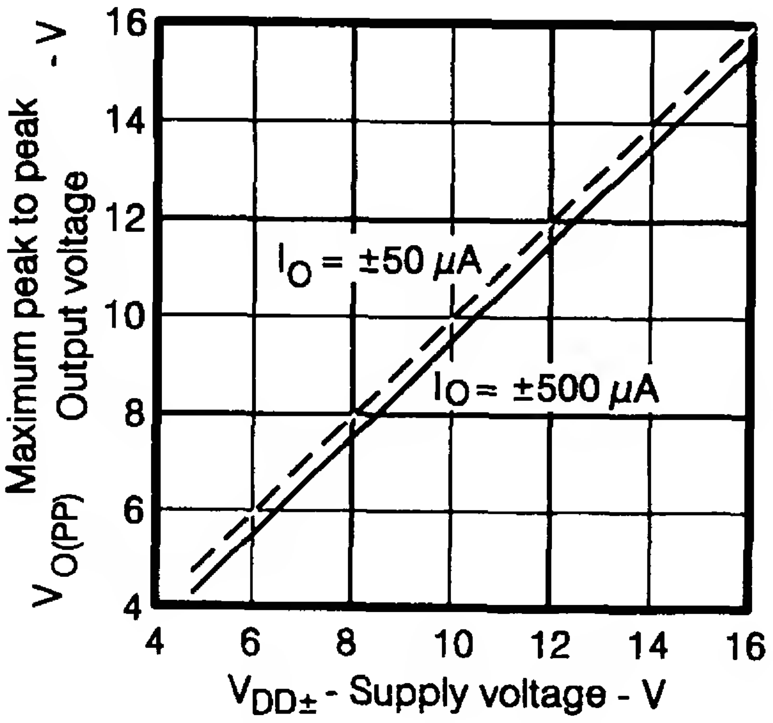


Figure 1.18 - TLC2272/4 dual and quad rail-to-rail op amps

The push-pull output stage enables the TLC2272/4 to swing within millivolts of both rails while sinking and sourcing current. This capability enables the device to work in both single supply applications (operating in Class A) and dual supply applications (operating in Class AB). This is very important when providing signal conditioning for ADCs, normal single supply op amps have their outputs clipped 1 V from the positive supply, which reduces the dynamic range of the ADC by 20%.

The wide output swing and low input offset errors $V_{IO} < 1$ mV and $I_{IB} = 1$ pA (Typ), make it suitable for high impedance transducer interfacing. Its capability for use in these applications is enhanced by its low noise specification.

All these features give it one huge advantage over other general purpose CMOS amplifiers and bipolar single supply op amps.

3.6 TLC2272 single supply sensor interface

The increase in use of electronics in the automotive industry has brought about the need for single supply op amps, capable of operating from a +5V supply. The TLC2272 was designed for these applications, using a PMOS input stage gives the common-mode range down ground, while a push-pull CMOS output stage gives it an output swing includes both rails.

3.6.1 Knock sensor

This application below, utilises all these features: interfacing to a piezoelectric pressure sensor used to sense knocking in an internal combustion engine. The first op amp is in a non-inverting configuration, making use of its high input impedance and its common-mode range down to the negative rail.

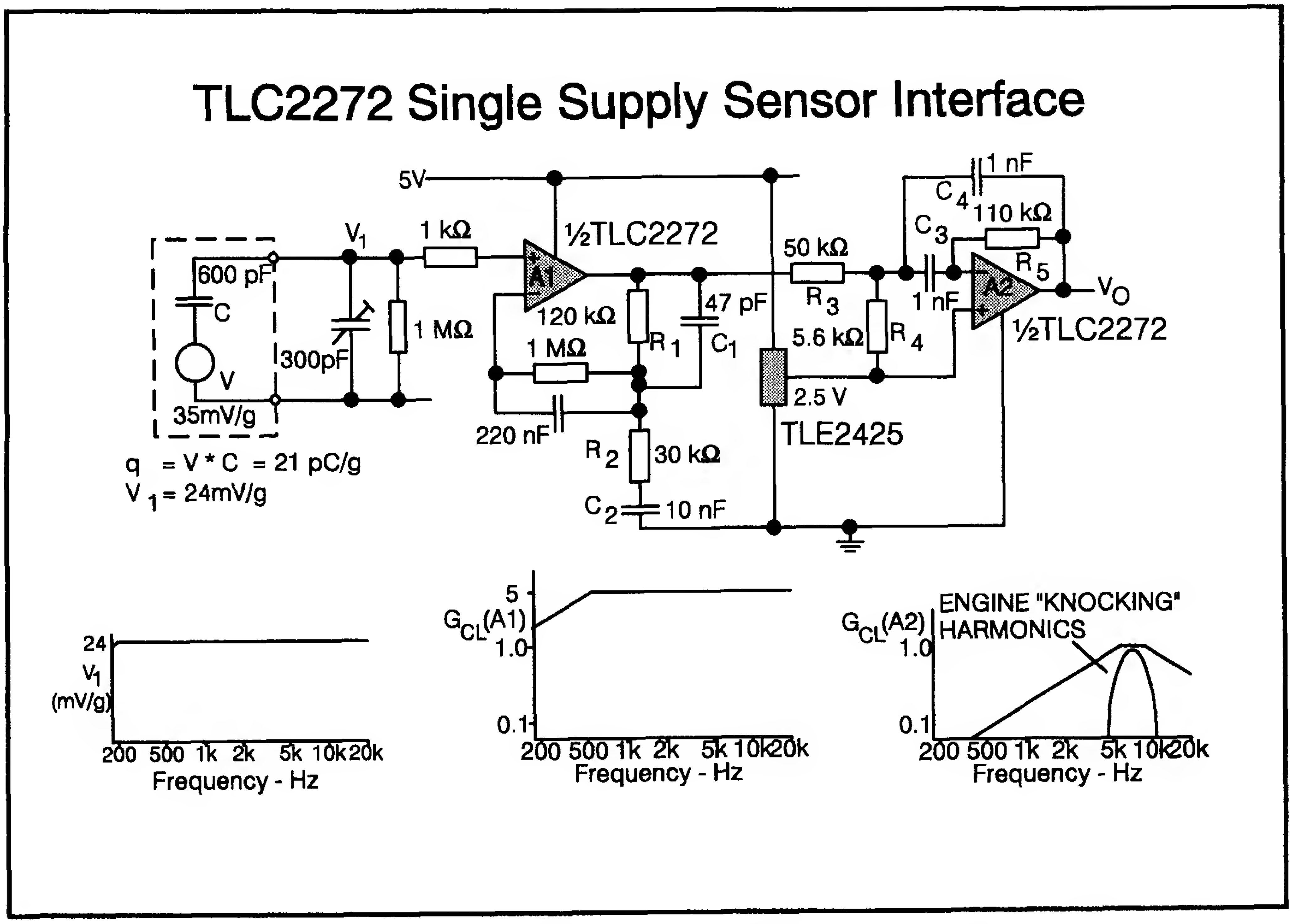

TLC2272 Single Supply Sensor Interface
5V
V1
1 kΩ
½TLC2272
A1
600 pF
C
V
300pF
35mV/g
1 MΩ
120 kΩ
1 MΩ
R1
47 pF
C1
220 nF
R2
30 kΩ
C2
10 nF
q = V * C = 21 pC/g
V1 = 24mV/g
50 kΩ
R3
5.6 kΩ
R4
2.5 V
TLE2425
1 nF
C4
C3
110 kΩ
R5
1 nF
A2
VO
½TLC2272
24
V1
(mV/g)
200 500 1k 2k 5k 10k 20k
Frequency - Hz
5
GCL(A1)
1.0
0.1
200 500 1k 2k 5k 10k 20k
Frequency - Hz
GCL(A2)
ENGINE "KNOCKING" HARMONICS
1.0
0.1
200 500 1k 2k 5k 10k 20k
Frequency - Hz

Figure 1.19 - TLC2272 single supply sensor interface

The piezoelectric sensor is an ac sensor and can be modelled by a voltage source in series with a capacitor. The sensor can be considered as working in two modes one as a sensors which produces charge or as a sensor which produces ac voltages. In this application the TLC2272 is amplifying the voltage produced by the sensor.

Interfacing to the sensor is a 1 MΩ resistor and a calibrating capacitor, this capacitor can be used to alter the high pass cut-off frequency of the sensor as well as affecting its gain. The shunt resistor is included to provide both a current path for any bias currents of the op amp and to provide a current path for any current flowing out of the sensor. In order not to load the sensor this shunt resistor needs to have a large resistance, and for this reason, the TLC2272 is ideal. No bipolar op amp has a high enough input impedance and more importantly, low enough bias currents to be able to interface with these resistors.

The first op amp acts as the sensor interface, and also doubles as a wideband filter amplifying the input signal plus filtering out signals which are not of interest.

The second op amp in the TLC2272 is connected in a Delyiannis-Friend configuration producing a band pass filter, which is used to filter out all other signals. It is configured in an inverting configuration, and in order maximum output swing it is important that its inputs are biased at around 2.5 V. In this application the 2.5 V reference operates as a ground. So for this reason the TLE2425 was chosen.

3.6.2 TLE2425

The TLE2425 contains an accurate low power 2.5 V reference that is buffered by a low power high output current capability op amp. This makes it ideal for 5 v supplied applications where either a low power reference is required, or a low impedance artificial ground is required. The TLE2425 requires only 170 µA of quiescent current while being capable of sourcing more than 20 mA of output current. No other integrated circuit can match this performance, and even discrete arrangements find it virtually impossible to meet the output current to quiescent current ratio, especially when the TLE2425 has been designed to drive capacitors of up to 100s of micro farads. No op amp can drive these orders or capacitors over this range without extensive compensation.

3.6.3 Delyiannis-Friend

The advantages of the Delyiannis-Friend circuit is that all the filter's key parameters can be designed and decided sequentially, simplifying the design process. The input resistors act as attenuators bringing the gain of this filter to unity. The centre frequency of the circuit is determined by the feedback resistor, R_5, and the Thevenin equivalent of the input attenuation resistors R_{TH}

$$\omega_o = \frac{1}{C * \sqrt{R_5 R_{TH}}}$$

and

$$R_{TH} = \frac{R3 * R4}{R3 + R4}$$

The quality factor Q, (a measure the reactance to resistance ratio at the natural frequency of the filter, roughly speaking it is a measure of how steep the initial roll-off is) of the filter depends solely on the ration of the feedback resistor to the Thevenin equivalent of the input resistors.

$$Q = \frac{1}{2}\sqrt{\frac{R5}{R_{TH}}}$$

When engine knock starts to occur, the sensor will generate a range of signals, whose frequency is not present when the engine is running properly, which the second op amp is used to exclusively amplify. The characteristic knock frequency of the engine will change depending on the size of the cylinders and the cylinder block's material. To meet all these changes in frequency, a wideband sensor and a versatile op amp are required; most of these sensors have bandwidths into the tens of kilohertz, meaning that one form of sensor should suit almost all applications. The TLC2272 with a unity gain bandwidth of 2 M/Hz and an input offset voltage of 950 µV provides the accuracy and speed required by the system, without using capacitive coupling.

The rail-rail output swing also increases the system's dynamic range by enabling the TLC2272 to drive A-D converters to their full input range. This is helped by the TLE2426 virtual ground, which enables the TLC2272 to drive symmetrical loads. This example typifies a usual LinCMOS op amp application requiring low bias currents and low quiescent currents whilst providing accurate signal conditioning.

3.7 TLC2262/4 low power rail-to-rail op amps

The TLC2262 and TLC2264 are the latest members of TI's family of rail-to-rail op amps. Just as the TLC2272/4 were improvements over the TLC272/4, the TLC2262/4 bring large improvements over the TLC27M2/4 devices.

TLC2262/4 Low Power Rail-Rail Op Amps

Lowest noise devices in their class

- Low supply current
  200 µA/op amp
- Rail-rail Output Swing
- Low Noise
  Vn = 12 nV/√Hz @ 25°C
  In = 2.8 fA/√Hz @ 25°C
- Low Input Offset Errors
  Vio = 950 µV @ 25°C
  Iib = 1 pA @ 25°C
- TSSOP, DIP and SOIC

Applications
5-V and ±5-V system ADC
Interface
Low power high impedance
transducer interface

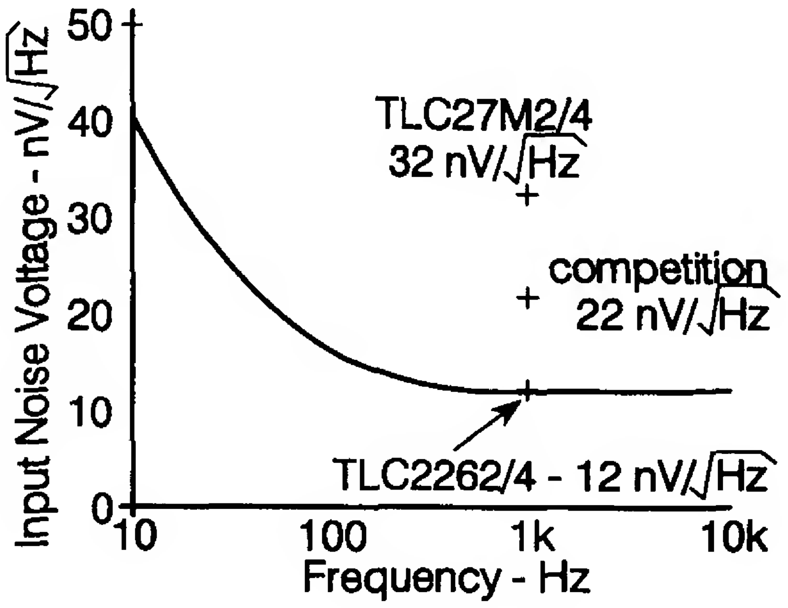


Figure 1.20 - TLC2262/4 low power rail-to-rail op amps

The TLC2272/4 provide very good performance at both 5-V and ±5-V supplies, increasing the available dynamic range, their supply current consumption limits their use in some portable/hand-held equipment.

The TLC2262/4 consumes about one fifth of the supply current of the TLC2272/4 without ruining their ac performance. Even at this lower supply current the TLC2262/4 offer sub-millivolt offset voltages (A-grade 950 µV) and noise voltages of only 12 nV/√Hz.

Their low noise voltages and low offset errors coupled with low power consumption make them ideal for portable/hand-held test equipment. The TLC2262 and TLC2264 are available in both the commercial and extended industrial temperature ranges in TSSOP. This package option makes them even better suited to meeting the needs of portable equipment.

3.8 TLC2264 battery power amplifier

The low power consumption of the TLC2262 and TLC2264 make them ideal for hand-held test equipment.

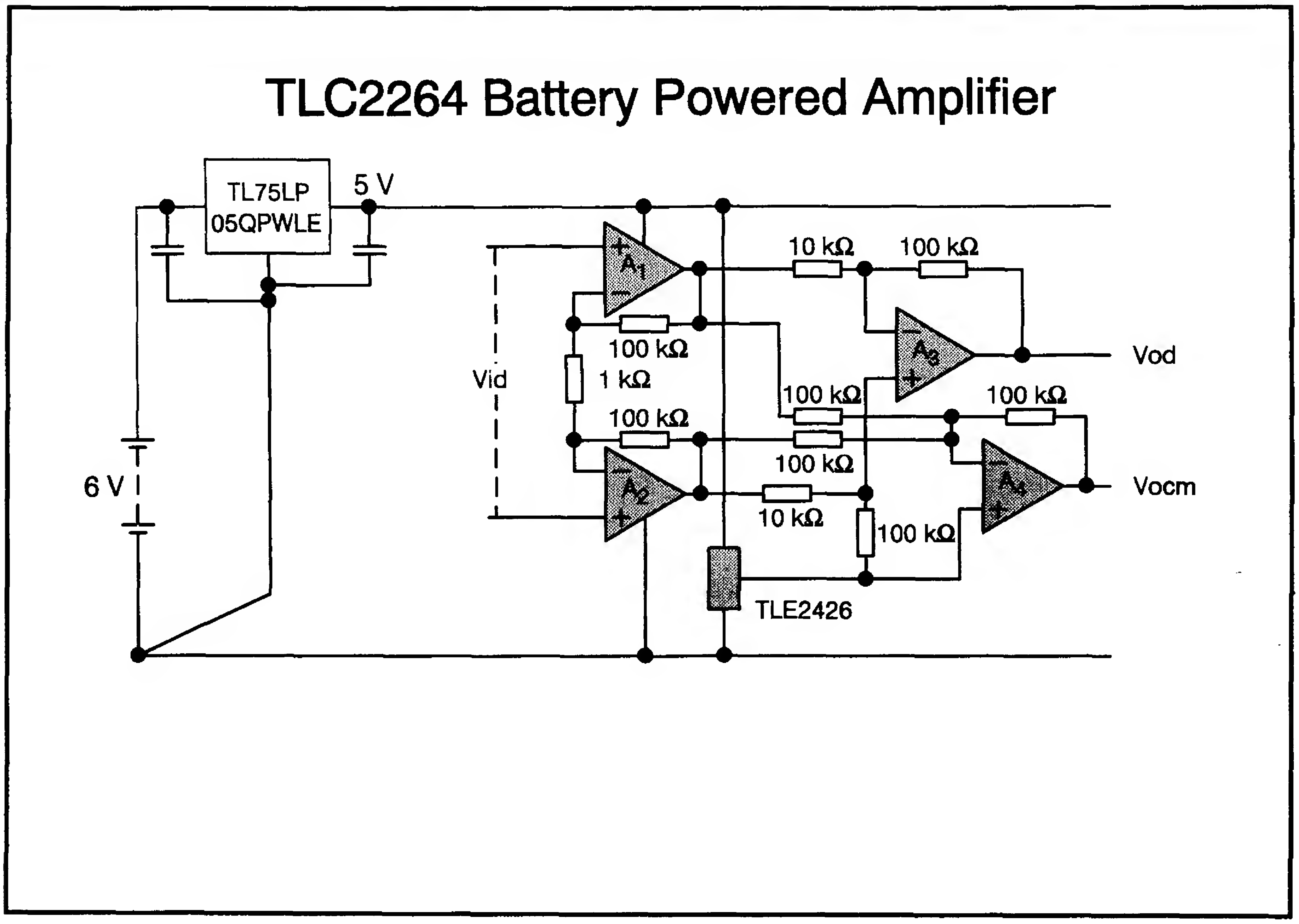


Figure 1.21 - TLC2264 battery powered amplifier

Figure 1.21 shows the TLC2264 configured as a three op amp instrumentation amplifier. This converts the differential input voltage to a single ended output voltage. The TLC2264 provides rail-to-rail output swing, which increases the dynamic range available to low power battery powered systems. The TLC27M4 has a typical output swing of about 4 V, the TLC2262 can sink and source current to within millivolts of both ground and the positive supply.

The fourth op amp is configured to add together the outputs from the first stage of the instrumentation amplifier, producing their common-mode voltage.

In order for the TLC2264 to amplify both positive and negative differential input signals the input of the third op amp must be referred to half of the supply voltage. this application uses the TLE2426 to produce a mid-rail ground.

3.8.1 TLE2426

The TLE2426 is very similar to the TLE2425 (discussed earlier) except that it contains a high impedance potential divider. This provides an "Analogue Ground" equal to half the voltage applied across its IN and COMMON terminals. This makes it particularly useful when trying to maximise the output swing of op amps whose outputs can sink and source current. The output of the TLE2426 will track the supply voltage, which makes it very useful for ratiometric applications; i.e. where the input is a ratio of the supply voltage.

4 3-V signal Conditioning

Not only is system design more difficult at these lower supplies, lower voltages also place extra demands on the IC designer.

In bipolar technology, one 'V_{be} will always be one V_{be}'. With a typical value of 0.7 V (even higher at lower temperatures), there is not much headroom to design complex functions. Most bipolar op amps share common design techniques to achieve certain characteristics, and reducing the supply voltage prohibits using these methods. For instance, the most common technique for implementing 'bias-current-cancellation' in an op amp simply will not operate from a 3-V supply. Similar problems occur in achieving low offset voltages without trimming, in attaining high gains and low noise figures and also in realising an output stage with high drive. IC designers need to so some work to achieve the same performance at 3 V as they do today at 5 V and above.

CMOS is a much better technology for low voltage operation. The MOSFET's V_T's can be 'tweaked' for optimal operation giving much more flexibility in the design. CMOS, however, has inherent trade-offs for Linear applications, and has a long way to go before it can achieve the noise and offset voltage of precision bipolar parts.

In areas other than op amps, there are some circuits that are more designable at lower voltages. Digital type circuits such as data conversion devices are already available at 3 V, and for DACs, lower supply voltages do not cause as big a problem. For higher than 12 bit resolution, more ADCs will be using Sigma-Delta techniques to meet the low voltage requirements of low frequency applications.

4.1 3-V signal conditioning products

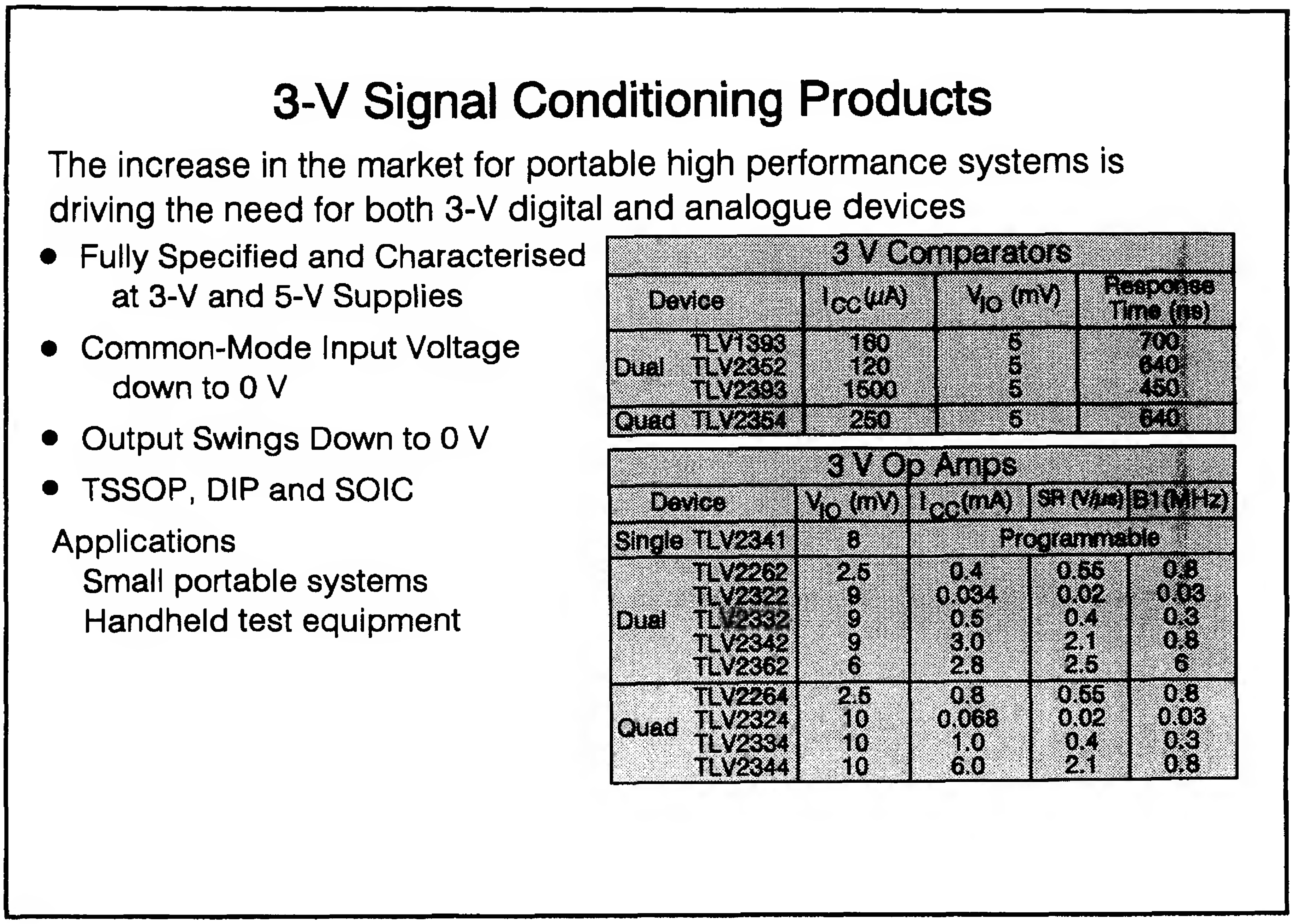
In 1983, to meet the growing need for low voltage operation op amps TI. introduced its TLC range of op amps. These devices are specified for 5 V and 10 V supply voltage operation. However as discussed above, with growth of portable equipment powered from batteries and to meet the needs of lower supply voltage logic there is now a need for op amps (and comparators) capable of operating from +3 V.

To meet this need, TI. has introduced its Texas Linear Low Voltage (TLV) range of LinCMOS op amps. These are devices specifically aimed for low voltage operation. It is for this reason that they have been characterised for operation at both 5 V and at 3 V. All members of the family are capable of operating from a minimum supply voltage of 2 V over the whole industrial temperature range of -40°C to +85°C, so increasing their versatility further.

As with all TI's LinCMOS op amps their common-mode input range extends down to the negative rail as do their outputs.

More recent additions to TI's family of 3-V devices include a high speed audio op amp and two new comparators, which use a new low voltage bipolar process. This process has been specially developed for 3-V applications, and enables all three devices to operate from a minimum supply voltage of 2 V over the whole of the industrial (-40°C to +85°C) temperature range.

The latest additions to 3-V family are the TLV2262 and TLV2264; offering rail-to-rail output swing with very low power consumption at 3 V.



3-V Signal Conditioning Products

The increase in the market for portable high performance systems is driving the need for both 3-V digital and analogue devices

- Fully Specified and Characterised at 3-V and 5-V Supplies
- Common-Mode Input Voltage down to 0 V
- Output Swings Down to 0 V
- TSSOP, DIP and SOIC

Applications
Small portable systems
Handheld test equipment

3 V Comparators				
Device		I_{CC} (µA)	V_{IO} (mV)	Response Time (ns)
Dual	TLV1393	160	5	700
	TLV2352	120	5	640
	TLV2393	1500	5	450
Quad	TLV2354	250	5	640

3 V Op Amps					
Device		V_{IO} (mV)	I_{CC} (mA)	SR (V/µs)	B1 (MHz)
Single	TLV2341	8	Programmable		
Dual	TLV2262	2.5	0.4	0.55	0.8
	TLV2322	9	0.034	0.02	0.03
	TLV2332	9	0.5	0.4	0.3
	TLV2342	9	3.0	2.1	0.8
	TLV2362	6	2.8	2.5	6
Quad	TLV2264	2.5	0.8	0.55	0.8
	TLV2324	10	0.068	0.02	0.03
	TLV2334	10	1.0	0.4	0.3
	TLV2344	10	6.0	2.1	0.8

Figure 1.22 - 3-V signal conditioning products

Figure 1.22 contains a table listing some of the capabilities of TI's 3-V devices. LinCMOS op amps, as usual, offer a good speed-power compromise over the entire product range, from the micro-power devices to the higher speed devices; while the bipolar device offer very good speed from 3 V.

The versatility of these devices is expanded yet further by the choice of 3 plastic packages. In addition to being available in the standard dual-in-line and standard small outline package all members are available in the new Thin Shrink Small Outline Package (TSSOP), as was discussed earlier. The TSSOP is attracting wide interest due to its extremely large savings in terms of board space area and its very small height, a maximum of just 1.1 mm. This makes the devices even better suited to portable systems.

4.2 TLV2262/4 low power rail-to-rail op amps

The TLV2262 and TLV2264 dual and quad low power op amps are the latest additions to TI's range of 3-V signal conditioning devices. Both devices are manufactured using the Advanced LinCMOS technology, which enables them to provide very high performance off of only 200 µA/channel from a 3-V supply.

TLV2262/4 Low Power Rail-Rail Op Amps

Lowest noise devices in their class

- Low supply current
  200 µA/op amp
- Rail-rail Output Swing at 3 V.
- Low Noise
  Vn = 12 nV/$\sqrt{\text{Hz}}$ @ 25°C
  In = 2.8 fA/$\sqrt{\text{Hz}}$ @ 25°C
- Low Input Offset Errors
  Vio = 950 µV @ 25°C
  Iib = 1 pA @ 25°C
- TSSOP, DIP and SOIC

Applications
  3-V system ADC Interface
  Low power high impedance
    transducer interface

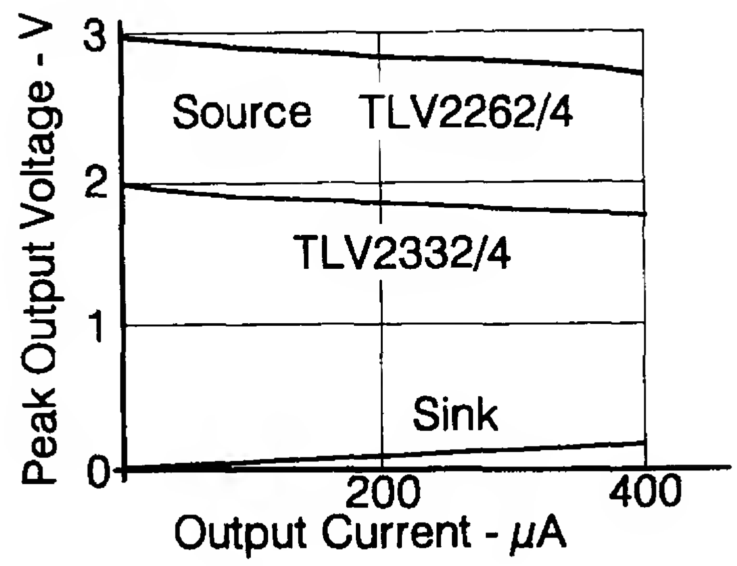


Figure 1.23 - TLV2262/4 low power rail-to-rail op amps

The greatest differentiator between the new op amps and the original members of the 3-V family is their rail-to-rail output swing. As stated earlier as the supply voltage is lowered then the errors/limitations of the op amp become more important.

A 1 V shortfall in the output swing of an op amp operating from 5 V is equivalent to a 20% reduction in the available dynamic range, at 3 V it is equivalent to a 33% reduction in the available dynamic range (this is excluding the larger relative effect of the input errors). The curves in figure 1.23 clearly shows its TLV2262/4 improvement in output swing over a standard 3-V op amp.

A Rail-to-rail output swing from the op amp becomes essential when interfacing to 3-V ADCs.

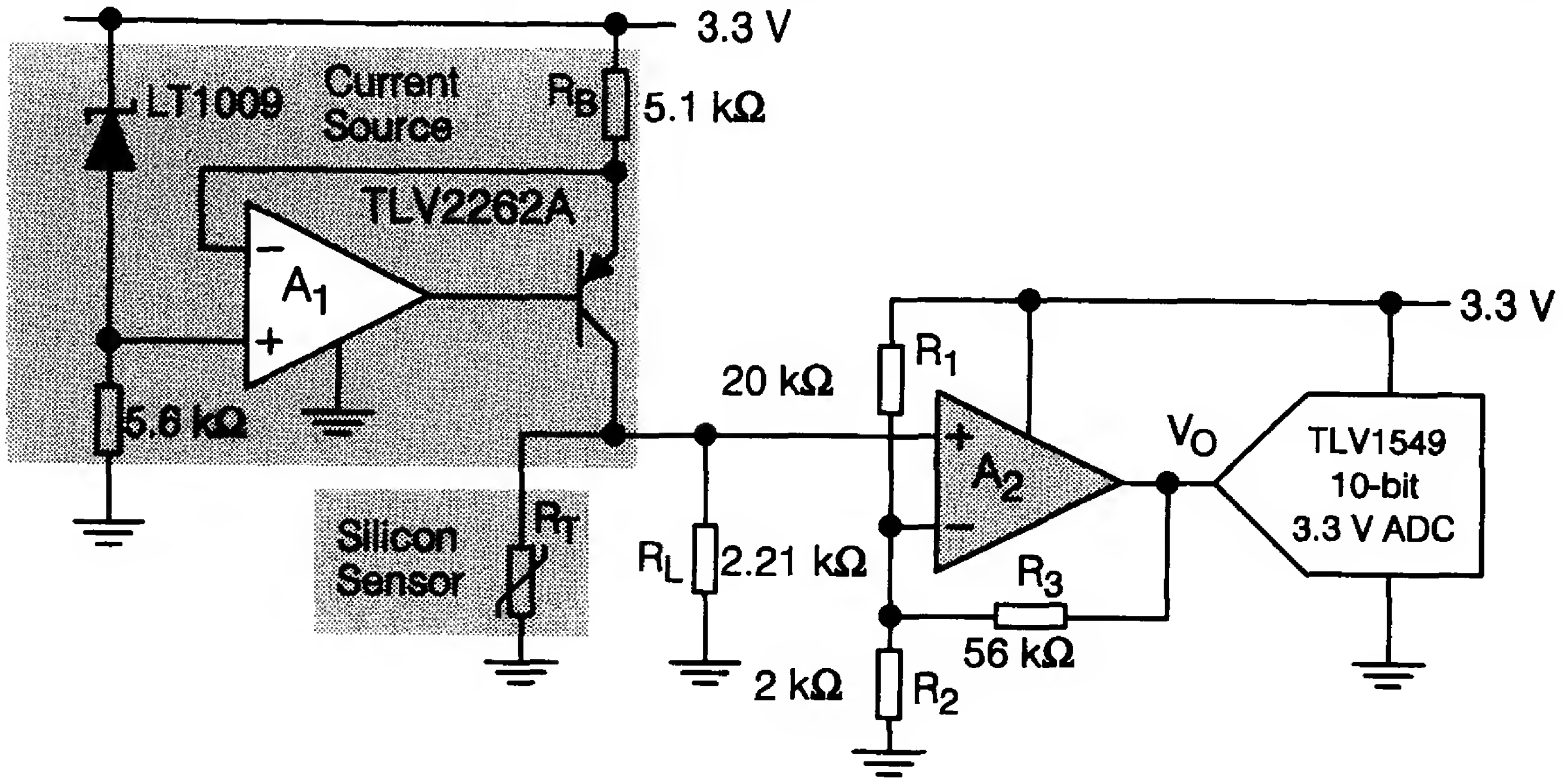
The low power consumption and rail-to-rail output swing makes these devices ideal for almost all portable applications.

The low power consumption of the TLV2262/4 doesn't destroy their ac performance; both devices have typical noise voltages and currents of only 12 nV/$\sqrt{\text{Hz}}$ and 2.8 fA/$\sqrt{\text{Hz}}$ - which is lower than most op amps can achieve at 3 to 5 mA off of a ±15-V supply!

As with all TI's 3-V devices, the TLV2262/4 are available in PDIP, SOIC and TSSOP. The TSSOP in conjunction with the low power and rail-to-rail output swing makes them well suited to portable applications.

4.3 3.3-V low power temperature sensor amplifier

3.3-V Low Power Temperature Sensor Amplifier



$$V_O = \frac{2.5}{R_B} \times \frac{R_L R_T}{R_L + R_T} \times \frac{R_1R_2 + R_1R_3 + R_2R_3}{R_1R_2} - 3.3\text{ V} \times \frac{R_3}{R_1}$$

V_O = 0.03 V to 3.0 V

Figure 1.24 - 3.3-V low power temperature sensor amplifier

4.3.1 Silicon sensor

Most temperature sensors are not linear, and therefore require some form of linearisation. This linearisation can be done via the biasing of the sensor, or via some post signal conditioning linearising.

The sensor used is made out of silicon and has a non-linear resistance versus temperature characteristic. One way of linearising its characteristic is to bias it with a constant current while placing a linearisation resistor in parallel with it. The value of linearisation resistor is determined by the temperature range over which the device will measure.

The value of the linearisation resistor, R_L, can be determined from the following equation:-

$$R_L = \frac{R_M*(R_4+R_5)-2*R_4*R_5}{R_4+R_5-2*R_M}$$

Where R_4 = Sensor resistance at minimum temperature point
R_5 = Sensor resistance at maximum temperature point
R_M = Sensor resistance value at the midpoint of temperature range

For an operating temperature range of 0°C to 50°C, the values for R_1, R_2, and R_M are:-

$$R_4 = 813.5\,\Omega$$
$$R_5 = 1211\,\Omega$$
$$R_M = 1000\,\Omega$$
$$R_L = 2210\,\Omega$$

4.3.2 Current source

Op amp A_1 is used with the LT1009 and a PNP transistor to set up a current source. The current sourced will nominally be equal to:-

$$\begin{aligned} I_S &= \frac{V_{REF}}{R_B} \\ &= \frac{2.5}{5.1}\ \text{mA} \\ &= 490\ \mu\text{A} \end{aligned}$$

4.3.3 TLV2262

To maximise the output swing at the output the gain of op amp A_2 should be set that at the maximum temperature measured the output of A_2 should be at around 3.1 V, and at the minimum temperature measured the output of A_2 should be close to 0.1 V.

In order to achieve this output swing extra biasing must be placed about the inverting input of A_2. The voltage appearing at the non-inverting input of A_2, is equal to:-

$$V_+ = \frac{2.5}{R_B}\frac{R_L R_T}{R_L + R_T}$$

At 25°C the parallel combination of R_L and R_T is equal to 688.5 Ω, producing a voltage at the non-inverting input of A_2 of 0.337 V. For symmetrical output swing the output voltage of A_2 should be approximately 1.6 V.

The output of A_2, V_O, equals:-

$$V_O = \left(\frac{R_1R_2 + R_1R_3 + R_2R_3}{R_1R_2}\right)V_+ - 3.3\frac{R_3}{R_1}$$

Implies
$$\frac{V_+}{R_2} = \frac{3.3 - V_+}{R_1} + \frac{V_O - V_+}{R_3}$$

Yielding
$$\frac{0.337}{R_2} = \frac{2.96}{R_1} + \frac{1.26}{R_3}$$

Repeating the same equations for the minimum temperature and maximum temperature yields:-

T_{min}
$$\frac{0.291}{R_2} = \frac{3.01}{R_1} - \frac{0.191}{R_3}$$

T_{max}
$$\frac{0.383}{R_2} = \frac{2.92}{R_1} + \frac{2.72}{R_3}$$

Solving these three equations to get values for R_1, R_2 and R_3 and using E24 values yields:-

$$R_1 = 20\ \text{k}\Omega$$

R_2 = 2 kΩ

R_3 = 56 kΩ

These nominal resistor values yields a minimum output voltage at 0°C of 30 mV, while at 50°C the output voltage would be 2.96 V.

The TLV2262 provides good accuracy whilst maintaining an overall low power consumption, and even when working off a single 3-V rail the offset voltage of the TLV2262A is still below 1 mV.

This example has used E24 value resistors, as these values are readily available in surface mount packaging. This can provide great board space savings, as can the use of TSSOP packaging. The TLV2262AIPWLE is available as a standard option, while the LT1009 is available as standard in SOIC and could even be made available in the minute PK package. The use of all these space and thickness saving packages fit nicely together in today's growing market in hand-held test equipment.

Greater accuracy will be attained by using E96 resistor values, these however are not available as standard in surface mount packaged resistors.

The accuracy of the system will still be affected by changes in the supply voltage. One way of overcoming this would be to linearise the silicon sensor via a series resistor. The output of the sensor would therefore now depend on the supply voltage; allowing a ratiometric conversion. This would allow the output of the op amp to track the supply voltage removing the dangers of saturating the output of the TLV2262.

4.4 TLV2362 high speed 3-V dual op amp

As the supply voltages of most devices decrease, their ac and dc performance also decrease. This for a long time created problems when moving from ±15 V to +5 V supplies. The move to 3 V or 3.3 V is creating yet more problems, with further reductions in output swing, input errors and speed.

Traditional bipolar processes are proving to be unsatisfactory for the new low voltage systems. To meet these needs TI developed a new low voltage bipolar process. This process uses smaller geometry devices, which results in smaller parasitic elements in the structure and so enables devices using this process to achieve much higher speeds than their higher voltage counterparts.

On the negative side their maximum supply voltage range has been decreased from 36 V to 7 V, but for 3-V systems this is not a limiting factor.

The TLV2362 has been designed specifically for 3-V (±1.5 V) audio applications. 3-V audio applications have the same requirements as standard audio applications, but has even tighter constraints placed on to the op amps used.

Audio applications require low noise, low distortion and high speed. The TLV2362 excels in these areas with its 9 $nV/\sqrt{Hz}$ noise voltage and distortion figures of only 0.0007% and a unity-gain bandwidth of 6 MHz.

As with all of TI's 3-V products the TLV2362 has been characterised over the industrial temperature range (-20°C to 85°C) at both 3 V and 5 V. Most applications using the TLV2362 will be 3-V portable applications and to meet the tight PCB area and overall system size constraints the TLV2362 is available in the Thin Shrink Small Outline Package as well PDIP and SOIC.

TLV2362 High Speed 3-V Dual Op Amp

High Speed and Low Noise at 3 V!

- Fully characterised at 3-V and 5-V supplies.
- Wide unity-gain bandwidth
  6 MHz @ 3 V
- Low Noise
  9 nV/$\sqrt{\text{Hz}}$
- TSSOP, DIP and SOIC

Applications

Portable Hi-Fi

Cellular Phones

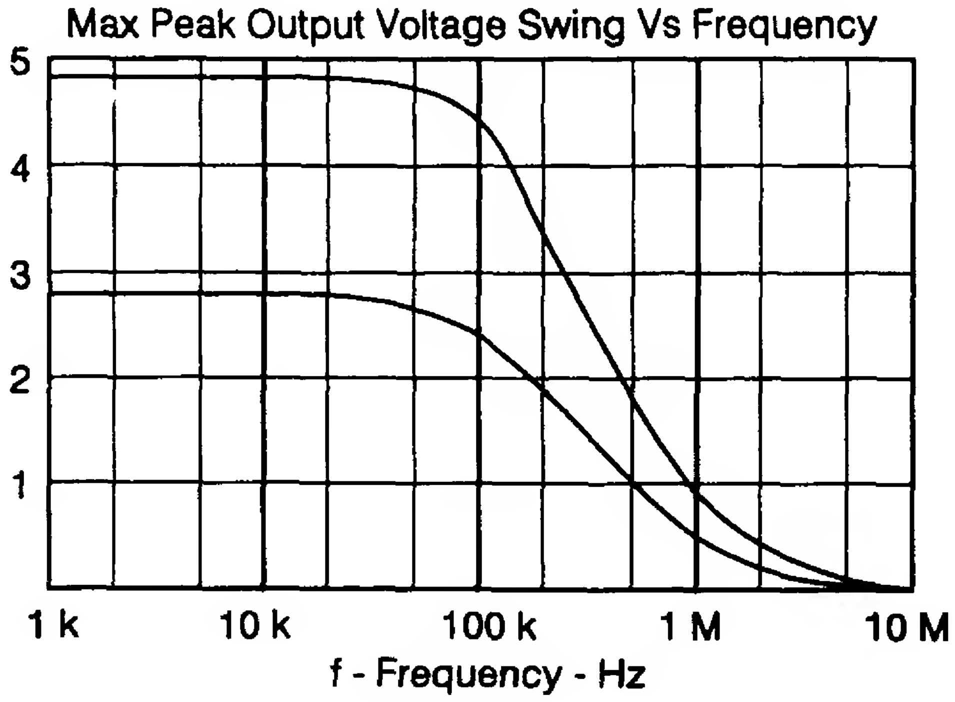


Figure 1.25 - TLV2362 high speed 3-V dual op amp

4.5 3-V portable audio amplifier

As stated earlier the low noise voltage (9 nV/$\sqrt{\text{Hz}}$), wide bandwidth (6 MHz) and low distortion (0.0007%) make the TLV2362 ideal for 3-V audio applications. One area where immediate impact has been seen is in personal stereos; compact cassettes, compact discs and even mini-disc.

In personal stereo CDs, 16-bit DACs are being used, which require the best performance from the op amps used. The TLV2362 has proved to be up to these demands.

3-V Portable Audio Amplifier

3-V 16-bit resolution audio amplifier

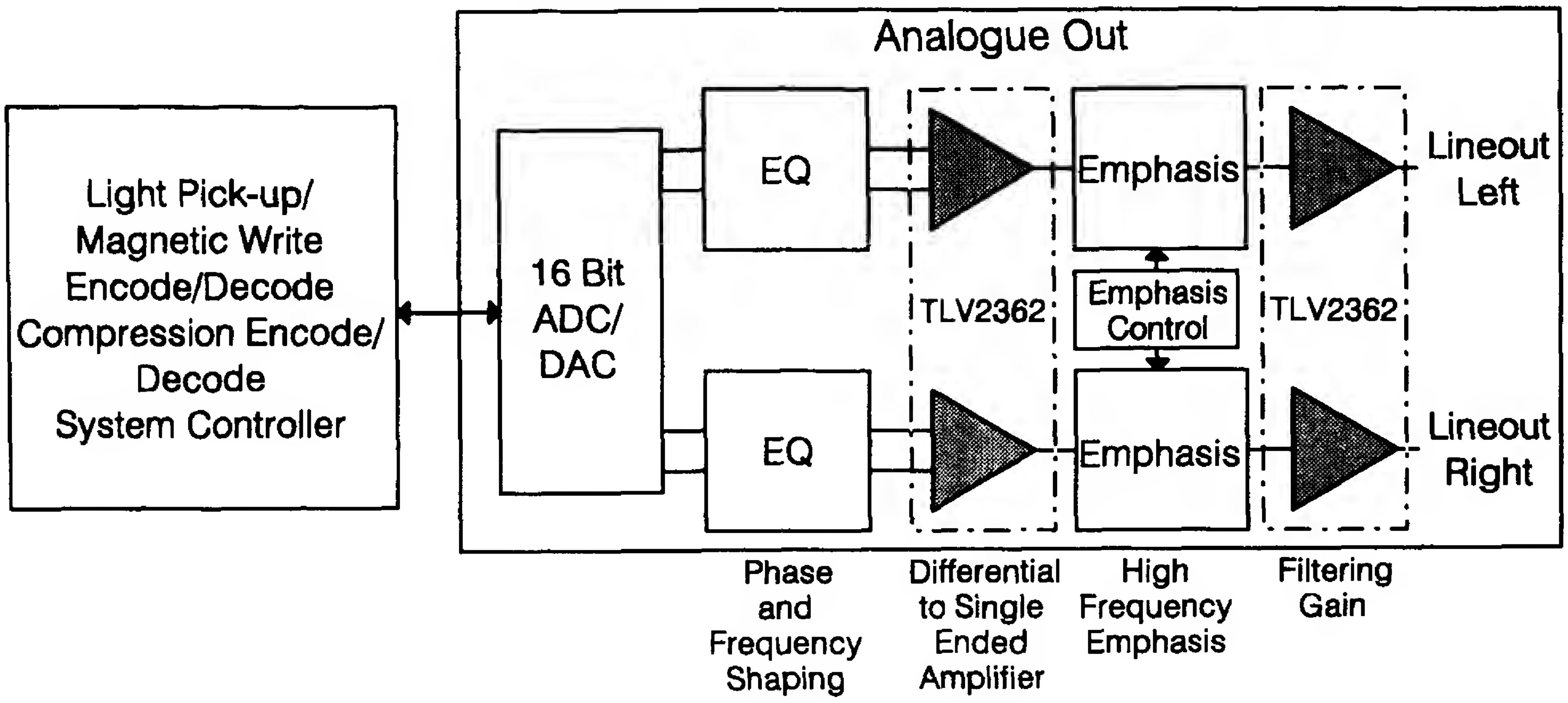

Analogue Out
Light Pick-up/
Magnetic Write
Encode/Decode
Compression Encode/
Decode
System Controller
16 Bit
ADC/
DAC
EQ
EQ
TLV2362
Emphasis
Emphasis
Control
Emphasis
TLV2362
Lineout
Left
Lineout
Right
Phase
and
Frequency
Shaping
Differential
to Single
Ended
Amplifier
High
Frequency
Emphasis
Filtering
Gain

Figure 1.26 - 3-V portable audio amplifier

The output from the DACs is normally differential, and so the first amplifiers after the DAC have to convert the differential signal in to a single ended signal. They will also be used to filter the output of the DAC as well as doing some waveform shaping. The second stage is used to provide further filtering and waveform shaping. Emphasis modification may also need to be done. This quite often entails reducing the high frequency signals which may have been emphasised during recording to avoid the bass signals swamping out all other frequencies.

The 16-bit DAC has a maximum signal to noise ratio of approximately 96 dB, which at 3 V equates to 1 LSB being approximately 45 µV. The TLV2362 in a real application has shown that it is able to meet these very severe demands.

Personal CDs are becoming smaller, and so every component can be critical, and so a further advantage of the TLV2362 in these applications is TSSOP. The 8-pin TSSOP uses 50% less PCB area than an 8-pin SOIC and is only 1.1 mm (maximum) thick which provides even greater savings in the system's outside thickness and area.

4.6 3-V micro-power sensor interface

One of the major application areas for 3-V op amps will be in the handheld or remotely powered sensor/metering areas. In these applications battery lifetime will be of prime consideration.

The application shown in figure 1.27 shows the TLV2324 amplifying the output voltage of a temperature sensor and a pressure sensor. This could be used in a an application where the volume of gas would want to be measured.

The output of the op amps is then fed to the TSS400/4 , Texas Instruments Sensor Signal Processor. The TSS400 contains its own CPU and 4 multiplexed analogue inputs which feeds to an on-chip 12-bit ADC.

The ADC of the TSS400 makes ratiometric conversions based on its output voltage SV_{DD}. By turning on SV_{DD} only when measurements are to be taken the overall power consumption of the whole system can be significantly reduced.

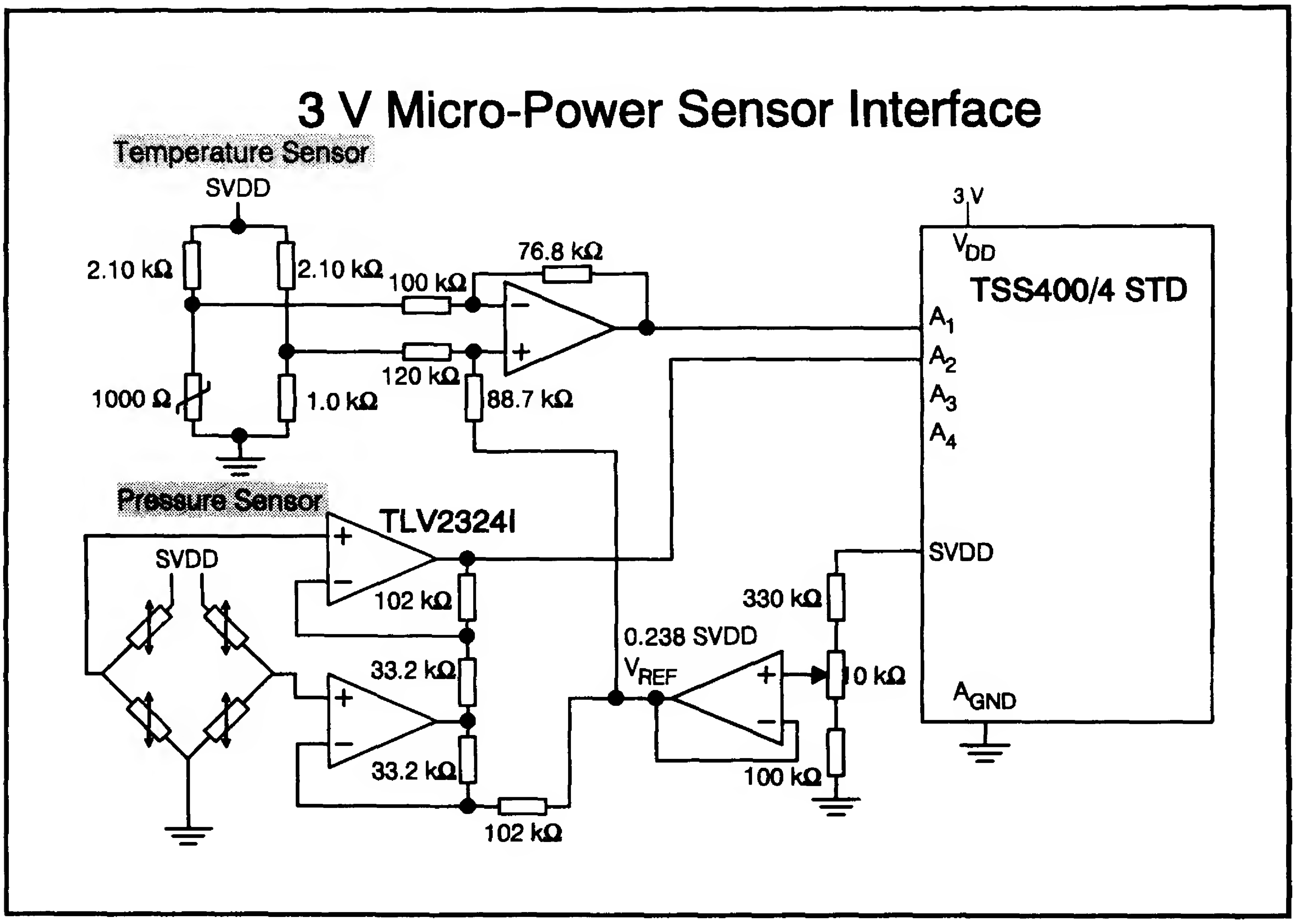

3 V Micro-Power Sensor Interface
Temperature Sensor
SVDD
2.10 kΩ
2.10 kΩ
100 kΩ
76.8 kΩ
120 kΩ
1000 Ω
1.0 kΩ
88.7 kΩ
Pressure Sensor
TLV2324I
SVDD
102 kΩ
33.2 kΩ
33.2 kΩ
102 kΩ
0.238 SVDD
VREF
330 kΩ
10 kΩ
100 kΩ
3 V
VDD
TSS400/4 STD
A1
A2
A3
A4
SVDD
AGND

Figure 1.27 - 3-V micro-power sensor interface

The first op amp is used to act a reference buffer, which buffers a proportion of SVDD. This is used to set the minimum input voltage of the analogue inputs to the TSS400's ADC. Which in this case is equal to $0.2380 * SV_{DD}$.

The second and third op amps are used to amplify the output of the pressure sensor, which is powered by SV_{DD}. This results in the output of the pressure sensor being relative to SV_{DD}, so that any variance in SV_{DD} will be cancelled out by the ADC.

The gain of the two op amp differential amplifier configuration is set to give a maximum output voltage of $0.4008 \times SV_{DD}$. This is equal to the maximum input range of the TSS400's ADC.

The fourth op amp is configured as single stage differential amplifier, the high input impedance and low input bias currents enable the TLV2324 to use large feedback and source resistor without increasing the offset voltage of the op amp while minimising the loading on the temperature sensor bridge.

The sensor bridge uses a 2.1 kΩ biasing resistor to cancel out the exponential temperature-resistance characteristics of the silicon sensor. This gives the output of the fourth op amp a near linear output voltage versus temperature characteristic.

Once again the resistor values and the reference voltage has been used to set the voltage range of the fourth op amp to the ADC's input range.

The ideal gas law relates the volume, pressure and temperature of a gas as:-

$$\text{Constant} = \frac{nPV}{T} \text{ .... Where n is a constant relating to the gas.}$$

This can be a more accurate way of measuring the amount of gas consumed in domestic applications than just measuring the volume.

5 High temperature op amps

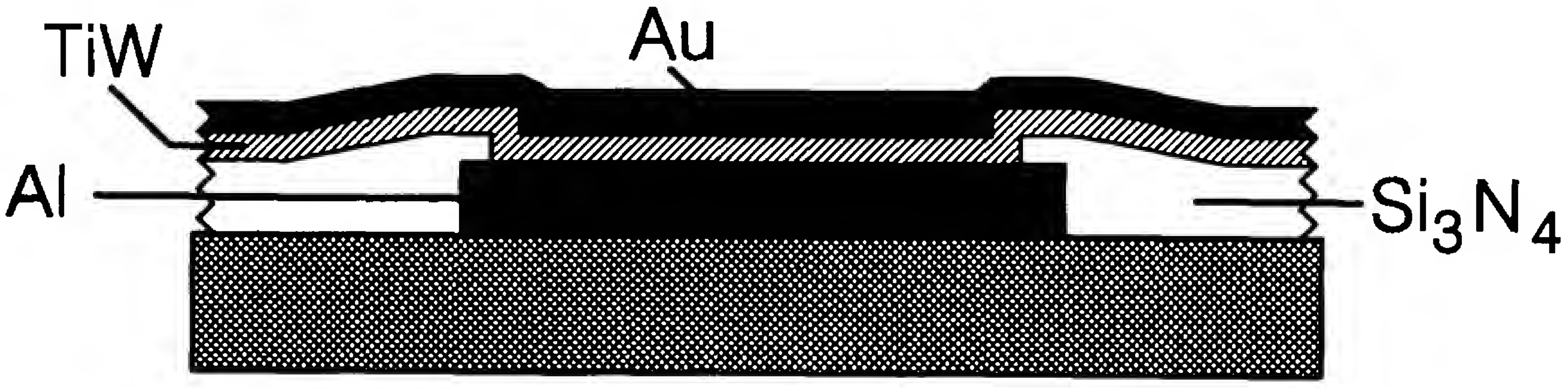
5.1 High temperature op amps

In a number of engineering sectors, signal conditioning circuits are now frequently mounted directly by the transducer. This can bring tremendous improvements in the quality of the signal fed to the system processor (digital and analogue). This can subject the signal conditioner to the extremes in temperature, stress and pressures. The largest problem, to which op amps are subjected, is elevated ambient temperature operation.

In automotive applications, there is direct cylinder block mounting, while industrial applications may require the op amps to be mounted on the vessel containing the process. In the past, this would have involved using expensive hybrid devices in ceramic packages.

High Temperature Op Amps

Cross Section of Bond Pad



150 °C Ambient Temperature Operation in Plastic Packages

Fully Specified and Guaranteed Parametric Operation

Increased Reliability of Bond Pads at High Temperatures

Die Sealed From Ingression of Moisture

Figure 1.28 - High temperature op amps

Plastic packages have generally limited reliability when subjected to high temperatures for great periods of time. This has been due to several factors of the package and bonding.

this section discusses how TI has dealt with this, to offer high reliability high temperature plastic devices.

5.1.1 Integrated Circuit Process

An integrated circuit will normally have all the silicon covered with Silicon Nitride. This has two main functions, one is to protect the surface from external effects, while the other is to protect the die from moisture ingression. There must, however, be holes in the silicon nitride to enable the bond wire to connect the silicon to the outside world. These holes in the silicon nitride can now let moisture into the silicon.

Plastic packages will normally let much more moisture into the integrated circuit than ceramic packages. This has led to plastic packages being rarely used in harsh environments. TI's high temperature process now enables hermetically sealed devices to be produced in a plastic package.

5.1.2 High Temperature Process

The bond wire material used plastic packages is normally Gold, which is bonded to Aluminium pads on the silicon die. At high operating temperatures the bond between the Aluminium pad and the Gold wire can degrade.

The process used for high ambient operating temperature devices involves depositing and patterning Titanium-Tungsten and Gold layers over the bond pad areas. The Titanium-Tungsten layer provides good adhesion to the Aluminium pads and Silicon Nitride overcoat. The Titanium-Tungsten layer also acts as a barrier between the Aluminium and Gold layers, this results in the Gold wire bonds being made to a Gold layer rather than an Aluminium layer. This eliminates the inter-metallic and voiding problems at high ambient operating temperatures.

With the development of this process Texas Instruments has now released the TL2828, TL2829, TLC2801 and TLC2872 devices whose performance is fully specified for operating in ambient temperature ranges up to 150°C.

5.1.3 High Temp Process Qualification

Any new product (and process) must go through a qualification process. This is to make sure that the device is reliably manufacturable. Due to the very harsh nature of the environment in which these products are to be used, and that it is a new process, the qualification procedure for the first op amp, TL2829, was very thorough - far in excess of any other linear design.

The table below shows the qualification performed on the TL2829 op amp.

TEST	CONDITIONS
Steady State Life	155°C for 5000 hours with bias.
Autoclave	121°C for 2000 hours without bias at 15 psi and 100% humidity.
Temperature Cycle	-65°C to 150°C for 5000 cycles.
Storage	170°C for 3000 hours.

Throughout all these extended tests, no failures occurred, which is impressive for any product, and highlights the outstanding reliability of Texas Instruments' high temperature op amps.

5.2 High temperature op amps

There are 5 members to TI's high temperature range of devices. 1 single 3 duals and 1 quad. All 5 devices have been characterised and are specified for operation over the new 'Z' temperature range which extends from -40°C to 150°C. The 150°C maximum ambient temperature exceeds that of the military temperature range by 25°C.

150°C High Temperature Op Amps

150°C Ambient Temperature Range Op Amps in Plastic Packages

- Wide ambient temperature range
  -40°C to 150°C
  25°C greater than military
- Low input offset voltages
  10 mV(max) at 150°C - TL2828/9
  1.5 mV(max) at 150°C - TLC2801
  3 mV(max) at 150°C - TLC2872
- Rail-rail output swing - TLC2801/2872

Applications

Automotive

Industrial high temperature apps

Geophysical drilling

	Device	Vio(max)	lib(max)	Icc(max)
Single	TLC2801	1.5 mV	30 nA	1.5 mA
Dual	TL2828	10 mV	-500 nA	1.2 mA
Dual	TLC2872	3 mV	5 nA	3 mA
Quad	TL2829	10 mV	-500 nA	1.2 mA

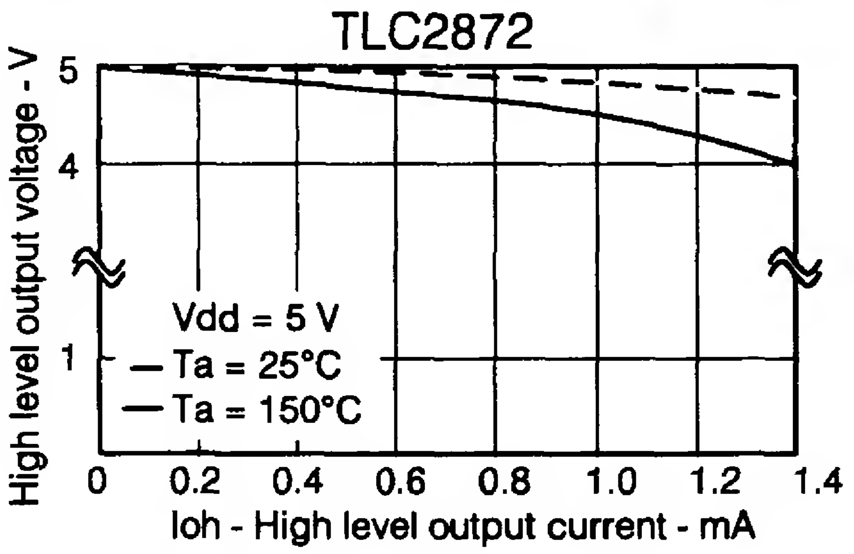


Figure 1.29 - 150°C high temperature op amps

5.2.1 TL2828 and TL2829

The TL2828 and TL2829 were the first in a series of very high temperature op amps from Texas Instruments. Both devices are single supply op amps capable of operating from a 4 V supply up to a maximum of 30 V. The supply current of the TL2829 is only 1.2 mA at a 5 V supply over a whole temperature range for all four op amps.

The density of op amps and low quiescent power, adds to its capabilities of functioning at very high ambient temperatures.

5.2.2 TLC2801

The TLC2801 was the third High temperature op amp to be released by TI. It combines the 150°C operating temperature range with very low offset voltages. The guaranteed maximum is just 1.5 mV even at 150°C.

This gives it an offset error of just under 12 bits!, and is provided from a single 5 V supply. Added to this its large open loop gain. The gain of the device still remains greater than 50,000 even at 150°C. This is greater than a lot of op amps can provide even at 25°C.

The low offset voltage and high are just two factors which make this device ideal for high temperature applications. The low bias currents allow the TLC2801 to directly interface to high impedance sensors. When this is coupled to the high ambient temperature range of the op amp, it makes the TLC2801 just about the only op amp capable of being directly mounted at the sensor output and still provide high accuracy reliable data.

5.2.3 TLC2872

The TLC2872 is the fourth member of the TI high temperature range of op amps. It combines the 150°C capabilities of the process with a dual op amp with rail-rail outputs. This enables the device to maximise the dynamic range by allowing its outputs to swing to within milli-volts of both supply rails.

This allows the device to be mounted at the sensor output, enabling the signal conditioning to be completed there. This means that signal to noise ratio should be increased. In the past the output of the transducer would have to be fed to the signal conditioning section via noisy lines that are susceptible to interference from motors and other sources. By doing the signal conditioning at the sensor output, its output will raised above the noise floor, reducing the impact of the switching noise.

Added to the rail-rail performance at 150°C is the large stability in offset voltage. The TLC2872 offers a maximum offset voltage of 3 mV at 150°C, while the bias currents have risen to only 3 nA. In addition to the very low input errors, the TLC2872 still offers a very high open loop gain, greater than 10,000; even at 150°C.

5.2.4 TLC2810

The latest addition to TI's high temperature op amps is the TLC2810. The TLC2810 combines the high impedance of all LinCMOS op amps with 150°C operation. This enables it to be used in applications where even LinCMOS op amps have been excluded.

5.3 High temperature op amps use

The 150°C ambient temperature range of these op amps allow them to be used in areas where they could never be used before.

Some typical applications are listed below:

Aerospace	Sensors/Instruments	High temperature environments
Automotive	Sensors	Sensors with direct contact to engine blocks, transmission, brakes or exhaust system
Industrial controls	System controls sensor/interface	High temperature process control, sensor interface
Instrumentation	Remote instruments	Down-hole oil well exploration

6 Intelligent opto sensors

6.1 Introduction

An important application for signal conditioning, is to amplify sensor signals from the outside 'real' world; and to generate appropriate signals for conversion to digital processing. In this section we consider techniques of measuring light and delivering these analogue measurements into the digital domain.

The simplest real-time measurement of light level is the simple photo-diode. In a photo-diode, incident radiation is absorbed by the silicon, to generate hole-electron pairs. These in turn give a photo-current across a reverse-biased p-n junction.

For a photo-diode current-mode sensor, the current is proportional to the light intensity.

Photo-diodes may be modified into photo-transistor elements or be used with appropriate op amps and then with data conversion elements to deliver a measurement of light level to a digital control circuit. In this section we shall examine structures which combine light sensing, signal conditioning and data conversion in integrated structures. Such devices will offer convenience of use at modest cost.

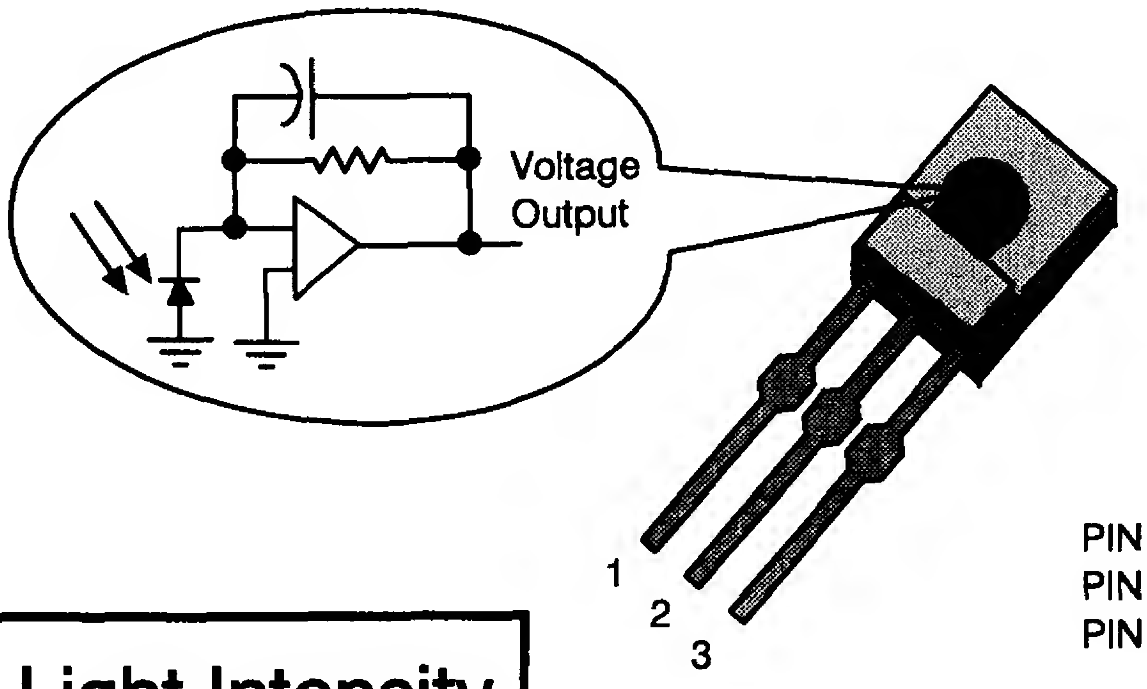
The Texas Instruments' LinCMOS(TM) process, used extensively for low input-offset operational amplifiers, can be easily adapted by the addition of light shields to make integrated photo-sensor structures. A photo-diode made by this process is responsive from 400 nm to 1100 nm (visible and short infra-red) when encapsulated in transparent plastic. The TSL250 and TSL230 integrated light sensors respond over this entire spectral range. However, by modified encapsulation a more restricted response (visible only, or infra-red only) can be achieved. An example of such a device is the TSL260.

6.2 Light-to-voltage sensors TSL250/TSL260

6.2.1 Overview

In this section, we shall describe how a current mode sensor is combined on a chip with relatively simple signal conditioning elements, to make a useful device. We shall consider the example of the TSL250 first. The TSL250 light-to-voltage converter solves some basic application needs. It is particularly suitable for analogue measurement of low light levels in an electrically noisy environment.

TSL250/TSL260 Light to Voltage Sensor



PIN 1 GND
PIN 2 Vdd
PIN 3 V_o

V_o α Light Intensity

Figure 1.30 - TSL250/260 light-to-voltage sensors

In the TSL250, a large area photo-diode is combined with a trans-impedance amplifier, so the photo-diode current output is converted to an output voltage.

Three versions of the device are produced, with different photo-diode areas, and internal feedback resistor values.

6.2.2 Sensitivity Variants

TSL250 gives 2V output	for 25 microwatts/cm^2
TSL251 " "	for 60 microwatts/cm^2
TSL252 " "	for 425 microwatts/cm^2

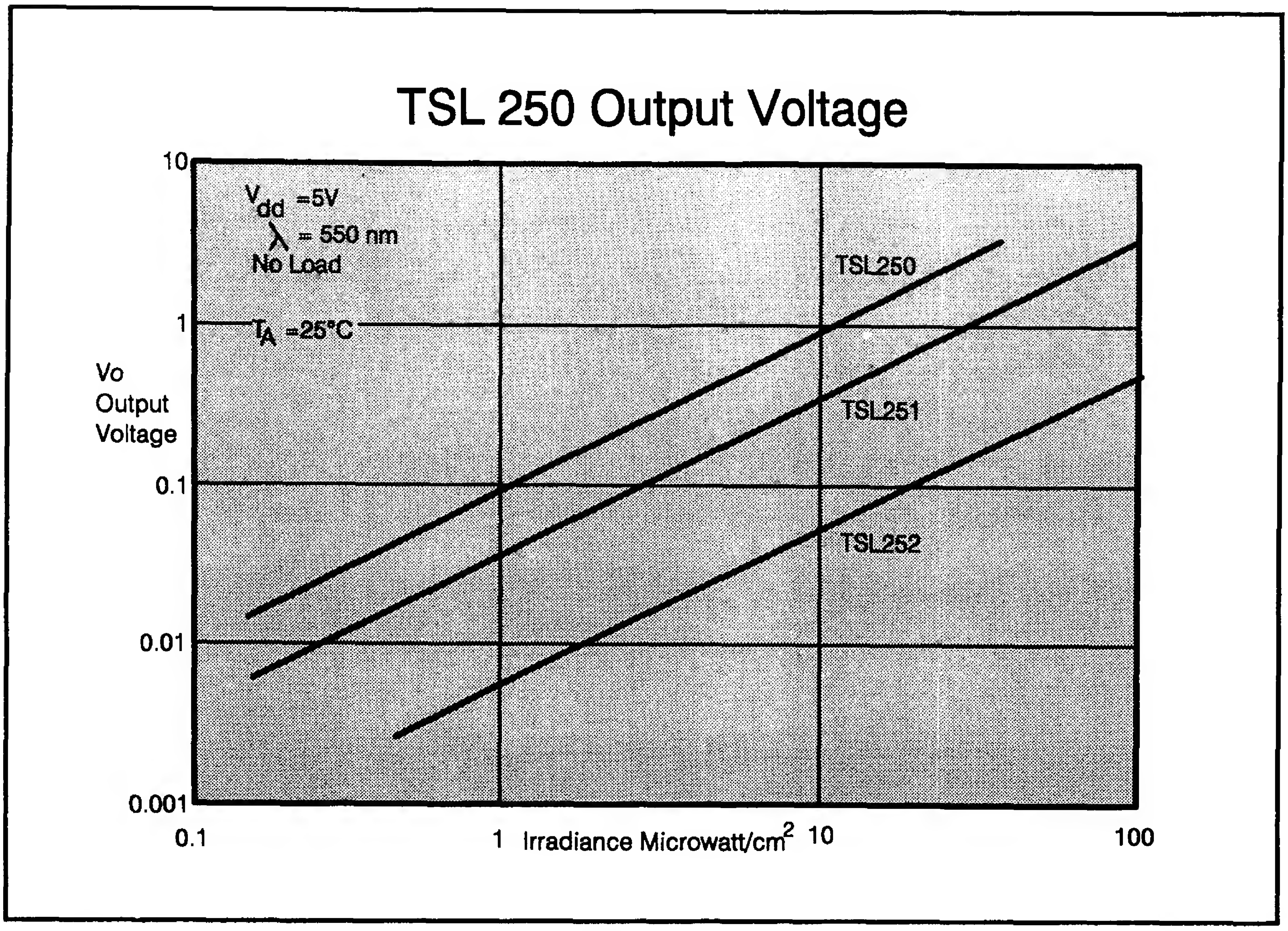


Figure 1.31 - TSL250 output voltage

To get some idea of what these incident light levels mean, we can consider a photo-metric equivalence (for visible radiation) of 90 lux = 14 μW/cm^2.

Dusk, when street lights are turned on, is about 70 lux. The TSL250 gives 2 V output at 150 lux. Office lighting at a work surface is typically 300-400 lux, where a TSL251 would give 2 V output. The TSL252 would give 2 V output in outdoor daylight illumination.

The TLS250 family is appropriate for a wide range of light sensing applications in light level control over a wide range of light levels, for security applications, and for boiler flame control in gas or oil heaters.

6.2.3 Characteristics

The LinCMOS™ trans-impedance amplifier (similar to the well-established Texas Instruments operational amplifier TLC272) provides stable low input offset. The TSL250 offers high dynamic range, with linear output up to 3V, with only 3 mV output in the dark.

The TSL250 has a significant advantage over discrete photo-diode light sensors under low illumination, since the high impedance output node of the diode is internal to the device. This makes the TSL250 inherently less sensitive to external electrical noise, so a highly stable sensitive detector can be realised without expensive and cumbersome screening techniques. Similarly the TSL250 is inherently less prone to current leakage problems in detector circuit assemblies.

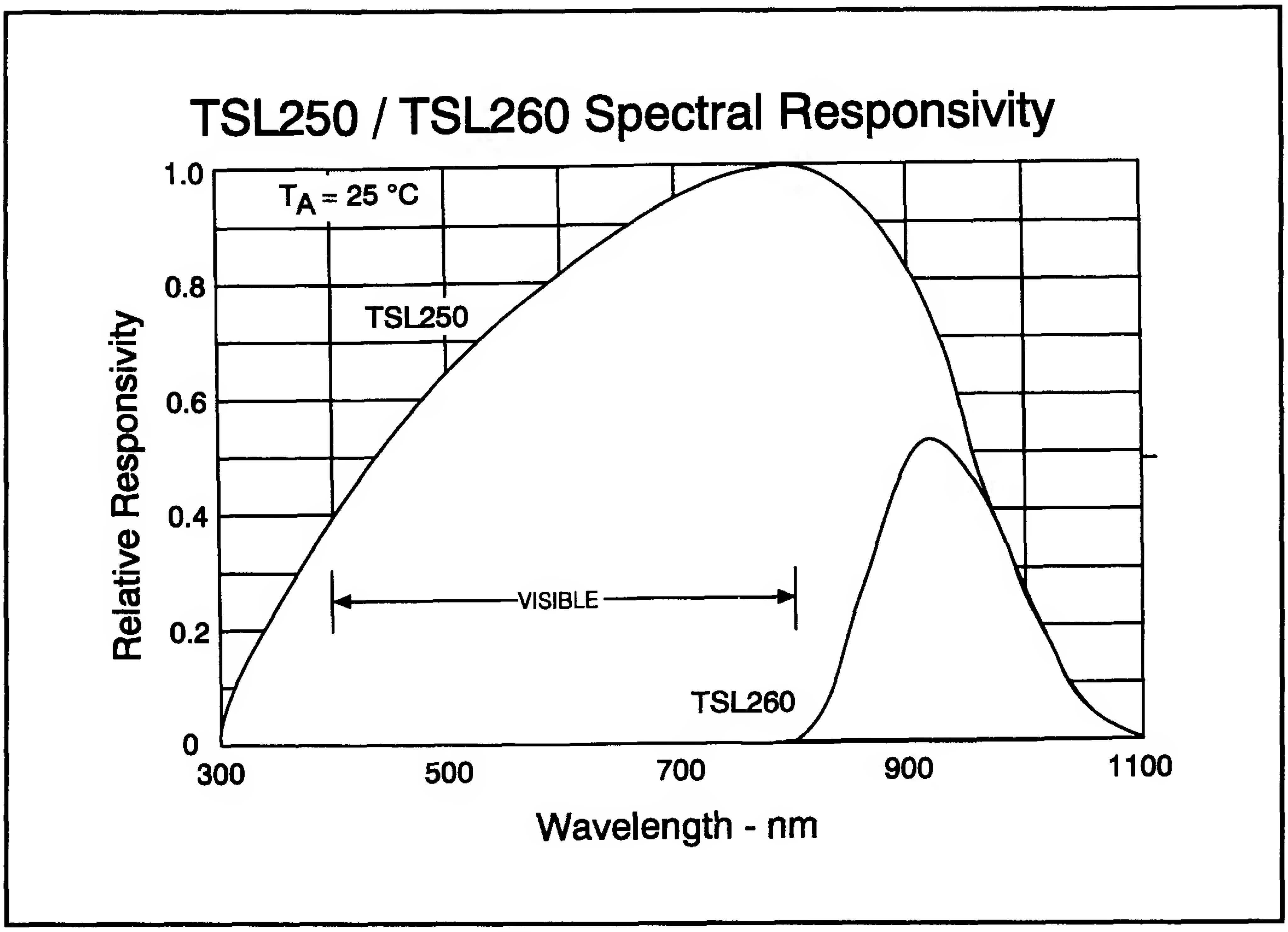
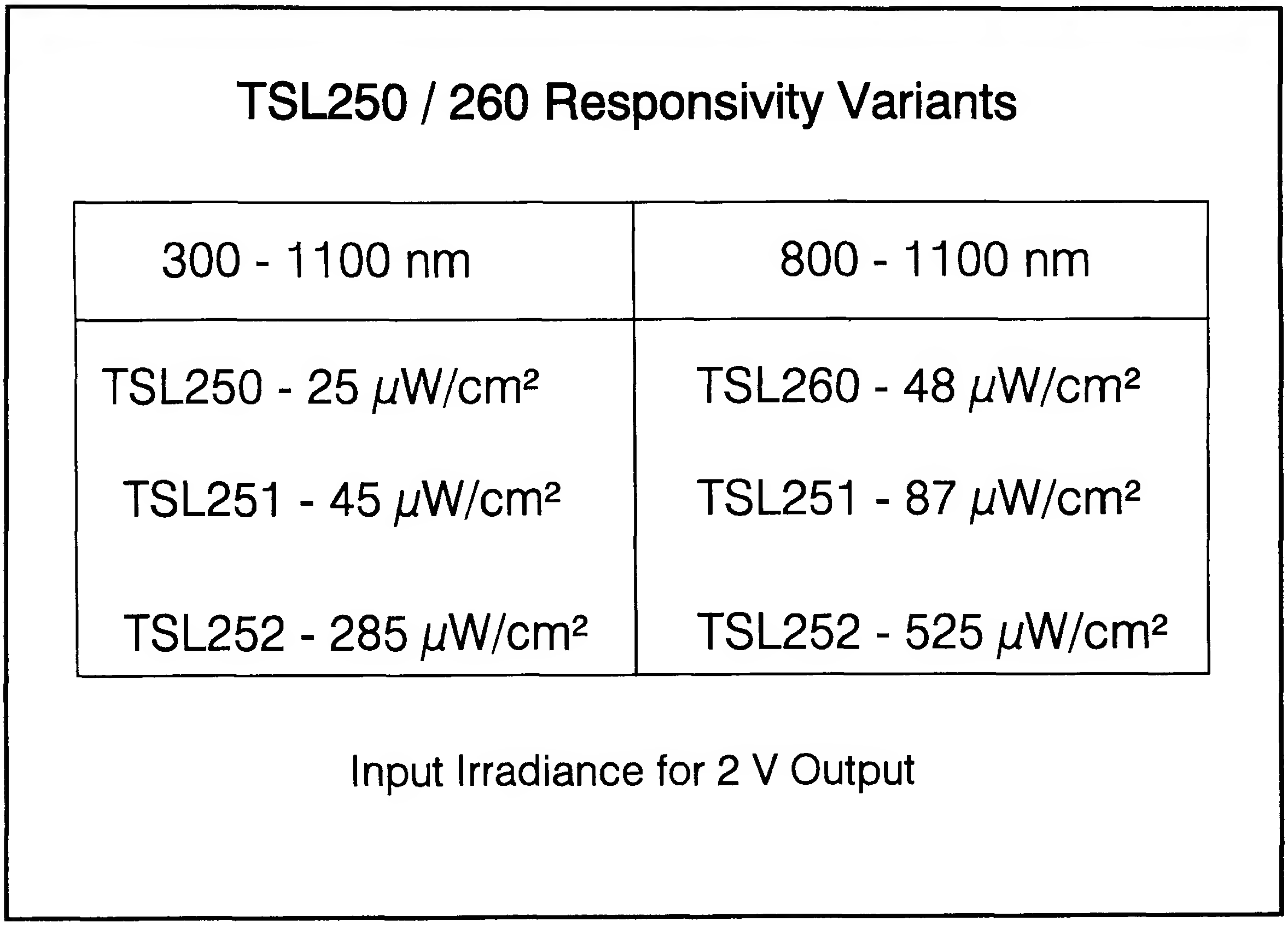


Figure 1.32 - TSL250 / TSL260 spectral responsivity

In summary, the TSL250 family has a highly linear, stable, low-impedance voltage output. The TSL250 output is stable with temperature, changing by 1 micro volt per degree Celsius. This is because the temperature coefficient of the polycrystalline silicon feedback resistor compensates the temperature coefficient of the photo-diode.

The TSL250 operates off a single supply voltage (it is characterised at V_{DD} = 5 V , but will operate between 3 V and 9 V), and consumes little current (800 µA at V_{DD} = 5 V when illuminated).

The TSL250 family is offered in a high-volume clear plastic side looker package. For applications like infra-red remote control where the device should not be affected by ambient visible light, the same silicon die can be packaged in a light-blocking, infra-red transmissive plastic. The family of infra-red-only light to voltage sensors is the TSL260, TSL261 and TSL262. The sensitivity of these filtered devices is less, with the voltage output at the peak response wavelength approximately halved.



TSL250 / 260 Responsivity Variants

300 - 1100 nm	800 - 1100 nm
TSL250 - 25 μW/cm^2	TSL260 - 48 μW/cm^2
TSL251 - 45 μW/cm^2	TSL251 - 87 μW/cm^2
TSL252 - 285 μW/cm^2	TSL252 - 525 μW/cm^2

Input Irradiance for 2 V Output

Figure 1.33 - TSL250 / TSL260 responsivity vs. variants

6.2.4 Speed Vs Responsivity

The internal feedback in the trans-impedance amplifier increases from the TSL252 to the TSL250. As the feedback is increased the speed is reduced. The TSL252 output rise and fall times are typically 7 µs, for the TSL251 they increase to 90 µs, and for the TSL250 they are 360 µs. In the TSL260 family the response time of each device corresponds to its unfiltered (TSL250) equivalent. For example the TSL261 has the same output rise and fall times as the TSL251.

The basic die design could be extended to higher speed operation, trading responsivity for speed, by reducing the diode area and the feedback resistor and capacitor values -- the extremely low dark voltage resulting from the LinCMOS™ technology would permit this.

6.2.5 TSL250/TSL260 Data conversion

From a 5-V supply rail the TSL250/TSL260 families give a linear output up to approximately 3 V, and saturate typically at 3.5 V. Use of a pull-up resistor can extend the linear output range to within typically 10 mV of the positive supply rail, with a penalty of only a few milli-volts increase in the dark level output. A TSL250 or TSL260 can be combined with an appropriate ADC to deliver light measurement to a digital processor.

3 V Digital Control Using TSL260

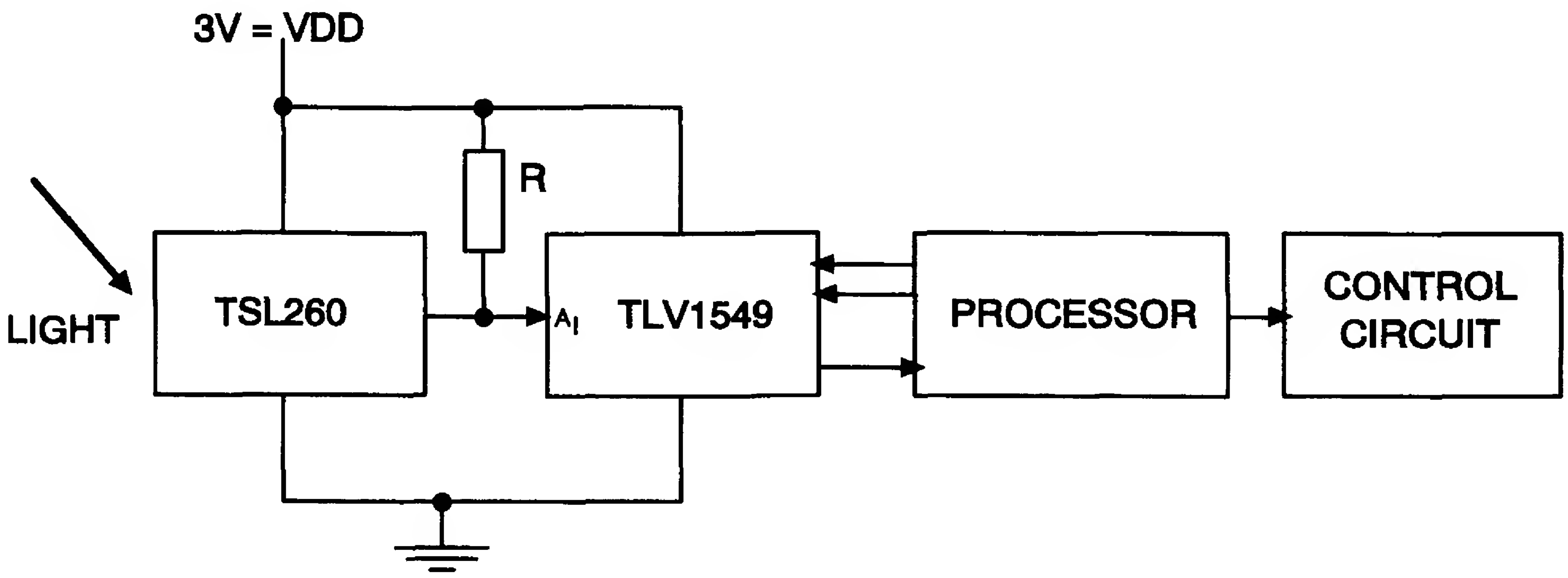


Figure 1.34 - Digital control using the TSL260

A simple schematic is shown, see figure 1.34, combining the TSL260 with the 10-Bit serial input ADC TLV1549, which is discussed elsewhere in the seminar. A pull-up resistor is used to give a good dynamic range from a nominal 3.3-V positive supply rail. The lowest dark level is obtained by use of a high pull-up resistor value, but this exacts a penalty in conversion speed. A resistor value of 100 kΩ will allow measurements of low light level, since the dark current level is typically 3 mV; however the conversion speed will be only 300 Hz. To run the TSL262 at its maximum speed with this simple circuit the resistor value would need to be reduced to 1 kΩ and the dark current level would increase typically to 15 mV.

The next device we shall consider operates through a different principle and is capable, at modest cost, of giving high resolution, linearity and speed.

6.3 Light-to-frequency sensors TSL230

6.3.1 Overview

Next we shall examine a high performance and low cost technique of delivering the output from a light sensor into the digital domain. Instead of classic conversion of an analogue sensor output through an A-D converter (either discrete as in the example of the TSL260 and the TLV1549; or with the A-D converter integrated into a micro controller, or sensor system processor like the TSS400) a photo diode current can be converted into a frequency output. This output can be handled by a counter or timer.

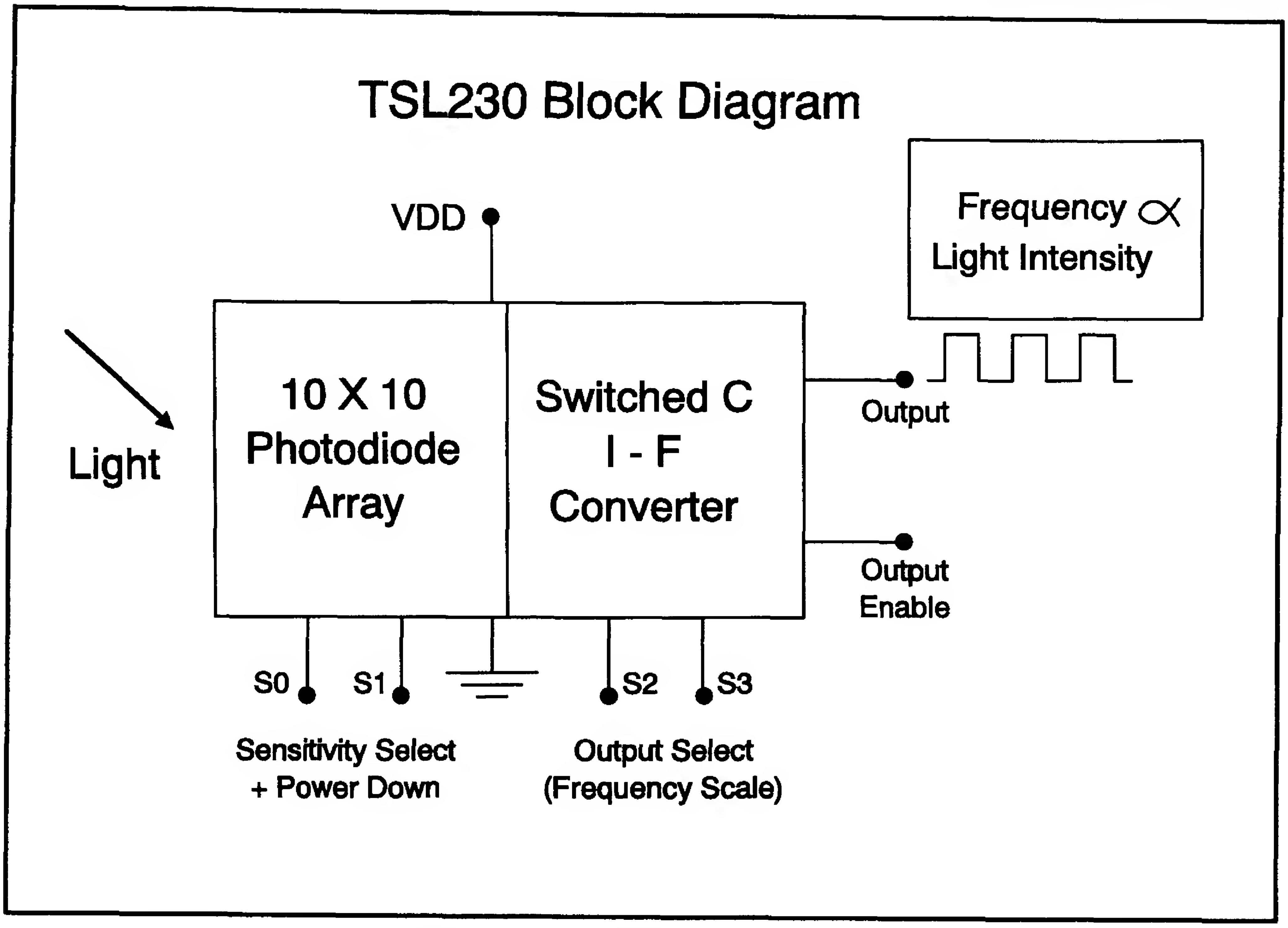

TSL230 Block Diagram
VDD
Frequency ∝
Light Intensity
Light
10 X 10
Photodiode
Array
Switched C
I - F
Converter
Output
Output
Enable
S0
S1
S2
S3
Sensitivity Select
+ Power Down
Output Select
(Frequency Scale)

Figure 1.35 - TSL230 block diagram

Next described is a low-cost programmable device, the TSL230. This enables a wide dynamic range of light level to be measured with high precision, linearity and temperature stability; or rapidly changing light levels to be processed. The TSL230 can be directly coupled to a digital processor, in micro controller, or logic control as the application dictates.

6.3.2 TSL230 Characteristics

The TSL230 is a monolithic programmable light-to-frequency converter. It is currently the only device of its kind to offer direct high resolution conversion of visible and short infra red radiation into digital format.

It contains an array of 100 photo diodes with a patented current-to-frequency converter (using switched capacitor charge metering). The output is a pulse train, with frequency proportional to the light intensity incident on the active photo diode area. Input lines from the digital control circuit provide real-time control of the TSL230 sensitivity (unlike the earlier TSL220 device no external capacitors need be provided) and offer a power-down function; also the output frequency can be scaled to match the characteristics of the digital control circuit. For stable or slowly changing light levels, very high resolution may be obtained by pulse counting; for rapidly changing light levels the pulse separation may be timed.

The TSL230 operates from a single supply (from 3 V to 6 V) drawing typically 2 mA supply current. These is a pin-programmable power-down option, reducing the supply to 10 micro amps when the sensor is not active. This is useful for portable, battery powered applications.

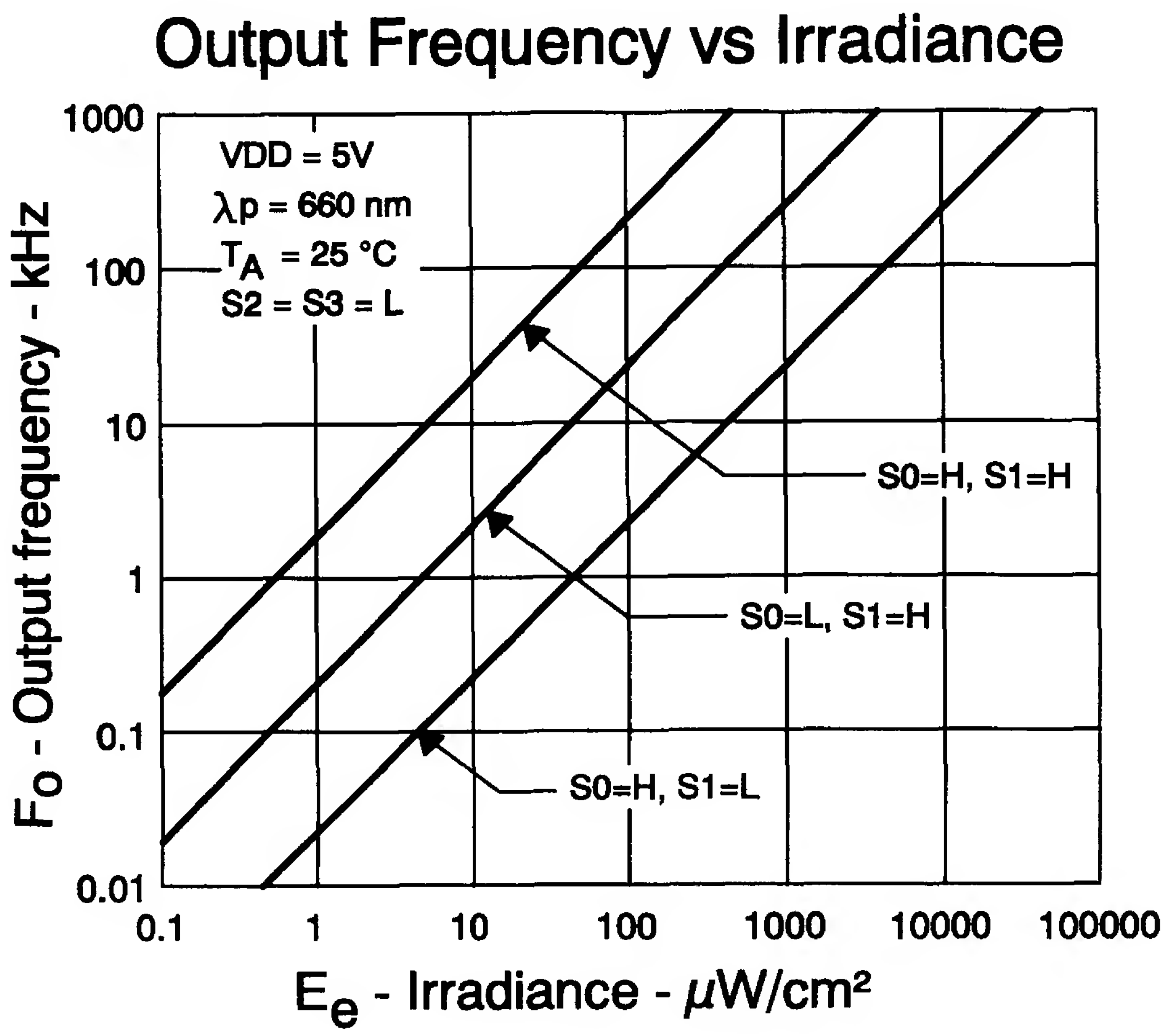


Figure 1.36 - TSL230 output frequency vs. irradiance

The programmable sensitivity of the TSL230 is effected by a simple electronic technique, switching in different numbers of the 100 elements of the photo diode matrix. These sensitivity ranges (X1, X10, X100) can be chosen through the logic levels of input pins S_0 and S_1. The digital control circuit can thus optimise the TSL220 operation to the ambient light level, preserving the full output frequency range. The light levels of 0.001 to 100,000 µW/am² can be accommodated directly, without the expense of filters.

For cost reasons, low cost micro controllers with limited frequency range may wish to be used for the digital control circuit. The TSL230 has two input lines S_2 and S_3 to provide output frequency scaling. Options are an undivided pulse train with fixed pulse width, or square wave divide-by-2, -10, or -100 outputs. There is also an output enable pin, so that the TSL230 can be placed in a high impedance state when not required. This is useful for applications where several input devices share a micro controller.

The TSL230 is temperature compensated to give a stable 300 ppm change in output frequency per degree Celsius (at 660 µm radiation).

The non-linearity error is low; being typically only 0.2% full-scale for the output frequency range 0 to 100 kHz. Dark output is typically only 1 Hz.

The TSL230 is offered in a transparent 8-pin Dual-In-Line package. It is highly versatile and suitable for a wide range of light-measuring and position-detecting applications.

The pulse output gives the TSL230 high noise immunity, making it suitable for industrial environments.

Typical applications of the TSL230 include water turbidty measurement, flame control in heaters, light-metering, fluid absorption measurement, paper handling, and general visual process control.

6.4 Line arrays - TSL213/TSL215

6.4.1 TSL213 Functional Block Diagram

6.4.2 Summary

The TSL213 array illustrates how a complex sensor, which integrates light-sensing , analogue and digital elements, can offer the prospects of low system cost, and ease of design.

The TSL213 is a 64-element line sensor, fabricated from the established Texas Instruments LinCMOS$^{(TM)}$ mixed-mode volume wafer technology. The pixels have a 125 micron centre-to-centre spacing. The TSL213 is a charge-mode sensor. That is, during an exposure period , a charge is developed on each pixel proportional to the product of the light intensity and the exposure time. (In this it is like a CCD imager, and analogous to photographic film).

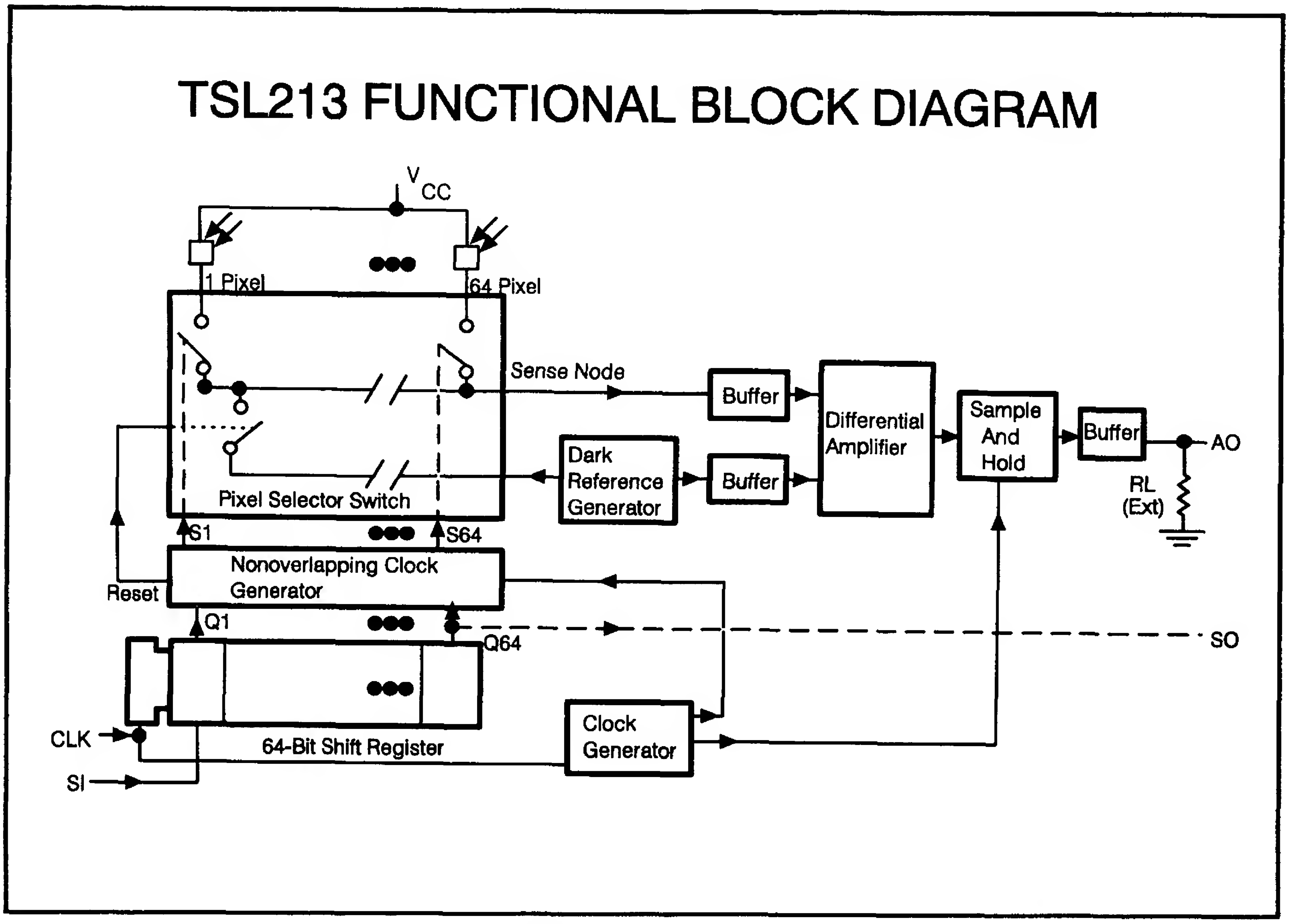

TSL213 FUNCTIONAL BLOCK DIAGRAM
V CC
1 Pixel
64 Pixel
Sense Node
Buffer
Differential Amplifier
Sample And Hold
Buffer
AO
RL (Ext)
Dark Reference Generator
Buffer
Pixel Selector Switch
S1
S64
Nonoverlapping Clock Generator
Reset
Q1
Q64
SO
64-Bit Shift Register
Clock Generator
CLK
SI

Figure 1.37 - TSL213 functional block diagram

On a single TSL213 die are integrated the light-sensing pixels, analogue signal conditioning, and digital address and switch elements (equivalent to approximately 2500 gates).

The internal complexity of the die has been chosen, to make the device easy to use in a microprocessor or digital processing system environment. To operate the TSL213, only a single 5V supply and integration (exposure) and pixel output clock pulses are required.

6.4.3 Characteristics

The TSL213 operates at data rates between 10 kHz and 500 kHz. The relatively large pixel size permits assembly in a high volume low cost 14-pin plastic dual-in-line package.

The TSL213 is recommended as a real alternative to either discrete photo-sensor arrays or to CCD line imagers in sensing systems where more than one sensor is required, and the sensors form part of a digital control system. Typically the pixel size in a line CCD imager is 10 microns, and for a discrete photo-diode or photo-transistor is 1000 microns. At 125 microns pixel size, the TSL213 is appropriate for many applications.

6.4.4 Function Blocks

The functional structure of the TSL213 is shown in Figure 1.37. There are 64 pixels in a line array, which are addressed individually (unlike CCD where all pixel charges are switched along an analogue register simultaneously).

The exposure or integration period is defined as the time between clock pulses on the Serial Input (SI) pin. The integration period is chosen in each application to give a suitable output level for the light intensity available.

The charge in each pixel is transferred to the output sense node by means of the Clock Pulse (CLK). The sense node generates a signal voltage directly proportional to the charge.

A 64-bit shift register controls the transfer of charges to the output and provides timing signals for the non-overlapping clock generator (NOCG). The NOCG provides internal control for the sensor elements , including charge sensing and reset. The reset establishes a known voltage at the sense node in preparation for the next pixel charge transfer. This voltage is used as a dark reference level for the differential signal amplifier. By means of the NOCG, feedthrough clock noise is eliminated at the output. The sample-and-hold signal generated by the NOCG holds the voltage analogue output of each pixel constant until the next pixel is clocked out.

6.4.5 TSL213 Timing Diagram

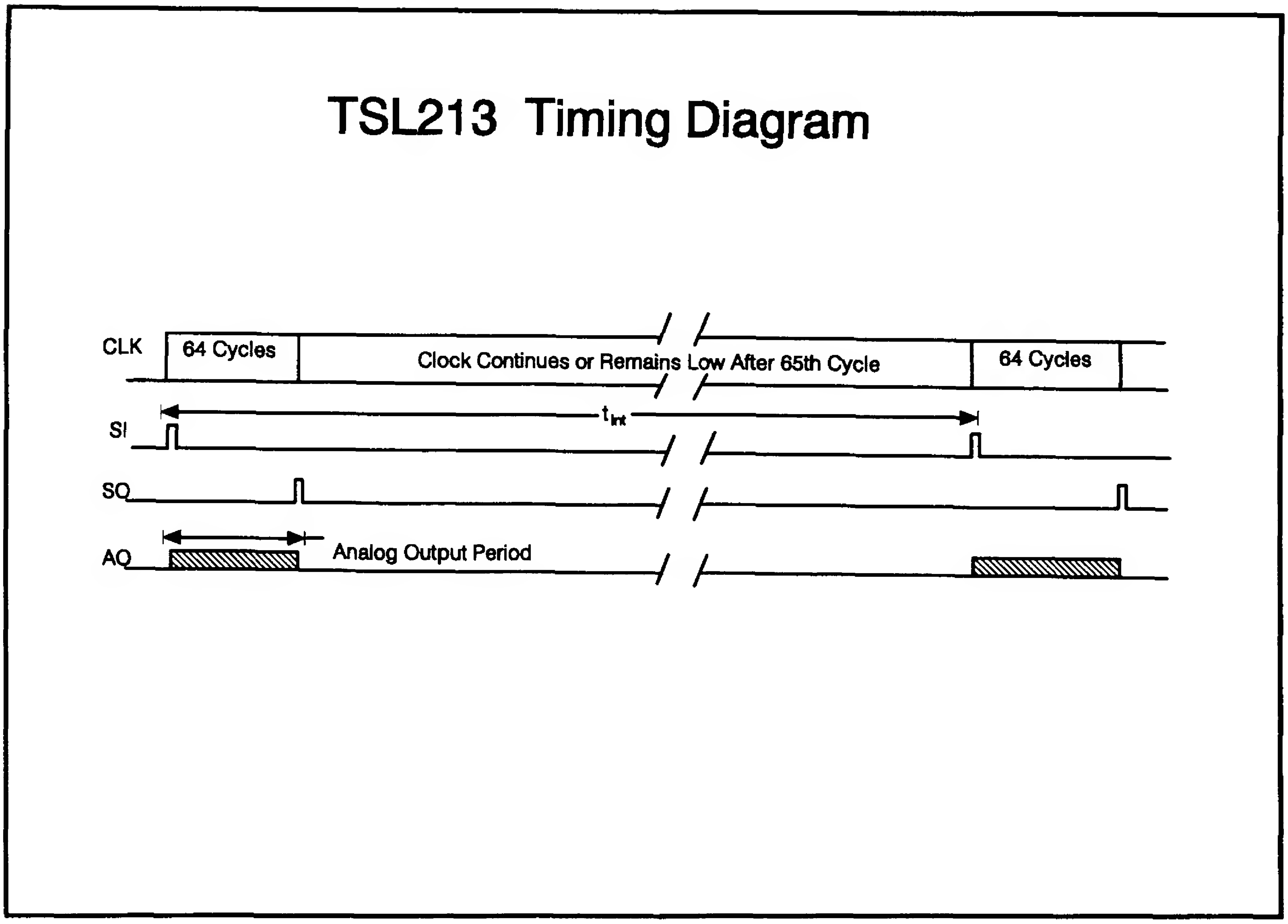


Figure 1.38 - TSL213 timing diagram

6.4.6 Combination Of Arrays

The architecture of the TSL213 enables more than one array or die to be connected in series or parallel configuration. Thus a 128 pixel device (TSL215) may be easily created. The 64 pixels of the TSL213 die are in groups of 8 pixels; the outputs of different groups may be balanced by means of resistors which can be fused to one of 5 levels at multiprobe. This enables long uniform arrays of pixels to be realised -- practical 1728 pixel 200 dpi A4 facsimile contact sensors can be made by serial connection of TSL213 dice.

Several TSL213 imager die may be connected in series or in parallel, on customised substrates to provide higher complexity imagers. For example, eight serially connected dice could make a 512 pixel line imager, for a mark reader such as a lottery card reader.

Serial Connection

For serial connection, the Analogue Outputs (AO) must be connected together and the Serial Output (SO) of each sensor array connected to the Serial Input (SI) of the next array. The externally applied SI pulse is applied only to the first array of the series. For n arrays in cascade the SI pulse is applied after each n x 64 positive going clock transitions.

Parallel operation

Parallel operation of multiple arrays is achieved by supplying clock and SI pulses simultaneously. The outputs of each device may then be processed separately.

Initialisation

At power up, or after a period of SI or readout clock inactivity exceeding the integration time, the sensor elements may need to be initialised. This consists of 15 consecutively performed output cycles to clear the pixels of any charge which has accumulated during the inactive period.

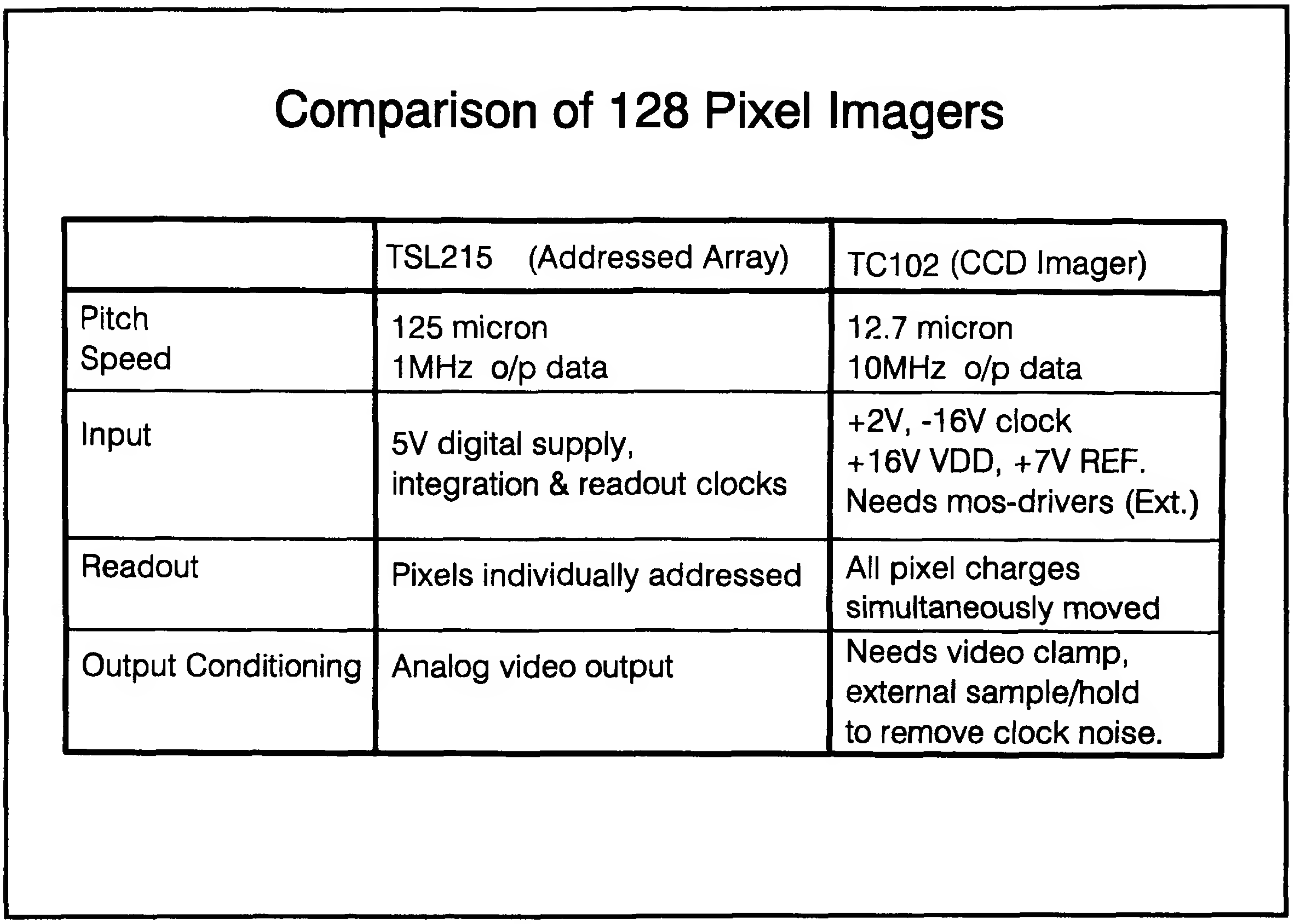
6.4.7 TSL215/TC102 Comparison

Summary

Two TSL213 dice may be combined serially within a single device to make the TSL215 128-pixel line sensor array. The TSL215 is here compared with a 128-pixel CCD line array , the TC102.

Pixel Size

The most obvious difference is that the active optical length of the TSL215 is almost 10 times that of the TC102. The TC102 is a CCD array where all the pixel charges of an integration period are clocked out together down transport registers, while the TSL215 is an addressed array where pixel charges are individually switched out. The coarser pitch of the TSL215 derives from the physical size of the switching elements (including the NOCG) associated with each individual pixel. For the standard LinCMOS™ technology the relatively fine optical resolution of the CCD cannot be realised.



Comparison of 128 Pixel Imagers

	TSL215 (Addressed Array)	TC102 (CCD Imager)
Pitch Speed	125 micron 1MHz o/p data	12.7 micron 10MHz o/p data
Input	5V digital supply, integration & readout clocks	+2V, -16V clock +16V VDD, +7V REF. Needs mos-drivers (Ext.)
Readout	Pixels individually addressed	All pixel charges simultaneously moved
Output Conditioning	Analog video output	Needs video clamp, external sample/hold to remove clock noise.

Figure 1.39 - Comparison of 128-pixel imagers

Data Rate

The maximum data output rate of the TSL215 has been set by the switching design at 1 MHz, whereas with careful driver circuit design the TC102 can deliver data out at up to

10 MHz. However, the TSL215 is far simpler and more economical to drive, and its output is more easily handled.

Drive Requirement

The TSL215 drive requirement is a single 5 V supply, an integration pulse and a output clock . The TC102, however, requires positive (+2 V) and negative (-16 V) clock pulses, +16 V V_{DD}, and a 7-V reference. The registers must be driven through a dual MOS-driver such as the TLD369.

Output Requirement

The output of the TSL215 is also much more convenient , being an analogue video envelope. With the TC102, the analogue voltage levels of the video pixels are offset by the output buffer amplifier, and must be externally clamped to a video black reference using a train of black reference pixels provided. External sample-and-hold must be done on the clamped voltage output, to eliminate the clock feedthrough noise between the valid pixel levels.

Cost

These input and output tasks with the CCD device make it much more expensive in a system, on top of the higher cost of the CCD device itself. (One advantage of the relatively coarse pixels is that a low cost plastic packaging technique may be used). For applications where arrays of discrete photo-sensors, or low resolution CCD were hitherto used, the TSL213/TSL215 provides an attractive alternative.

6.4.8 PC404/PC405 - Evaluation Systems

Evaluation kits, PC404/PC405, are available to facilitate initial evaluation of the TSL213 and TSL215 Line Arrays. They also demonstrate the simplicity of operation of the arrays with digital control circuits to perform complete light sensing functions.

PC404 kit

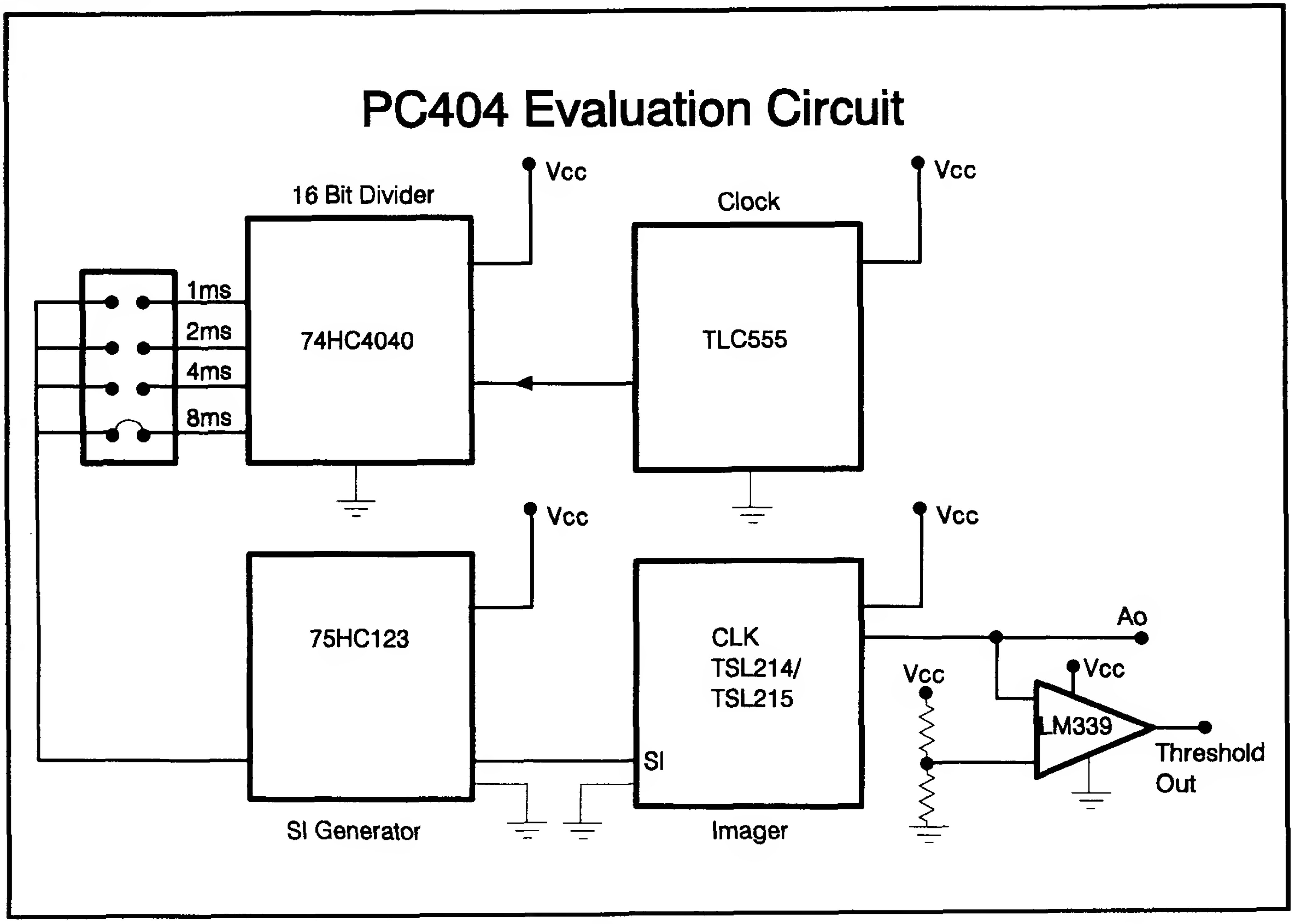

PC404 Evaluation Circuit
16 Bit Divider
Vcc
Clock
Vcc
1ms
2ms
4ms
8ms
74HC4040
TLC555
Vcc
Vcc
75HC123
CLK
TSL214/
TSL215
Ao
Vcc
Vcc
LM339
SI
Threshold
Out
SI Generator
Imager

Figure 1.40 - PC404 evaluation circuit

The PC404 consists of an imager, a circuit board with drive and output circuitry, and a detachable 10 x magnification lens in a housing. The circuitry of the PC404 comprises an oscillator, a counter/divider, a one-shot pulse generator and a comparator. The oscillator is built round a TLC555 timer and generates a 500 kHz output data clock pulse. the clock output of the oscillator is routed also to a 74HC4040 divider. This has a set of jumper terminals to four of the outputs, and 1 ms, 2 ms, 4 ms or 8 ms Integration Time may be selected. The chosen output is connected to the 75HC123 one-shot pulse generator, which provides the imager with the SI pulse.

Trimming potentiometers and test points are provided. Two alternative outputs are provided. One is the Analogue Output (AO); for the other - Threshold Out - the AO is routed to an LM339 comparator, which squares up the output for digital compatibility.

PC405 kit

The PC405 board is software based. A pre-programmed 8 bit micro controller provides the drive to the line imager, processes the imager output and drives a two-digit LED output display.

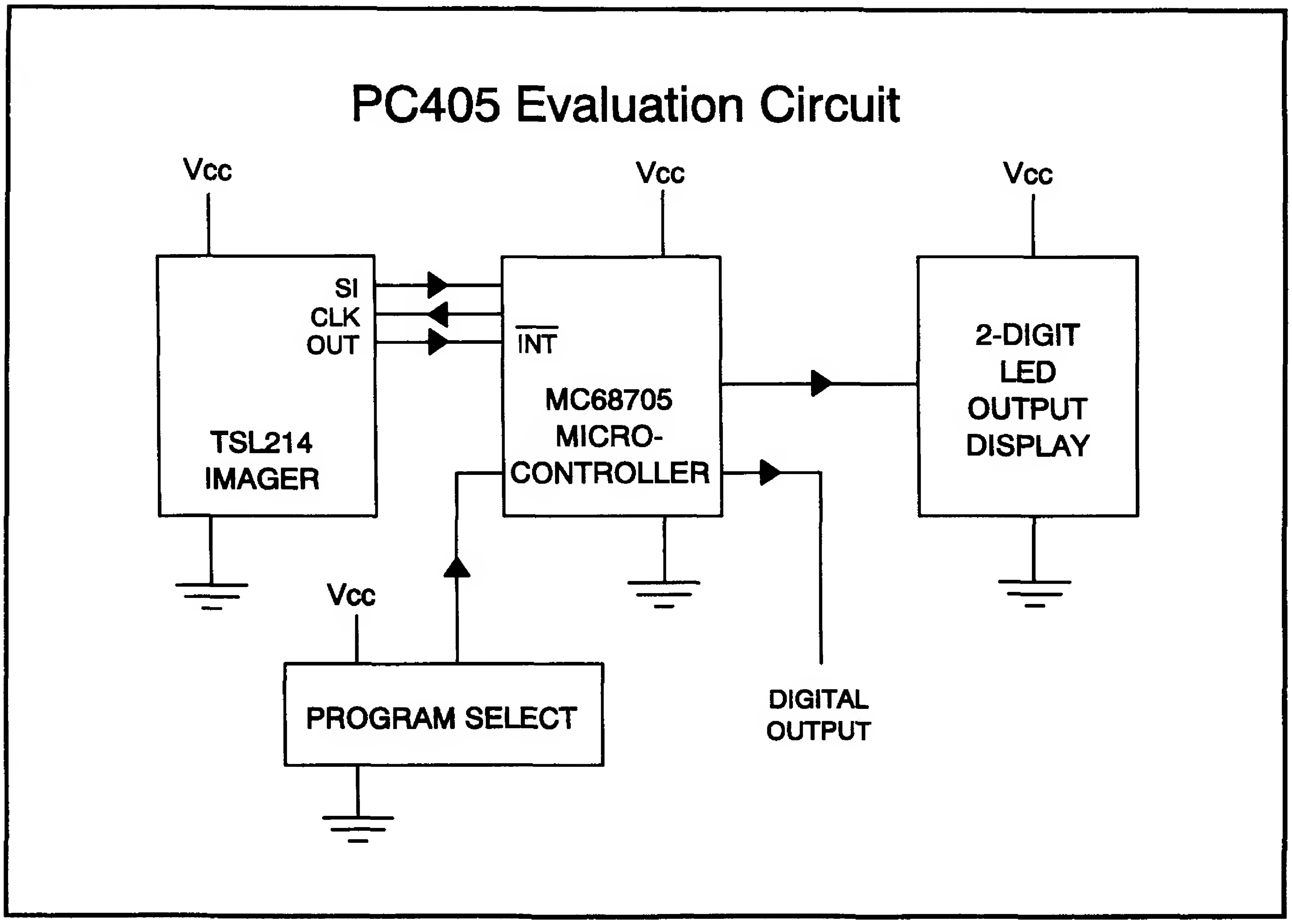

PC405 Evaluation Circuit
Vcc
Vcc
Vcc
SI
CLK
OUT
TSL214
IMAGER
INT
MC68705
MICRO-
CONTROLLER
2-DIGIT
LED
OUTPUT
DISPLAY
Vcc
PROGRAM SELECT
DIGITAL
OUTPUT

Figure 1.41 - PC405 evaluation circuit

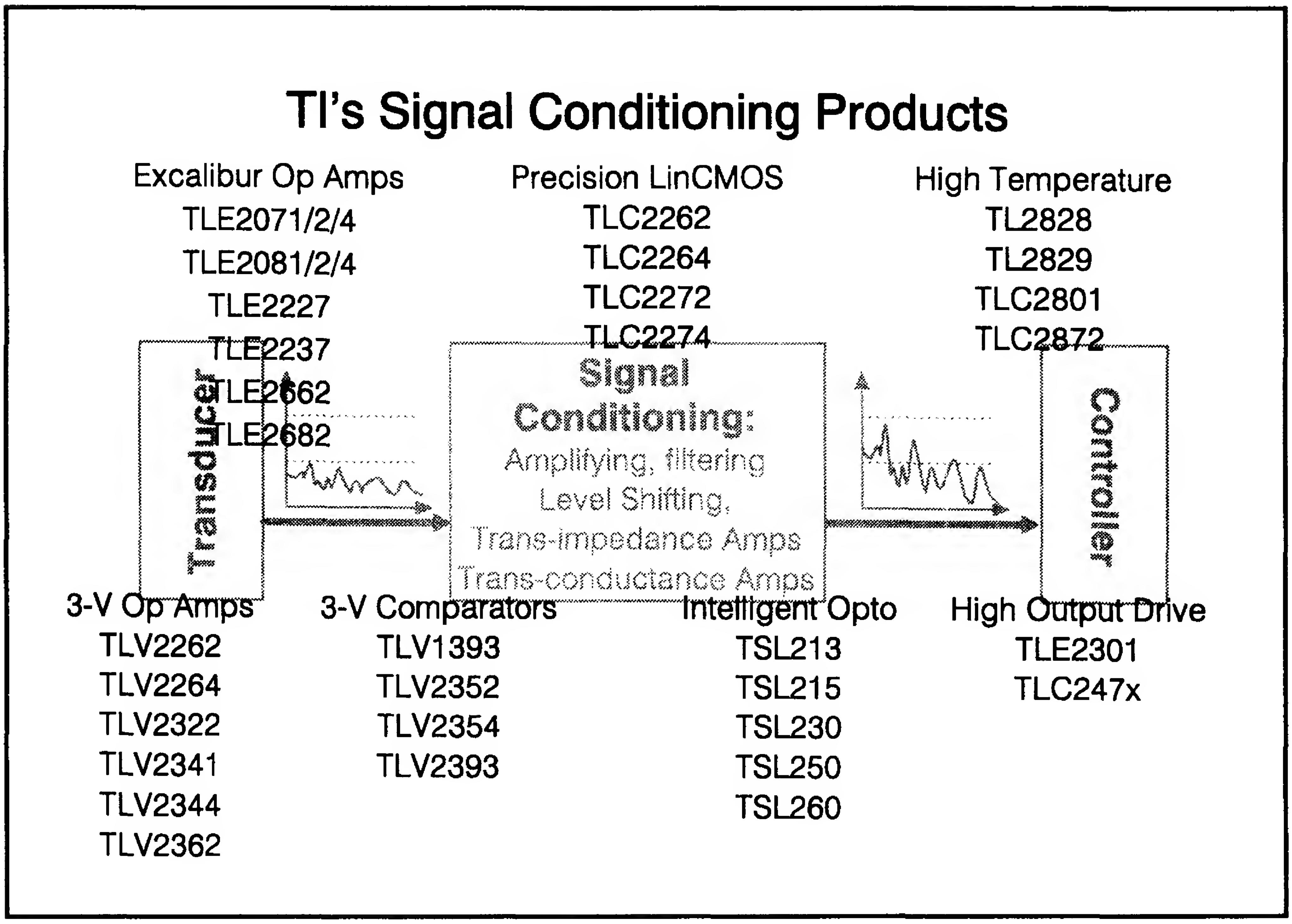
Four functions are available:

- Digital Output
- Object Edge Detection
- Line Position Detection
- Light/Dark Transition Counter

7 Summary

7.1 TI's signal conditioning products

TI has a long history in analogue signal conditioning products, and is continuing to introduce more products each year.



TI's Signal Conditioning Products

Excalibur Op Amps
TLE2071/2/4
TLE2081/2/4
TLE2227
TLE2237
TLE2662
TLE2682

Precision LinCMOS
TLC2262
TLC2264
TLC2272
TLC2274

High Temperature
TL2828
TL2829
TLC2801
TLC2872

3-V Op Amps
TLV2262
TLV2264
TLV2322
TLV2341
TLV2344
TLV2362

3-V Comparators
TLV1393
TLV2352
TLV2354
TLV2393

Intelligent Opto
TSL213
TSL215
TSL230
TSL250
TSL260

High Output Drive
TLE2301
TLC247x

Transducer
Signal Conditioning:
Amplifying, filtering
Level Shifting,
Trans-impedance Amps
Trans-conductance Amps
Controller

Figure 1.42 - TI's signal conditioning products

Most of these new products have been designed in Excalibur and in Advanced LinCMOS. These processes enable TI to produce high quality and high performance products capable of meeting most of today's system needs.

This seminar has discussed some of the newer and higher performance products, and Figure 1.42 lists most of the devices discussed today.

By gaining better market understanding and combining this with the Excalibur and Advanced LinCMOS technologies we hope to provide you with the right device to meet your needs.

Section 2
Power Supply

Section Contributions by:

Author

Tim Ardley

TEXAS
INSTRUMENTS

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1 Introduction

A power supply is required in every electrical and electronic system. When designing the power supply for the system, consideration needs to be given to the number of supply voltages required, the power handling capabilities of the supplies as well as the ultimate generator of the input. Depending on the power supply requirements of the system, there are seven building blocks that could be used to make up the power supply unit. The combination of the building blocks will depend on the input source and output power constraints of the system.

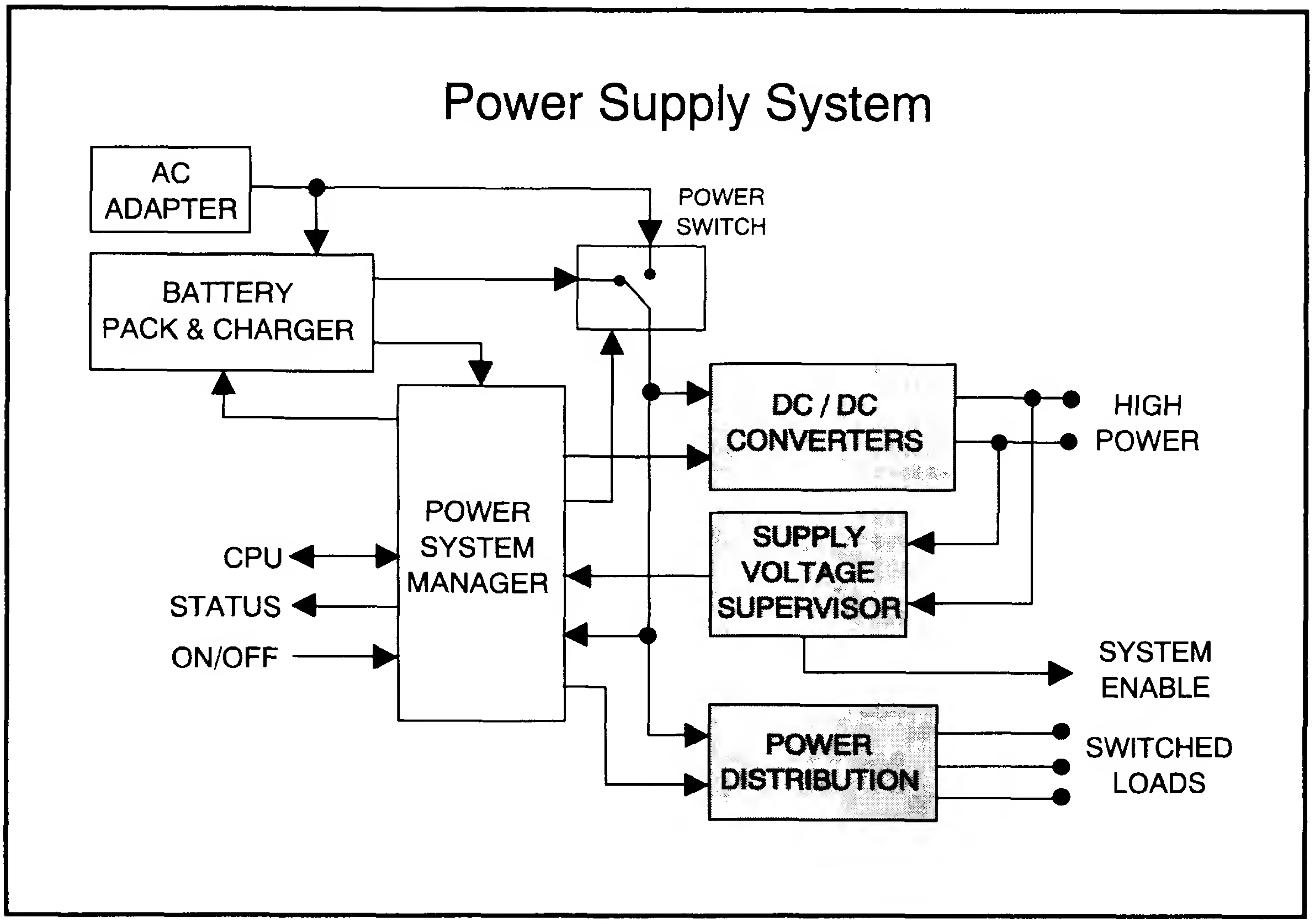

Power Supply System
AC ADAPTER
POWER SWITCH
BATTERY PACK & CHARGER
DC / DC CONVERTERS
HIGH POWER
CPU
STATUS
ON/OFF
POWER SYSTEM MANAGER
SUPPLY VOLTAGE SUPERVISOR
SYSTEM ENABLE
POWER DISTRIBUTION
SWITCHED LOADS

Figure 2.01- Power Supply System

1.1 AC Adapter.

The function of the AC Adapter is to transform an AC voltage into a DC voltage. Traditionally, this has been accomplished by the use of a stepdown transformer, bridge rectifier circuit, large smoothing capacitors and a linear regulator. However AC to DC converters are becoming popular due to the fact that they act as "intelligent switchers". The AC input voltage can vary from 90 V - 264 V at 47 - 63 Hz but the DC output must stay constant with little power dissipation in the module. This is difficult to achieve using the traditional method. The output voltage from the AC adapter can be in the range of

6 V to 24 V with a rated output power of between 25 W - 30 W. This specification can vary and is dependent on the voltage and power requirements of the application.

1.2 Battery pack & Charger.

Battery packs are generally made up of rechargeable batteries such as NiCd's. NiCd batteries have been the preferred chemistry technology due to their better power densities, but Nickel-hydrogen (NiMH) is becoming popular due to the environmental issues regarding NiCd's. The battery pack requires an accurate and constant current charge which is controlled by the battery charger. Battery packs can be damaged by management misuse such as over charging. The number of batteries used in a system is dependent on the required output voltage and power requirements of the system.

1.3 Power Switch.

The power switch enables the power supply unit to switch from AC adapter to battery sourced power without interrupting the systems supply. If only an AC adapter is used for example, then the Power switch could be a simple mechanical supply on / off switch. The power switch is required to handle high currents and therefore the on resistance of the switch - $R_{DS(on)}$ needs to be as low as possible to reduce power loss through power dissipation in the switch.

1.4 Power System Manager.

The Power System Manager (PSM) is the heart of the power supply system in that it provides direct interface to a CPU. The PSM unit is especially important in applications requiring high efficiencies such as in battery powered equipment. The PSM can control the charging time and current of the battery charger, the DC / DC converters and the distribution supplies through commands from the CPU thus powering down sections of a system to save power. The PSM can also take inputs from the Supply Voltage Supervisor (SVS) and act on the results or relate messages to the CPU if any problems occurring during the power-on stage.

1.5 DC / DC Converters.

DC / DC converters change an input voltage level to either a higher, lower or negative voltage. The input voltage source can be either from the AC Adapter or the battery pack. The converters efficiency in changing the input voltage to the required output voltage is important in both cases. The most common types of converter are the switching regulators which are covered in more detail in section 3.

1.6 Supply Voltage Supervisors.

Supply Voltage Supervisors (SVS) are used to monitor the input voltage to the power supply unit for early warning and from the power supply unit to ensure that the system only operates within a defined supply voltage window. The added feature is that devices sensitive to supply potentials can be protected during the power up and power down stage. The output(s) of the SVS can also be used as enable / disable controllers through an input control facility on the SVS.

1.7 Power Distribution.

Power distribution supplies are generally used in power supply systems where power efficiency is critical. Instead of the power supply being routed around the board to the individual components, the board is laid out in groups dependent on component function with a power supply control element being used to power-up and power-down the individual groups when required. This means that the overall power consumption of the system can be significantly reduced by turning off parts of the application that do not require power at a particular time.

2 Power Distribution

Power Distribution is generally used in power supply systems where power efficiency is critical. To save power, some sub-sections which are not continuously used can be shut-down and only powered up when required. It might be thought that mains powered equipment does not need to be as efficient as battery powered applications. However, new standards which place an emphasis on reducing the power consumption in main frame systems to make them more "Environmentally friendly" will become an issue in the near future.

There are two main types of power distribution; distribution switches and distribution supplies.

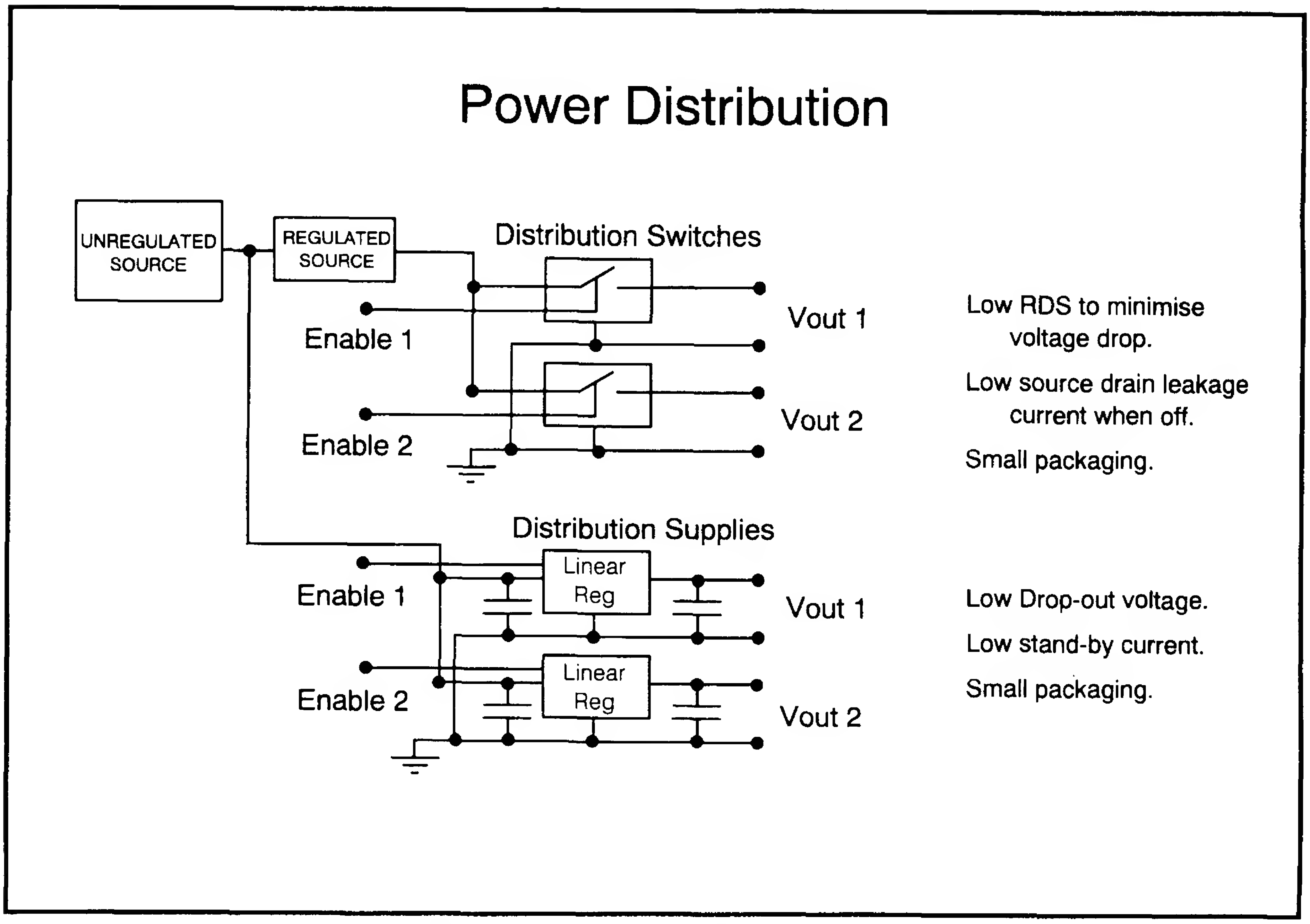

Power Distribution
UNREGULATED SOURCE
REGULATED SOURCE
Distribution Switches
Enable 1
Enable 2
Vout 1
Vout 2
Low RDS to minimise voltage drop.
Low source drain leakage current when off.
Small packaging.
Distribution Supplies
Linear Reg
Linear Reg
Enable 1
Enable 2
Vout 1
Vout 2
Low Drop-out voltage.
Low stand-by current.
Small packaging.

Figure 2.02 - Power Distribution

2.1 Distribution Switches.

Distribution switches are used in applications where a regulated power source is available for the system or that the input voltage variation is not critical to the systems performance. The distribution switch acts as an enable / disable function by connecting or removing power to the sub-section of the system as a simple mechanical switch might do. In both application areas, the voltage drop across the distribution switches needs to be as low as possible (ideally 0 V) so that all the input power is delivered to the application and very little is lost through the distribution switch.

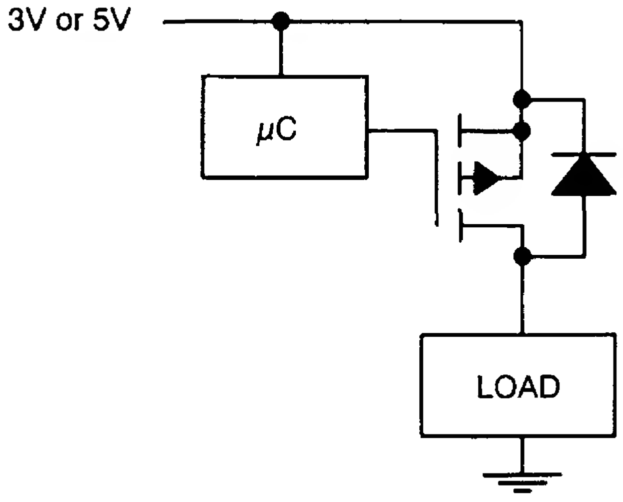
Another important parameter for a Distribution switch is the leakage current through the switch when open circuit. This must also be negligible so that the power consumption of the system is kept to an absolute minimum. An increasing development in plug-in cards for rack systems and computers is an interface between the mother board and the cards to protect the electronics from ESD.

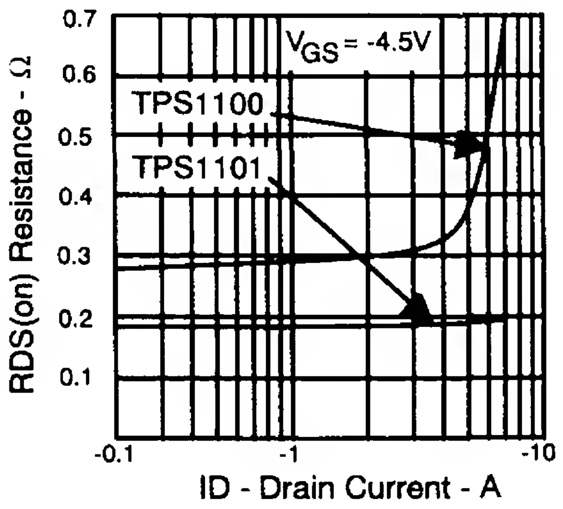
Texas Instruments has recently introduced a family of devices which are suitable for battery powered applications.

2.1.1 PMOS FET Switches.

Distribution Switches

- Ultra Low RDS(on)
  - TPS1100=0.18 Ω (@ -1 A, -10V)
  - TPS1101=0.09 Ω (@ -1A -10V)
- Ultra Low Leakage Current.
  - IDSS = -0.5 μA max
- Good AC Performance.
  - Tr = 10 ns, Tf = 2 ns (TPS1100)
  - Tr = 5.5 ns Tf = 13 ns (TPS1101)
- Small FootPrint.
  - 8 pin TSSOP Package
- ESD Protection





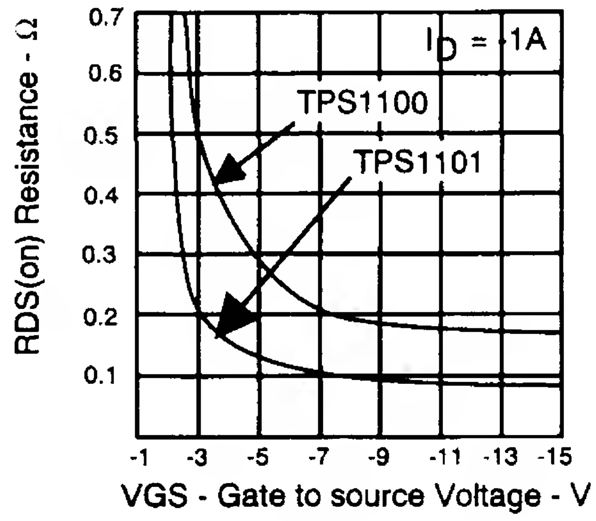


Figure 2.03 - Distribution Switches

The TPS1100 and TPS1101 have been designed specifically as a high-side switch for low voltage, portable battery management systems where maximising battery life is a concern. The key feature of these devices is the extremely low RDS(on) resistance which is specified at 0.18 Ω (typical) for the TPS1100 series and 0.09 Ω (typical) for the TPS1101 series. The TPS110X family also offers a high AC performance specification, with a rise time (t_r) of 5.5 ns (typical) and maximum switch current of ± 10 A for the TPS1101. The TPS1100 & TPS1101 have been designed to switch with V_{GS} voltages as low as -2.7 V (typical) making them ideal for 3.3 V applications, but also to address future lower voltage switching needs such as PCMCIA cards. For added security, the TPS1100 family has full ESD protection circuitry that increases the reliability of the end product in static sensitive areas. The TPS1100 is available in the new 8 pin TSSOP package thus offering a small foot print and a height of only 1.1 mm. This further reduces the board space and height requirements in high density and portable applications where component compactness is important. Due to the larger die size, the TPS1101 is available in the 16 pin TSSOP and the family is also available in the 8 pin SOIC package.

2.2 Distribution Supplies

In distribution supplies, the supply voltage (V_{CC}), different parts of the system is controlled through Linear series voltage regulators. This is the preferred method where the input power source is unregulated or clean supplies are required in a noisy environment. For example, if the input to the distribution switches runs close to a switching relay or RF generator, the supply could become contaminated with noise on the DC voltage. If series regulators are used, this generated noise on the DC voltage would be removed through regulation therefore supplying a clean supply voltage. In these types of applications the series regulator is situated close to the sub section. Enable pins are required on the voltage regulators so that they can be used to control different sections of the system independently.

2.2.1 Standard Linear Series Voltage Regulators

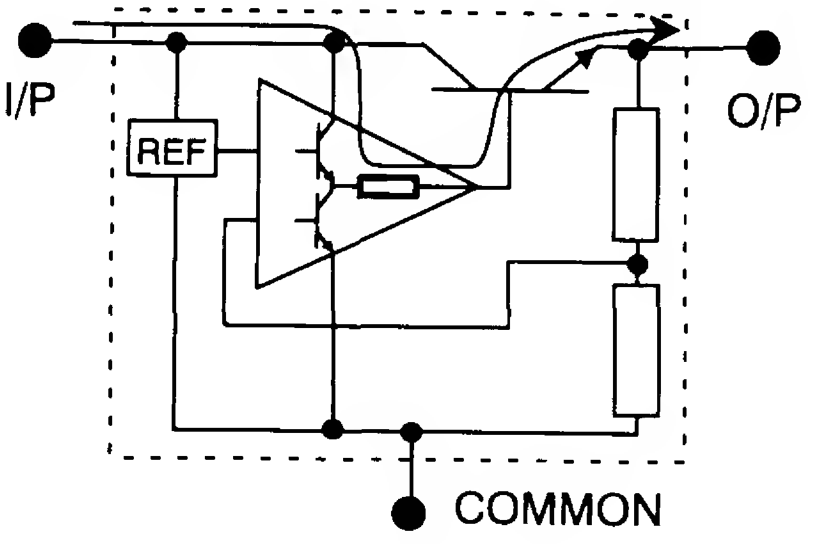
In the past, all linear regulators were designed with a series NPN pass transistor. Silicon techniques resulted in higher performance NPN transistors than PNP transistors. This meant that the NPN transistors were very much faster and had very much higher current gains than their PNP counterparts. So for low noise and good line and load regulation NPN transistors had to be used, but this meant that quite often minimum drop-out voltages of 2-3 V had to be allowed for. So a device providing an output current of 1 A had to be capable of withstanding a minimum power dissipation of 2 - 3 W. The drop-out voltages used would normally have to be much larger than this to allow for the poor regulation of the source, which means that the regulators had to withstand a much larger power dissipation and therefore heat sinking was required.

A standard linear voltage regulator will have a large voltage drop-out between its input and output terminals in the range of 1.7 V to 2.5 V. This is due to the NPN pass transistor which requires the base drive circuitry voltage to be above the output voltage ($V_{base} = V_{out} + 0.7$ V). The error amplifier's output drive capability is not ideal and therefore a voltage drop will occur between its output and supply voltage. This is due to the output resistance of the error amplifier and the effective Collector / Emitter voltage drop of the drive transistors. This voltage drop can be in the region of 0.5 V to 1.3 V depending on the required output current and will make the drop-out voltage in the region of 2 V above the output voltage. (see figure 2.04).

The quiescent current of the voltage regulator is the result of the biasing current required for the internal reference and the error amplifier. The drive current required to turn on the NPN is ultimately fed to the load, which makes the standard voltage regulator have a better overall efficiency compared to Low Drop-Out voltage regulators.

The increase of low voltage supply and battery powered applications led to the development of serial voltage regulators that have much lower drop-out voltages. This has come about with improvements in PNP transistors.

Linear Series Regulators



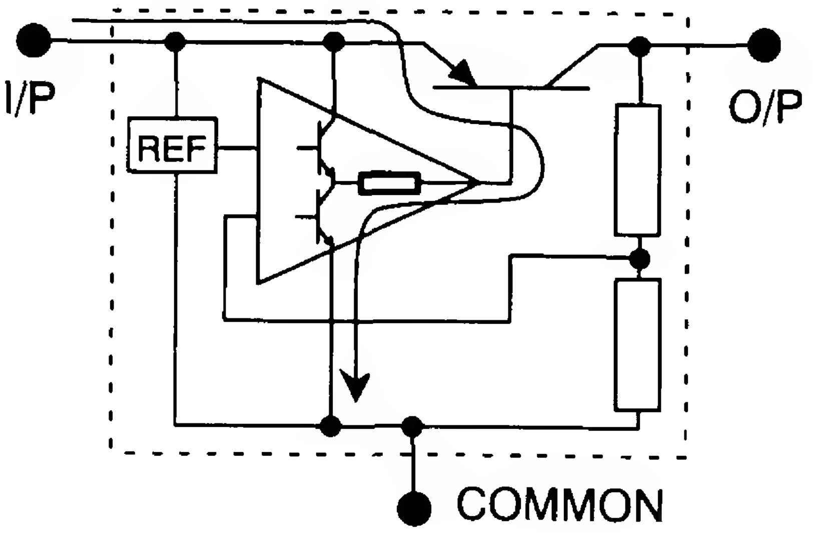
Traditional Linear Series Voltage Regulator

Pro's:

- Lower Quiesent currents. (6 mA)
- Good output Noise Voltage. (46 µV)

Cons:

- Higher drop-out Voltage. (1.7 V)
- Higher I/P Regulation. (200 mV)



Low Drop-Out Series Voltage Regulator

Pros:

- Excellent drop-out Voltages. (0.6 V)
- Good I/P Regulation. (10 mV)

Cons:

- Higher Quiesent Current. (10 mA)
- Higher O/P Noise Voltage (500 µV)

Figure 2.04 - Linear Series Regulator

2.2.2 Low Drop-Out Voltage Regulators

The Low Drop-out (LDO) Regulators use PNP pass transistors which allows the base drive circuitry to be below the output voltage. The drop-out voltage is now dependent on the V_{ce} voltage of the transistor (V_{ce} ~ 0.3 V) thus enabling a much smaller drop-out voltage. However, LDO's are more prone to oscillate under certain conditions. This is due to the PNP being in an "inverter" configuration (base voltage low, collector voltage high), and that the operational amplifier now sees a larger drive capacitance between the base and collector. The quiescent or bias current of a PNP voltage regulator is significantly larger than its NPN counterpart because the base current now has a path to the common rail and not the output pin as in the standard voltage regulators.

LDO's are only important if the power consumed is critical and the input voltage is reasonably regulated (i.e. from a battery) or where the input can vary by a large amount and regulation must be maintained (i.e. starting a car's engine where the battery voltage can fall to as low as 5.6 V). In other applications, traditional voltage regulators will do just as well as an LDO.

Texas Instruments released its own family of low drop-out voltage regulators in the late eighties. These were aimed primarily at automotive applications, which was one of the driving forces behind low drop-out regulators at the time. This is why the TL750/1L and TL750/1M families have 60 V load-dump protection specifications and reverse voltage input voltage protection.

2.3 Battery Powered Applications

Batteries are an increasingly important component in many forms of electrical and electronic equipment since they are a practical way of storing electrical energy. There are two different types of batteries; primary and secondary. Primary batteries can only be used once because the chemical reactions that supply the current are irreversible. Primary batteries are the most common batteries available today because they are cheap and simple to use. Carbon-Zinc dry cells and alkaline cells dominate portable consumer applications where supply currents are low and usage is random. Secondary batteries, which are sometimes called storage batteries or accumulators, can be used, recharged and reused (rechargeables). In these batteries, the chemical reactions that provide current from the battery are readily reversed when current is supplied to the battery. The major benefits of these batteries are their high current delivery and the economics of a rechargeable product. Only two rechargeable battery chemistries, lead-acid and nickel-cadmium (NiCd) have achieved significant commercial success.

Battery Powered Applications

Considerations for Maximising Battery Life

- Drop-Out Voltage:
    Minimum Input Voltage
    Power Dissipation .
- Quiesent Current:
    Amp-Hrs in Standby
    Biassing in Drop-Out
- Output Tolerance:
    Minimum Input Voltage.
- Lower Output Voltage:
    System Supply Voltage.

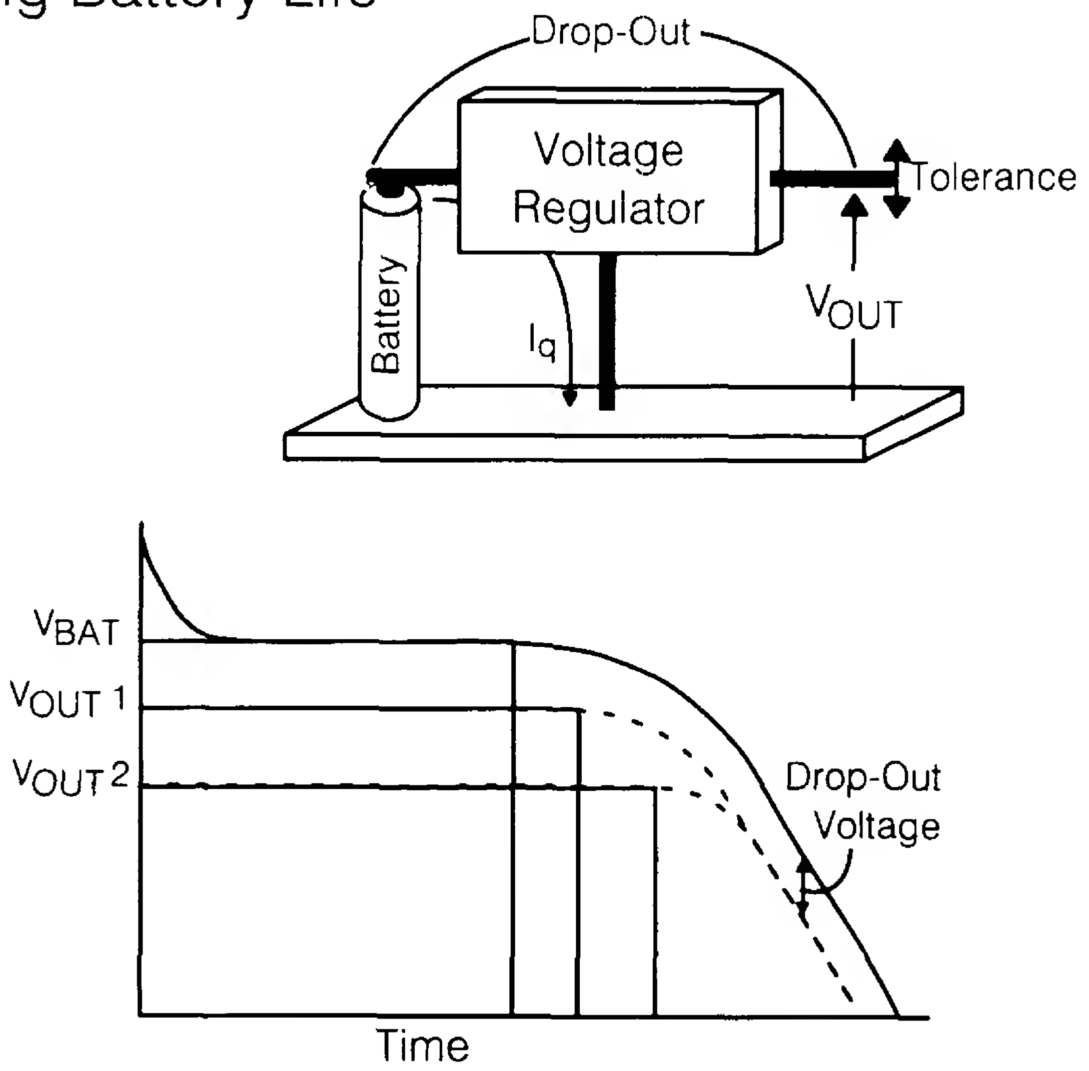


Figure 2.05 - Battery Powered Applications

A NiCd cell generates a nominal 1.2 V (lead acid battery is 2 V) and therefore to generate a minimum 5 V supply, 5 NiCd batteries have to be used. However, this would equate to a 6 V supply. From the initial full charge state, the total battery voltage could be as high as 7.5 V. This is too high for 5 V digital electronics where the maximum supply is specified at 5.25 V. Therefore, a fixed voltage regulator must be used to achieve the 5 V output.

A major problem with using batteries for power supplies is that the output voltage varies with the amount of current being removed from the cell since the series resistance of the battery is comparatively large.

Designers of portable, battery powered systems such as cellular telephones, laptop computers, hand-held voltmeters and portable sensor instruments have two main concerns. These are to extend the battery life of the equipment and to reduce the product's physical dimensions.

Battery life can be extended by four ways;

2.3.1 Drop-out Voltage

The dropout voltage of a regulator is the difference between the input voltage and the output voltage when regulation ceases and is an important parameter for series regulators. Reducing the drop-out point of the regulator extends the life of the battery by allowing the regulator to function longer from a lower input voltage. All batteries exhibit relatively large output resistance, which increase with the battery's life span. Low drop-out regulators help to increase the lifetime of the battery by reducing the output impedance of the battery. For a linear voltage regulator, the drop-out point is reached when the voltage provided by the battery has degraded to such a low level that the regulator can no longer provide the correct regulated voltage.

2.3.2 Quiescent Current

To extend the battery life of a portable system further, the LDO should have a TTL or CMOS compatible enable pin that can be used to switch it into a standby operating mode. This facility can be used to automatically power down the system when it is not in use so that battery power is conserved. One parameter is the "stand-by" current that the regulator consumes when the output is turned off since it will affect the life time (Amp - Hrs) of the battery when the unit is not in use. The value of the standby current is only really critical if the equipment is likely to be powered down for long periods of time. A more important parameter is often the amount of current that the regulator will consume in order to maintain regulation. The ratio of the output current and the biasing current of the regulator that needs to be as high as possible. A third important parameter is the amount of biasing current that the regulator will consume when it goes out of regulation and still providing current to the load.

2.3.3 Lower Supply Voltage

Using a lower operating supply voltage can add to the battery life of a system since the battery voltage can fall lower while the regulator still maintains a regulated output voltage. This is one of the reasons why digital supply systems are moving from 5 V to 3.3 V. Another benefit is that the operating power requirements is reduced if the supply voltage is reduced.

2.3.4 Regulator Output Voltage Tolerance

The output tolerance will have an indirect effect on the minimum input voltage of the regulator. If the tolerance of the regulator is 5% for example, then the minimum input voltage to maintain regulation will be the maximum drop-out voltage plus the 5% output voltage tolerance of the regulator. Therefore it is important to select a regulator with a low output tolerance and low drop-out voltage.

2.4 TL75LPXX Family of Voltage Regulators

Texas Instruments has recently introduced a family of fixed voltage regulators which have been specifically designed for battery powered applications. The key features of these devices are low drop-out voltage and low power standby mode. Another key feature of the TL75LPXX family is that all devices are available in the latest 20 pin Thin Shrink Small Outline Package (TSSOP). The TSSOP is comparable to the SOIC package in surface area but only has a height of just 1.1 mm, and so allows higher density applications where the height is critical to be achieved on the PCB. The TL75LPXX family also has maximum continuous reverse voltage capability of -15 V (which is a requirement for battery powered applications), reverse voltage transient protection to -50 V and load dump protection to 60 V for noisy environments in the automotive and industrial segments.

The TL75LPXX family of Low drop-out regulators address the concerns for linear pass regulators as discussed in section 2.3 of this section.

2.4.1 Low Drop-out Voltage

The drop-out voltage for the TL75LPXX family is typically 220 mV @ 300 mA of output source current. This drop-out voltage falls to a typical of just 120 mV @ 100 mA of output current. The absolute maximum drop-out voltage for the TL75LPXX family of devices is just 400 mV when sourcing 300 mA. This is the lowest drop-out voltage linear regulator that Texas Instruments manufactures at present.

TL75LPXX Family of Voltage Regulators

Low Drop-Out Voltage Regulator With An Enable Pin

- Only 220mV (typical) Drop-out at 300mA of output current.
- Available in TSSOP.
- Standby Mode Available.

Device	O/P Voltage
TL75LP48QPW	4.85 V
TL75LP05QPW	5.00 V
TL75LP08QPW	8.00 V
TL75LP10QPW	10.0 V
TL75LP12QPW	12.0 V

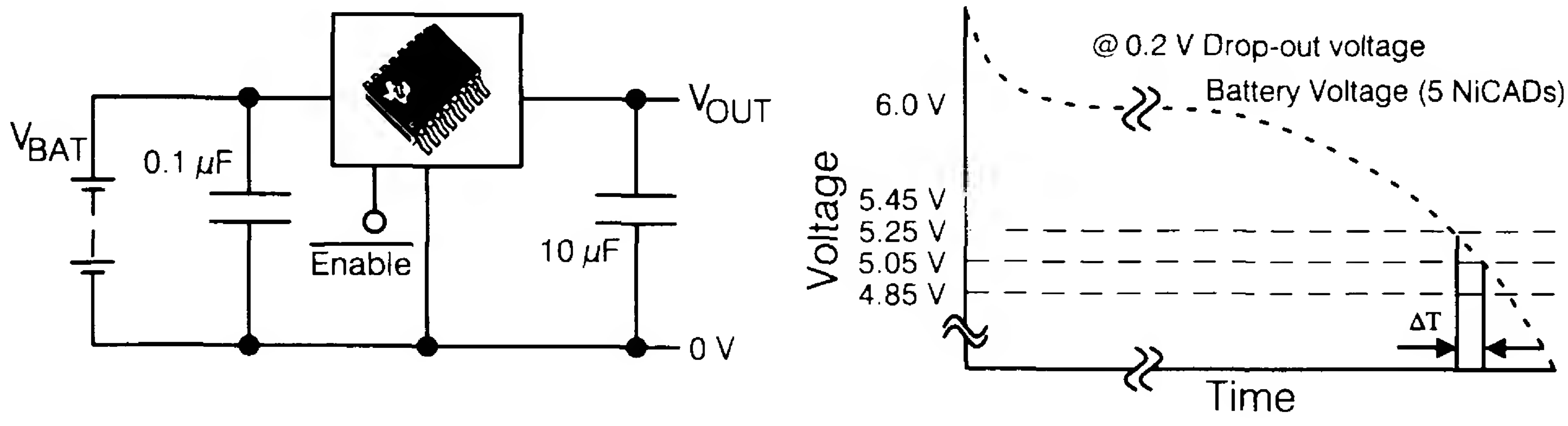


Figure 2.06 - TL75LPXX Family of voltage regulators

When a LDO regulator goes out of regulation (the input voltage is not sufficiently high enough potential to maintain regulation), the regulator's quiescent current will increase due to the reduced current gain of the pass transistor. In this condition, the PNP pass transistor is driven into saturation and therefore further reduces the efficiency of the regulator. This is another important reason for using a regulator with a low fixed output and drop-out voltage.

2.4.2 Low Power Stand-by Mode

The TL75LPXX has an enable / disable pin which places the output part of the voltage regulator into a high impedance state. In this condition, the voltage regulator will only consume a typical current of 100 µA. The standby mode is TTL and CMOS compatible which makes it suitable to be controlled by virtually any digital system.

2.4.3 Lower Supply Voltage

There is a voltage option of 4.85 V available in the TL75LPXX family of voltage regulators. A lower supply voltage for 5 V systems can be used because of the regulator's tight output tolerance. With an output voltage of 4.85 V and maximum tolerance of ±2%, the minimum output voltage will be 4.75 V which equates to the minimum supply voltage of TTL. This lower output voltage (4.95 V max.) results in an increase in battery life of the system by letting the input voltage drop further (5.25 V - 4.95 V = 300 mV) before the regulator goes out of regulation. The length of this "extra time" (shown in figure 2.06 as Δ T) is dependent on the application in question and the battery pack used. Reports of 20 minutes or more usage is not uncommon among battery operated equipment.

2.4.4 Output Tolerance

Modern devices have an output tolerance of ± 5% which equates to an output voltage range of between 4.75 V - 5.25 V and which increases the nominal input voltage required to maintain regulation. The TL75LPXX family of regulators have an output tolerance of just ± 2%, thus reducing the effective input voltage required to maintain regulation. The tight output tolerance has also made it possible to reduce the supply voltage. which is explained in section 2.4.3

2.4.5 Design Considerations

De-coupling Capacitance & Stability

The input and output capacitance loading is important to the performance of any low drop-out voltage regulator. The TL75LPXX Family of voltage regulators only require a minimum input capacitance of 0.1 µF, and a minimum output load capacitance of 10 µF. This saves both board space and height compared to the more common 100 µF load capacitors required by most other similar voltage regulators. The reduction in the load capacitance value will also bring a reduction in component cost. Without a load capacitor, the output will oscillate to a peak of the input voltage. The capacitance value and its Equivalent Series Resistance (ESR) affect the control loop of the device and therefore must be defined for the load and temperature range. Like all LDO's, as the output current increases, the LDO becomes more stable, and therefore do not require a large ESR capacitance value. However, as the load current approaches 0 A, the LDO will have a higher risk of oscillation due to the PNP pass transistor not being driven sufficiently.

To overcome the problem when low output capacitance values such as 10 µF are being used, Texas Instruments recommends the use of a resistor, Rs connected between the output and the load capacitor. This has the effect of increasing the ESR of the capacitor and reducing the possibility of the device oscillating under light load conditions.

The recommended value of this series resistor is 1Ω.

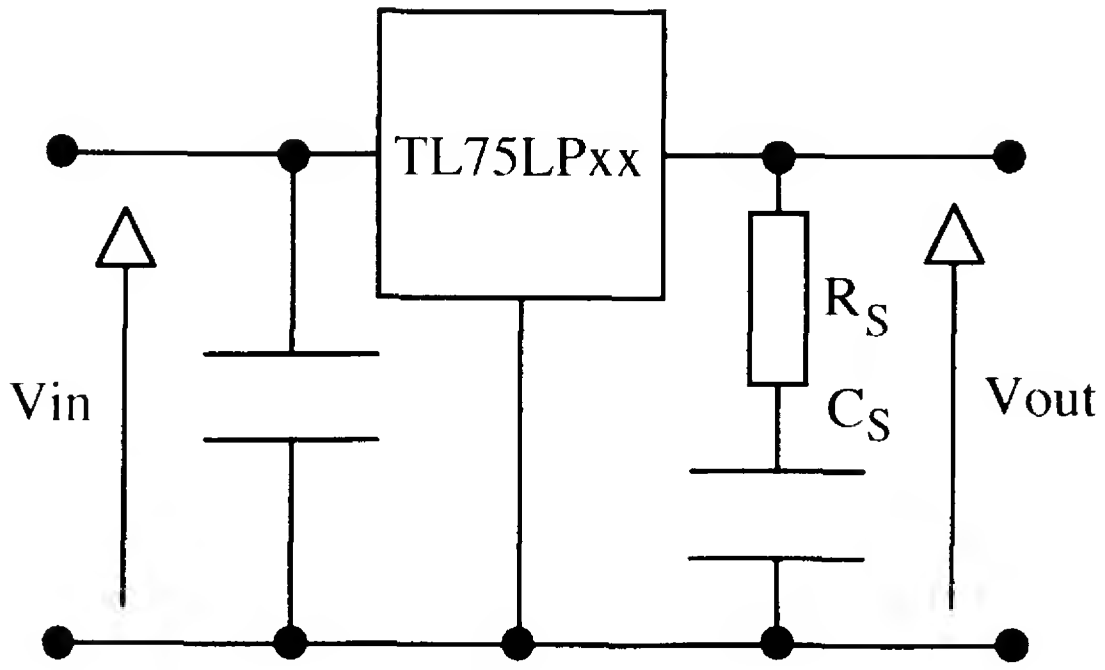


Figure 2.07

However, there are a few negative aspects of using a low value of output capacitor. As the load capacitance of the LDO is reduced and the output current increased, the output noise voltage will increase. This may become important when supplying an operational amplifier with a poor Power Supply Rejection Ratio (PSRR). The line regulation performance is also reduced in that larger output voltage "spikes" may occur with sudden output current changes.

Start-up Current

A characteristic of a LDO is the initial start-up current of the device. The feedback network from the output makes the operational amplifier drive the PNP pass transistor into saturation. This action causes the LDO voltage regulator to take a higher start-up current which can be in the region of 40 mA. This current will fall off sharply once the regulated output voltage reaches its desired output. Once the regulator is in this state, the quiescent current will be in the region of 2.5 mA with 10 mA of output current.

Texas Instruments has recognised that relatively high start-up current is a major problem area in battery powered applications and is therefore in the process of designing a family of new voltage regulators with FET pass elements instead of PNP's and with even lower stand-by and bias currents.

2.5 3.3-V Power Supplies

Like established 5-V supply systems, the 3.3-V supply is dictated by the needs of the digital system. There are a number of reasons why moving to 3 V is attractive for the digital system. From a technology standpoint, low voltages allow smaller transistor geometry's which permit higher density technologies (particularly 64 MByte DRAMs and beyond) and faster digital circuits. When combined with lower power consumption it is obvious that digital systems such as portable computers have to benefit from moving to 3.3 volts. At present, the portable market uses 5 NiCd cells or more to generate the required 5 V supply voltage. With the supply being reduced to 3.3 V, only 3 NiCd cells are required to generate a nominal voltage of 3.6 V. Since much of the weight and equipment size is governed by the size of batteries, the reduction in the number of batteries will enable smaller end equipments to be manufactured.

3.3 V Supplies

Like 5V, 3.3 V is being driven by The Digital world
Because :-

- Increased Memory Capacity
  (64Mb and greater)
- Reduced Power Consumption
  (P = V x I)
- Reduced Battery Pack Size
  (6V= 5 Cells, 3.6V = 3 Cells)
- Increase In Operating Speed

5.0 V

3.3 V

Figure 2.08 - 3.3 V Power Supplies

2.6 TLV2217-33 LDO Voltage Regulator

The 3.3 Volt supply potential has become the preferred voltage compared to 3 V since it has full 3.3-V standard JEDEC approval. In response to this new 3.3-V standard, Texas Instruments designed a new low drop-out 3.3 V fixed output voltage regulator named the TLV2217-33. This was specifically designed to meet the new 3.3 V JEDEC standard. The TLV2217-33 has a maximum drop-out voltage of 500 mV while sourcing 500 mA of output current. Since the drop-out voltage is low, the minimum input voltage can be 3.8 V which makes it suitable for running off existing 5 V supplies. This enables the device to be designed into the mixed supply systems which are being designed at present.

TLV2217-33 Voltage Regulator

3.3 V Low Drop-Out Fixed Output Voltage Regulator

- Meets the new 3.3 V JEDEC Standard.
- Available in the New TSSOP (surface mount package)

Application Areas

- 3.3 V from existing 5 V supplies.
- Medium power 3.3 V hand-held systems.
- 3.3 V High density applications

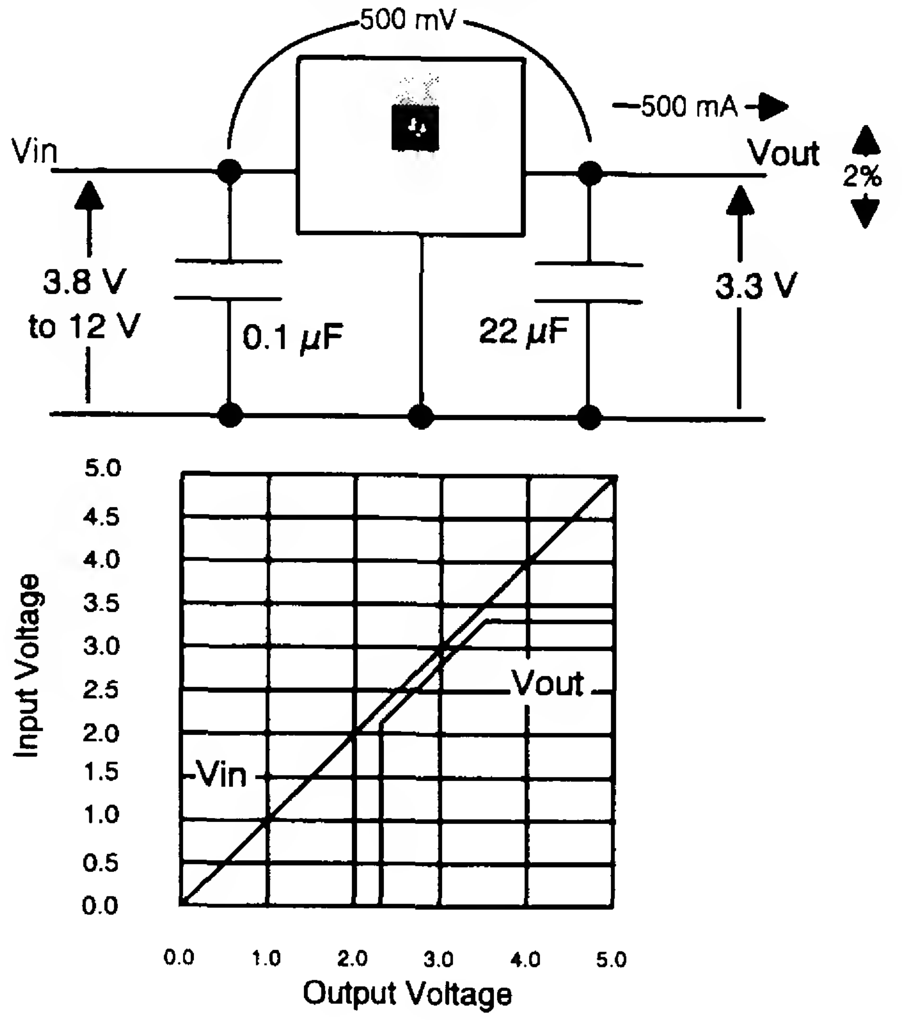


Figure 2.09 - TLV2217-33 Voltage Regulator

The device is available in the new 20 pin Thin Small Shrink Outline Package (TSSOP) for high density applications. The package is comparable to the surface area of the SOIC package, but only has a height if just 1.1 mm high. The output tolerance is 1% at $T_J = 25°C$ which guarantees an accurate output voltage. The TLV2217-33 requires input and output de-coupling capacitors to make the voltage regulator stable. The minimum input capacitor value is 0.1 µF while the typical output value is 22 µF.

At present, the alternative solution is to use a variable voltage regulator whose output can be adjusted to 3.3 V. The disadvantage of using a variable voltage regulator is the number of external components required. Two de-coupled resistors must be used as the feedback network to the voltage regulator. Most variable voltage regulators on the market do not have low drop-out voltages when sourcing high output currents. This can render the voltage regulator unsuitable for operating off existing 5 V supplies.

2.6.1 Design Considerations

De-coupling Capacitor

The main design consideration for the TLV2217-33 is the minimum ESR (Equivalent Series Resistance) loading of the output smoothing capacitor. Choosing the right ESR and capacitor value will ensure stability throughout the output current range of 0 A to 500 mA. The TLV2217-33 data sheet shows two graphs associated with the stability and the ESR value of the capacitors. The output current requirement of the regulator affects the ESR of the load capacitor in that lower the output current, the greater the required capacitor's resistance needs to be. This is also shown in a graph within the data sheet.

The lowest capacitor value that the TLV2217-33 can operate with and be stable on the output is 10 μF with an ESR of 2 Ω. However, if low output currents are to be used, then a higher value capacitor such as 22 μF or greater. However output ripple rejection will suffer since this can be linked directly to the value of load capacitor.

Bias Current

The TLV2217-33 has a typical bias current of 2 mA with no load output current. In mains powered applications this parameter is not too critical. In battery powered applications however, the bias current under no load is regarded as a significant power loss and therefore needs to be as low as possible. The TLV2217-33 does not have an enable pin to place the device into a stand-by mode like the TL75LPXX. However, the TLV2217-33 can still be designed into battery powered applications by placing an electronic switch such as a F.E.T between the power source and the input to the regulator. This will reduce the stand-by bias current of the TLV2217-33 to negligible levels.

2.6.2 Design Ideas

The following applications are not intended to document the specific design of a circuit, but rather to generate ideas in the minds of Engineers and Engineering Managers.

Enable pin

An Enable pin for the TLV2217-33 can be simply designed as shown in figure 2_10. There is a limitation with the application drawing in that the digital gate is driving the external pass transistor which has a maximum sink current capability. Since the TLV2217-33 is capable of supplying a maximum of 500 mA of output current, Q1's base current will be in the region of 20 mA. Therefore a Darlington transistor may be used for Q1, but this will increase the overall drop-out voltage of the regulator by at least 1.2 V.

Another potential solution that would overcome the excessive increase in the drop-out voltage of the regulator circuit would be to use the TPS1100 P-Channel Enhanced MOSFET. However, the digital control element would need to be an "open collector" configuration for the transistor to operate as a simple switch. A "current snatch" resistor will most probably be needed across the source - gate pins of the MOSFET to aid the switching characteristics of the open collector transistor.

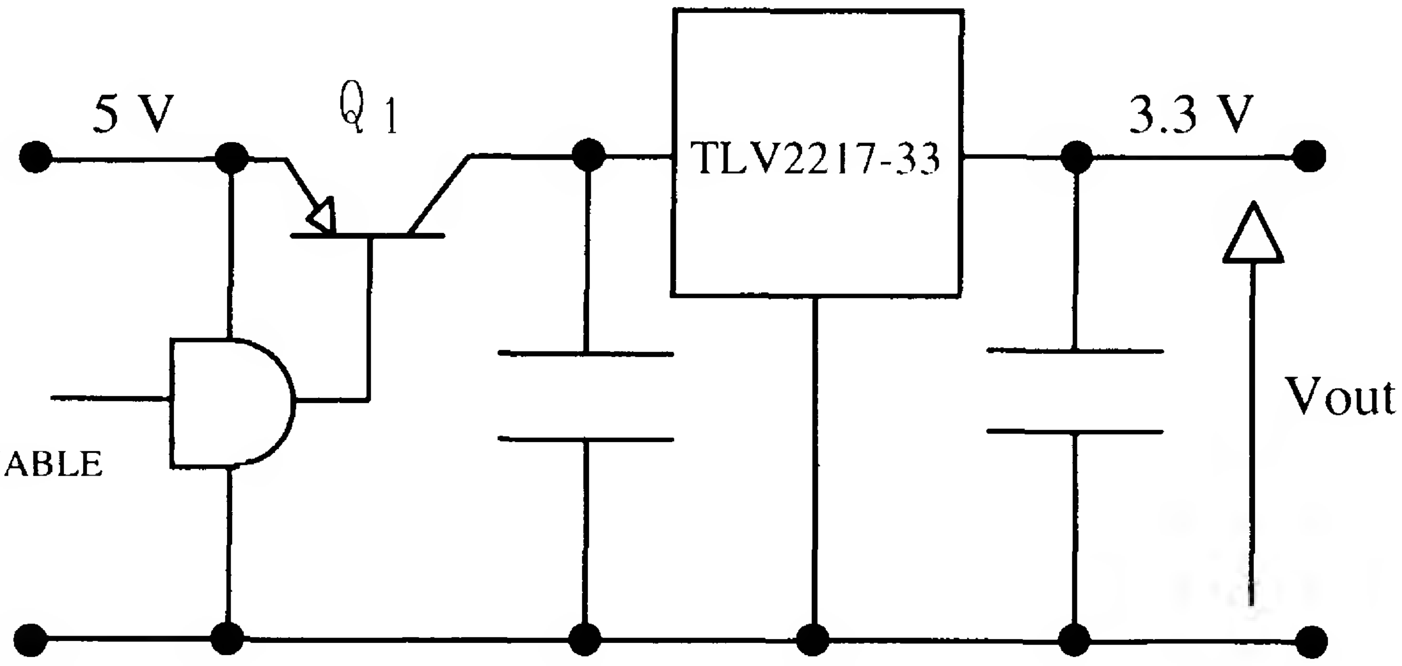


Figure 2.10

Current Boost

To increase the output current capability of the TLV2217-33, a shunt transistor can be used as shown on figure 2_11. The output voltage tolerance which is governed by the LDO will be unaffected, but the output current will increase through the external pass transistor. The value of RB is selected so that Q1 is off when the LDO is operating well within its maximum current output and power dissipation capability. As the current approaches the TLV2217-33's maximum current capability, the current through R_B, is sufficient to generate approximately 0.7V (VBE), and therefore the transistor Q1 starts to conduct, increasing the current capability to the load. The bias current of the transistor must go through the TLV2217-33; this needs to be considered when calculating R_B. Figure 2.10 can be further enhanced by designing in a current limit for Q1. It must also be noted that the inclusion of R_B on the input of the TLV2217-33 will affect the drop-out value of the LDO which will increase from 0.5 V max. to about 1.2 V.

Figure 2.11 has the benefit of keeping the output voltage of 3.3 V ±2% maximum while offering the designer higher levels of output current to meet his system requirements.

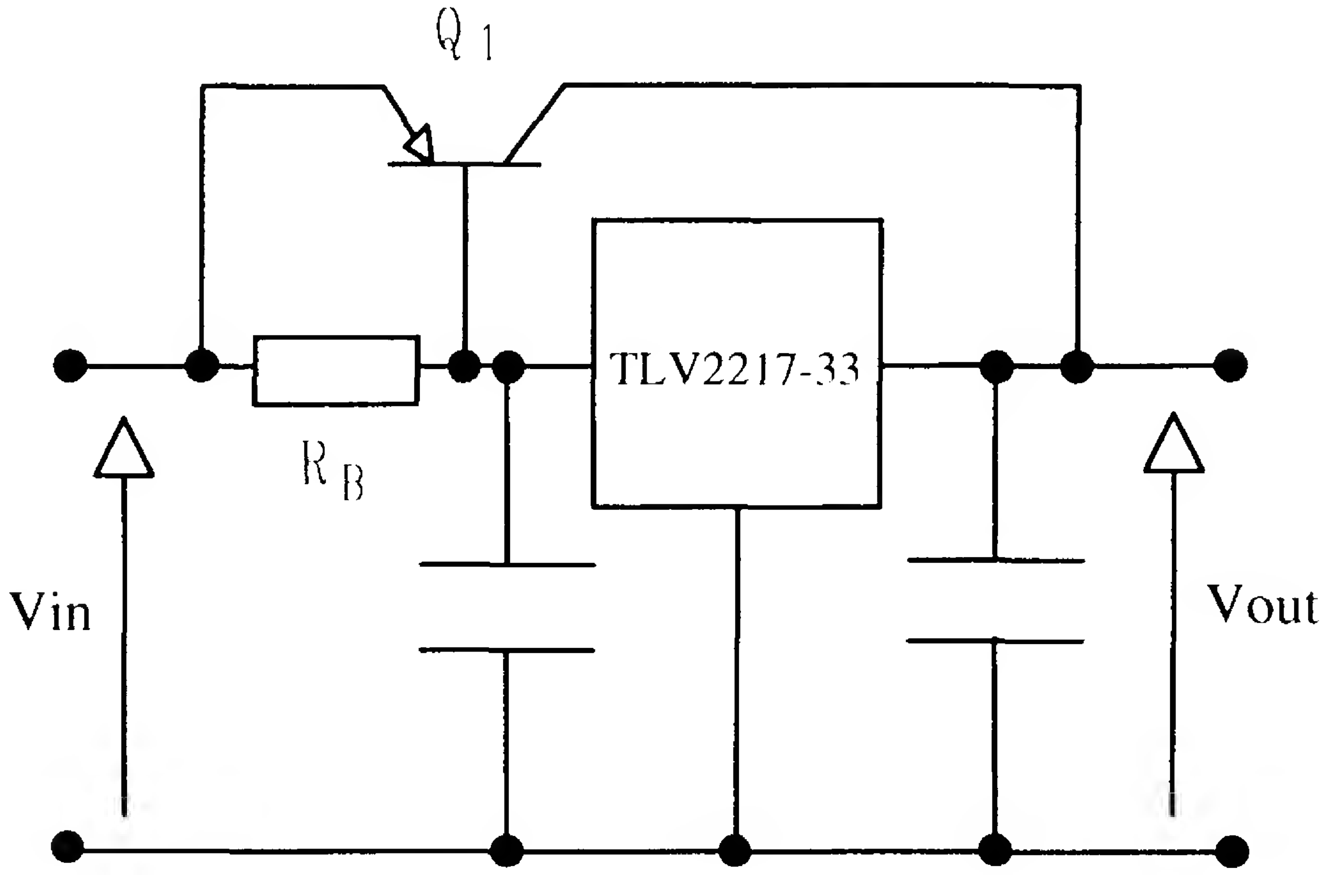
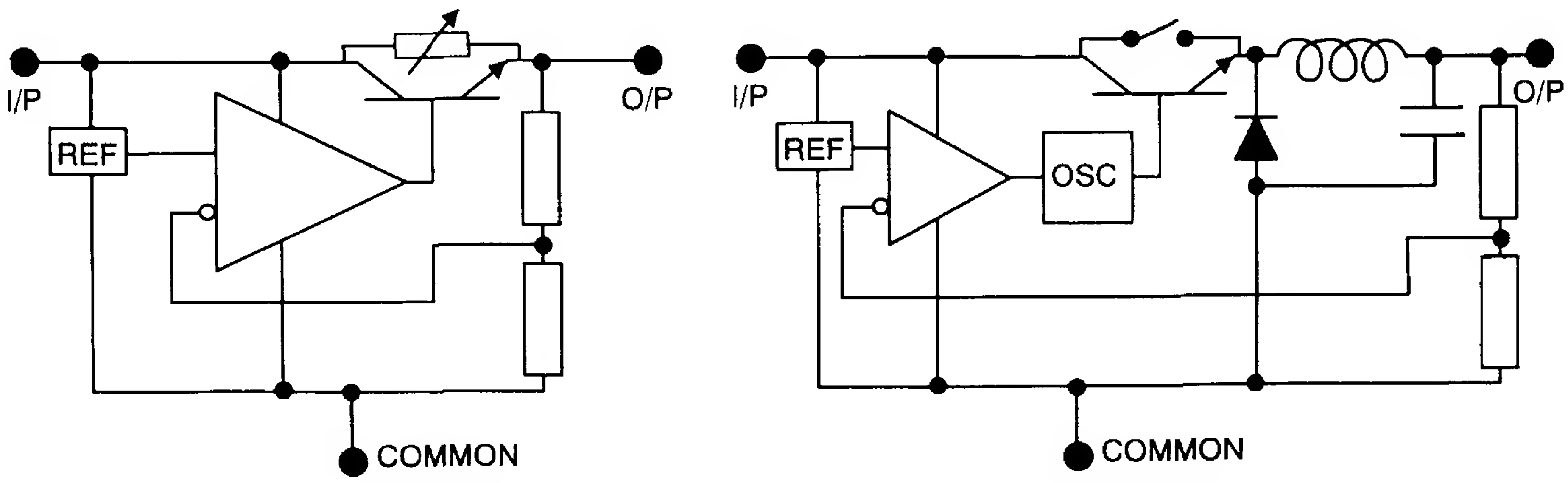


Figure 2.11

3 Switching regulators

In a switching regulator a transistor acts as the control element (as a linear regulator), but it is used in a different way. The control is provided by "chopping" the input voltage to pass energy (½LI^2) which is stored in the inductor from input to output in proportion to the duty cycle.

Switching Regulators



Parameter	Linear Regulator	Switching regulator
Efficiency	Typically 30%	Typically 70% - 90%
Vin - Vout	Small (minimise losses)	Can be large
Power	Low (2 Watts)	High (30 Watts)
Noise	Low (20mV)	High (100mV)

Figure 2.12 - Switching Regulators

Advantages

The primary advantage of this technique is that the active element (the transistor) is either fully saturated or fully off. In both cases the power dissipated in the switch is minimised. Therefore the switching regulator operates at a higher efficiency than its series regulator counterpart. Typically, a switching regulator operates at 70% to 90% efficiency, compared to 30% of a series regulator.

Another benefit of the switching regulator is a decrease in size, weight and hence cost per watt of output power. This is because by operating at a higher duty cycle, the size of the passive components required is reduced by a factor of about 8 times for switchers operating over 100 kHz.

Disadvantages

The major disadvantage of a switching regulator is that they are more complex and require more complicated supporting circuitry. An Inductor is used as the passive component to store charge instead of a capacitor, and inductor design is a complex area. The most common fault with switching regulator design is that the inductor becomes saturated and therefore the output voltage collapses. For this reason some designers steer clear from using switching regulators. The switching process also introduces high frequency (switching frequency) electrical noise on the input and output voltages, and radiates noise from the switching currents in the inductor. The noise generated by the switching regulator will be attenuated to some extent by the filter capacitors on the input and output. As switching frequencies increase, this noise also becomes easier to filter out, but the negative aspect is that the efficiency of the regulator reduces due to greater transition cycles over a period of time. Finally, switching regulators tend to introduce more ripple on the output than linear voltage regulators.

3.1 Switching Regulator Topology

There are four main types of configurations to generate the required output voltage from a switch mode power supply.

3.1.1 Buck (Step-down) Converter

The Buck converter operates by interrupting the current flow through the Inductor to the load and therefore the voltage to the load. This means that the inductor voltage is either Vin or 0 V.

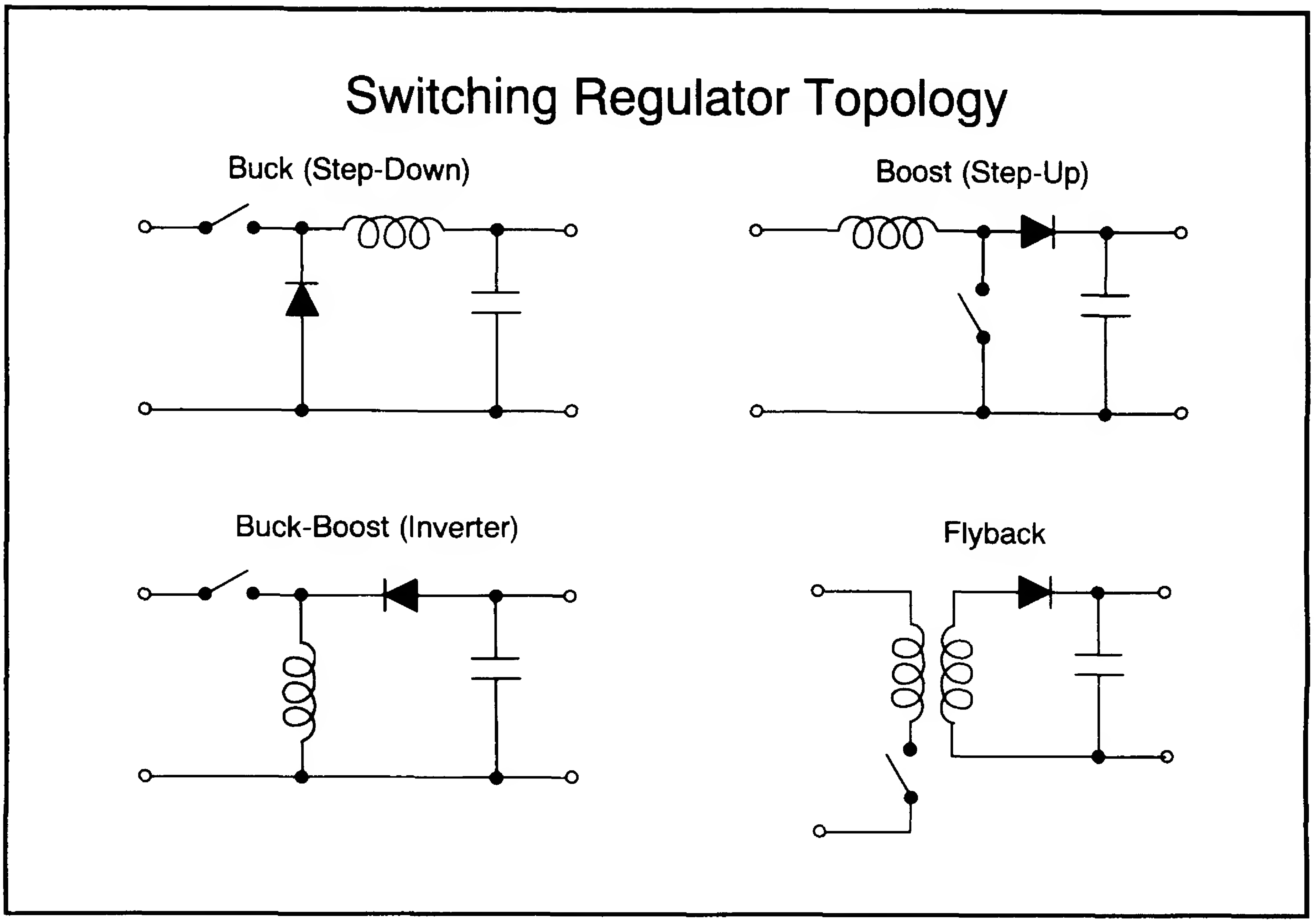


Figure 2.13 - Switching regulator Topology

If a variable duty cycle is applied to the switch, the Inductor and capacitor works as a simple LC filter to create a DC output voltage that will be the average voltage applied to the inductor. From this, a simple formula can be found;

$$V_{OUT} = V_{IN} \bullet \text{Duty Cycle}$$

$$\therefore V_{OUT} = V_{IN}\left(\frac{T_{ON}}{T_{OFF}+T_{ON}}\right)$$

Therefore, Vout can be set to any voltage level which is less than the input voltage by simply controlling the duty cycle of the switch. A higher "OFF" switch time will result in a lower output voltage. If the load current which flows through the diode and the inductor is allowed to drop to Zero when the switch is open, the operation is commonly known as "Discontinuous mode" .If current is still flowing through the inductor when the switch closes, this operation is called "Continuous mode".

3.1.2 Boost (Step-up) Converter

The Boost converter operates by storing energy in the inductor when the switch is closed, and transferring this stored energy to a load capacitor when the switch is open. This configuration allows the output voltage to be set to a greater voltage than the input voltage. When the switch closes, the current in the inductor builds up at a rate determined by the inductance value and the supply voltage. When the switch is opened, the magnetic field in the inductor collapses, causing a reverse voltage that will forward bias the diode and supply its stored energy to the load capacitor.

If the inductor current has decayed to zero during the time that the switch is stayed open, this operation is also commonly known as "Discontinuous Mode" and therefore a relationship of the "ON" and "OFF" time can be found by;

$$I_{L(on)} = I_{L(off)}$$

$$\left(\frac{V_{IN}}{L}\right)\bullet T_{ON} = \left(\frac{V_{OUT}-V_{IN}}{L}\right)\bullet T_{OFF}$$

$$V_{IN}\left(T_{ON}+T_{OFF}\right) = V_{OUT} - T_{OFF}$$

$$V_{OUT} = V_{IN}\frac{T_{ON}+T_{OFF}}{T_{OFF}}$$

$$V_{OUT} = V_{IN}\left(\frac{1}{1-T_{ON}+T_{OFF}}\right)$$

$$V_{OUT} = V_{IN}\left(1+\frac{T_{ON}}{T_{OFF}}\right)$$

3.1.3 Buck-Boost (inverter) Converter

The inverter operates in almost the same way as the Boost converter discussed previously. Energy is stored in the inductor when the switch is closed. However, when the switch is turned off, the energy is transferred through the diode to the load capacitor with a negative amplitude. Notice that in this configuration, the output voltage is only derived from the inductor. This enables the output voltage to be set to virtually any value, regardless of the input voltage.

3.1.4 Flyback Converter

The flyback converter uses the same principle as in the Boost converter in that the current flowing through the inductor is actively switched from the input to ground potential. However, the inductor is now the primary winding of a transformer and therefore the secondary winding is used as the output. In this configuration, the output voltage can be set to any voltage potential, which is dependant on the winding relationship (1:N) between the primary and secondary of the transformer.

3.2 Switching Control Techniques

There are three system configurations that could be used in Switch mode power supplies;

3.2.1 Pulse-Rate-Modulation (PRM).

One early form of PRM switching regulator to be released on to the market was the Texas Instruments TL497. This is an easy to use PRM integrated circuit, and as a result, has proved very successful. The TL497 suffers from the problem, which is common to all PRM controllers, of enormous variation in oscillation frequency with load. At light loads, the frequency can drop into the audible frequency range. More modern Switching Regulators use either Voltage or Current mode Pulse Width Modulation (PWM) Control circuits. PWM control circuits operate at a fixed frequency chosen by the Designer, and the Mark - Space ratio is adjusted accordingly.

3.2.2 Current Mode PWM Control

A more recent innovation in Switching regulators is to use Current Mode Control. This uses a technique of monitoring the current flowing through the power switch which is then used to modulate the on-time of the switching regulator. This in effect uses a dual control loop, with the inner loop being the current control. The current flowing from the input through the inductor and the output power transistor is converted to a voltage by a low value sense resistor. This provides direct feedback of the current flowing through the inductor.

3.2.3 Voltage Mode Pulse Width Modulation Control

With Voltage mode PWM control, the control mechanism is provided by a feedback loop from a sampling element on the output, (usually a potential divider network) which is compared to an accurate internal voltage reference. The difference between the actual and the desired output voltage is then generated by a differential amplifier which produces an error signal (V_{ERR}). This error signal is compared to the oscillator voltage (V_{OSC}) which the result is a switched output (V_{PWM})

The frequency of the oscillator is normally controlled by an external timing capacitor chosen by the user. When ever the magnitude of the voltage ramp exceeds that of the error signal, the comparator output is high, activating the power switch. Similarly, when the ramp is below the error signal, the output is low and the switch is turned off. In this way, a series of pulses of magnitude Vin is passed to the L.C. lowpass filter and hence to the output. The width of these pulses (and hence the duty cycle) is modulated by the error signal. Due to the increasing need to use switching regulators in portable and high density applications, Texas Instruments has developed a range of Voltage Mode PWM control circuits which are suitable for generating accurate output voltages from a single supply voltage source.

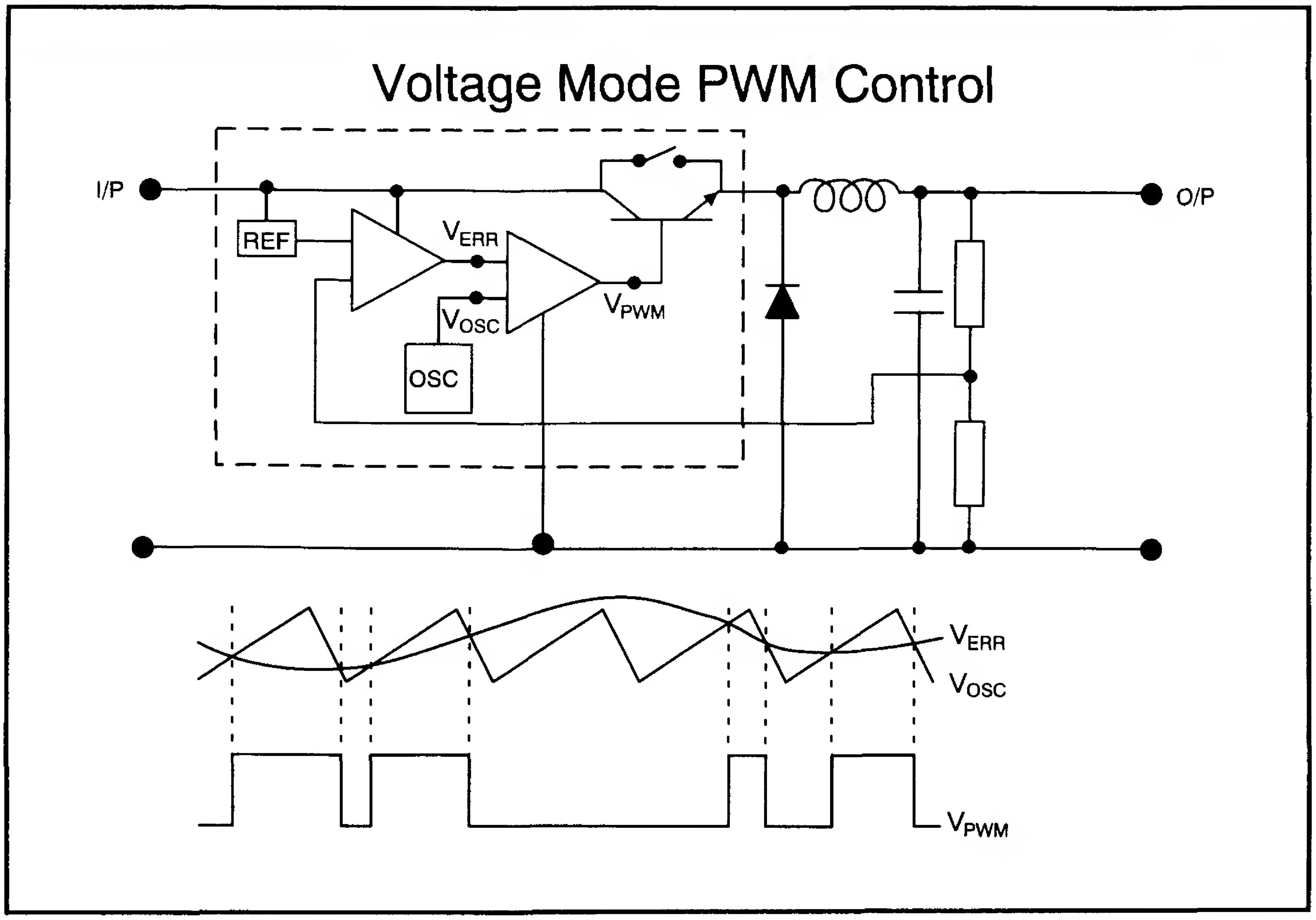
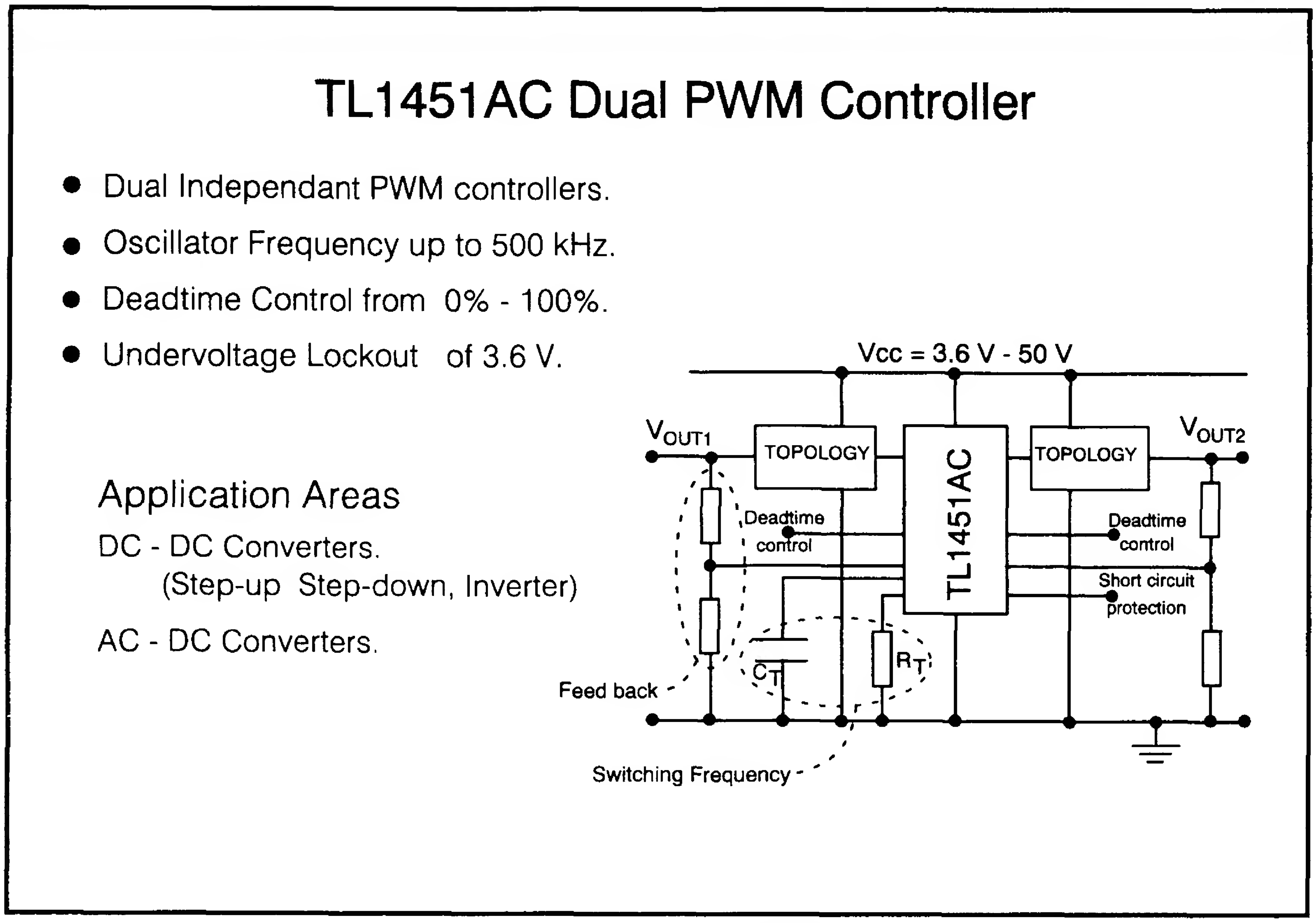

Voltage Mode PWM Control

Figure 2.14 - Voltage Mode PWM Control

3.3 TL1451AC Dual PWM Controller

Many applications require two or more voltages to be monitored independently. The first option is to build the two supplies using one switching controller and a centre tapped transformer. However, only one of the two output voltages can be monitored and is usually the secondary winding that is supplying the most output current. The disadvantage of this is that the unmonitored-supply accuracy is dependent on the coil windings and that if a fault occurred, it might not be noticed by the switching regulator.

The other option is to generate the two supplies using two single switching regulators such as the TL594 or TL598. However, this adds complexity and increases board area. Texas Instruments has a Dual Voltage Mode PWM controller named the TL1451AC that incorporates some features which offer greater control and performance than other PWM controllers currently available.



TL1451AC Dual PWM Controller

- Dual Independant PWM controllers.
- Oscillator Frequency up to 500 kHz.
- Deadtime Control from 0% - 100%.
- Undervoltage Lockout of 3.6 V.

Application Areas

DC - DC Converters.
(Step-up Step-down, Inverter)

AC - DC Converters.

Figure 2.15 - TL1451AC PWM Controller

3.3.1 Dead time Control.

The dead time control is the period of time in each cycle when the PWM control is over-ridden and the output transistors are turned off. This is achieved using another input to the PWM comparator. If the voltage at these pins exceeds that of the oscillator output, the output transistors are switched off irrespective of the error voltage signal. By setting a level between 1.2 V and 2.3 V, the dead time can be controlled from 0% to 100% of the cycle.

This is useful in a push-pull configuration when the outputs operate out of phase with each other on two halves of a centre tapped transformer. In this case, it is essential that there is no time when both outputs are switched on together since this would create a short circuit from the supply rail to ground. Dead time is employed here to ensure that there is no overlap between the two outputs.

Dead time control also provides the means to include a soft start-up capability. Soft start cushions the output at start-up when the large capacitor on the output needs to be charged up. Without it, the error feedback would be very large, forcing the output to be on for 100% of the cycle. With a capacitor tied between the reference pin and the dead time control pin of the TL1451AC, the voltage on the dead time control pin starts at 2.5 V and then decays as this capacitor charges up. In this way the dead time falls from 100% at start up to 10% when the circuit has stabilised.

3.3.2 Undervoltage Lockout

An undervoltage lockout (UVLO) circuit monitors the supply voltage and over rides the operation of the switching regulator if it falls below the minimum of 3.6 V. This ensures that the reference regulator and other circuitry stays within its operating specification and prevents faulty operation of the device. The UVLO operates by adjusting the Dead Time Control to 100% thus turning the output transistors off.

3.3.3 Design Ideas

Texas Instruments has a comprehensive application note to aid in designing with the TL1451AC. The applications note includes three circuit schematics, showing the switching regulator in the Step-Up, Step-down and Inverter configurations.

The application in figure 2.16 shows the TL1451AC in a Buck (step-down) and Buck-Boost (inverter) converter mode. The dead time control voltage is set by the adjustment of VR1 and VR2. The soft start control is governed by C5 and C9. The output voltage is set by the combination of R3 / R4 and R8 / R9. A proportion of the output is fed back to the error amplifier. The oscillator switching frequency is governed by C_T and R_T. The Feedback reference voltage is set by R1 and R2 for the error amplifiers. C2, C3, R7 and C6, C7 and R12 creates a filter for the error amplifiers attenuating any high frequency noise which could cause instability. The remainder of the components are configured as per the "Buck" and "Buck-Boost" topologies.

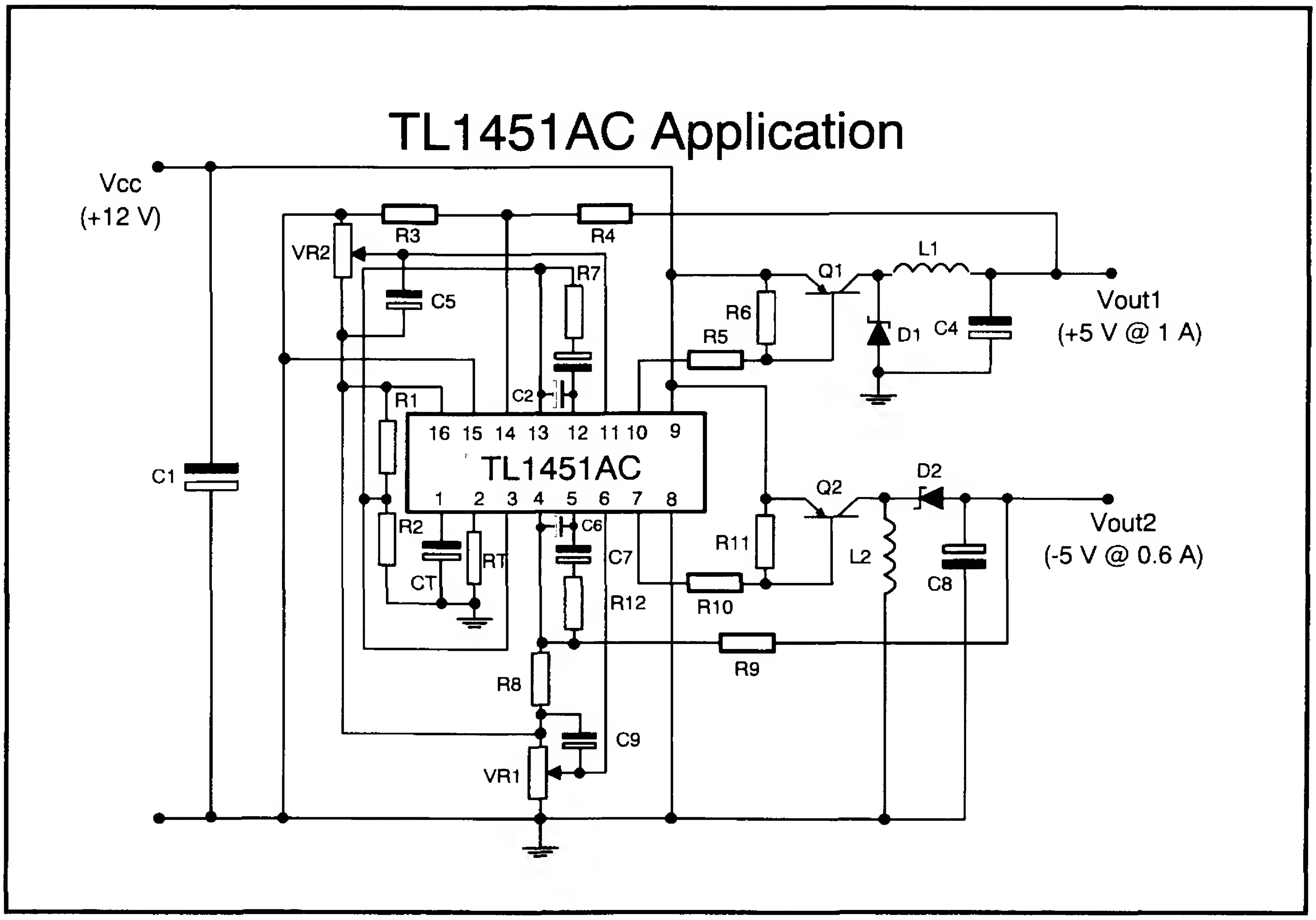

TL1451AC Application
Vcc
(+12 V)
C1
VR2
R3
R4
C5
R7
R6
R5
Q1
L1
D1
C4
Vout1
(+5 V @ 1 A)
C2
R1
16 15 14 13 12 11 10 9
TL1451AC
1 2 3 4 5 6 7 8
R2
CT
RT
C6
C7
R12
R11
R10
Q2
D2
L2
C8
Vout2
(-5 V @ 0.6 A)
R9
R8
C9
VR1

Figure 2.16 - TL1451AC Application

The component list for the Buck and buck-boost is shown below.

Ref	Value	Make	Ref	Value	Make
R1	39 kΩ	¼W Metal Film	C1	100 µF	50-V Electrolytic
R2	39 kΩ	¼W Metal Film	C2	470 pF	Ceramic
R3	4.7 kΩ	¼W Metal Film	C3	150 pF	Ceramic
R4	15 kΩ	¼W Metal Film	C4	1000 µF	25-V Electrolytic
R5	470 Ω	¼W Metal Film	C5	0.47 µF	10-V Electrolytic
R6	470 Ω	¼W Metal Film	C6	470 pF	Ceramic
R7	130 kΩ	¼W Metal Film	C7	150 pF	Ceramic
R8	4.7 kΩ	¼W Metal Film	C8	1000 µF	25-V Electrolytic
R9	24 kΩ	¼W Metal Film	C9	0.47 µF	10-V Electrolytic
R10	47 Ω	¼W Metal Film	C10	0.47 µF	10-V Electrolytic
R11	18 Ω	¼W Metal Film	CT	2.2 nF	Ceramic
R12	130 kΩ	¼W Metal Film			
R13	220 kΩ	¼W Metal Film	D1	MBR150	1A Schottky Diode
RT	18 kΩ	¼W Metal Film	D3	MBR150	1A Schottky Diode
VR1	47 kΩ	Linear Carbon preset	L1	220 µH	3.5 A, 0.106 Ω
VR2	47 kΩ	Linear Carbon preset	L2	220 µH	3.5 A, 0.106Ω
Q1	TIP30B	Ic=1A, PNP			
Q2	TIP30B	Ic=1A, PNP			

Table 2.01

4 Supply Voltage Supervisors

In the previous two sections, we have explored two different ways to generate a regulated power supply by either using a Linear or a switch mode regulator. Although these methods offer protection like output current limit protection, under-voltage lock-out and so forth,. faults can still occur on the input to the PSU which will affect the output performance of the regulator and hence the supply to the system. In an analogue system, variations in the supply can affect the performance of the signal to noise ratio and the dynamic range of the system. However, in a digital system where the supply voltage window is stipulated to be 5 V ± 5% tolerance level to guarantee its operation, any power supply variation caused by either an undervoltage or overvoltage condition outside the specified window may cause unpredictable erroneous data to be produced.

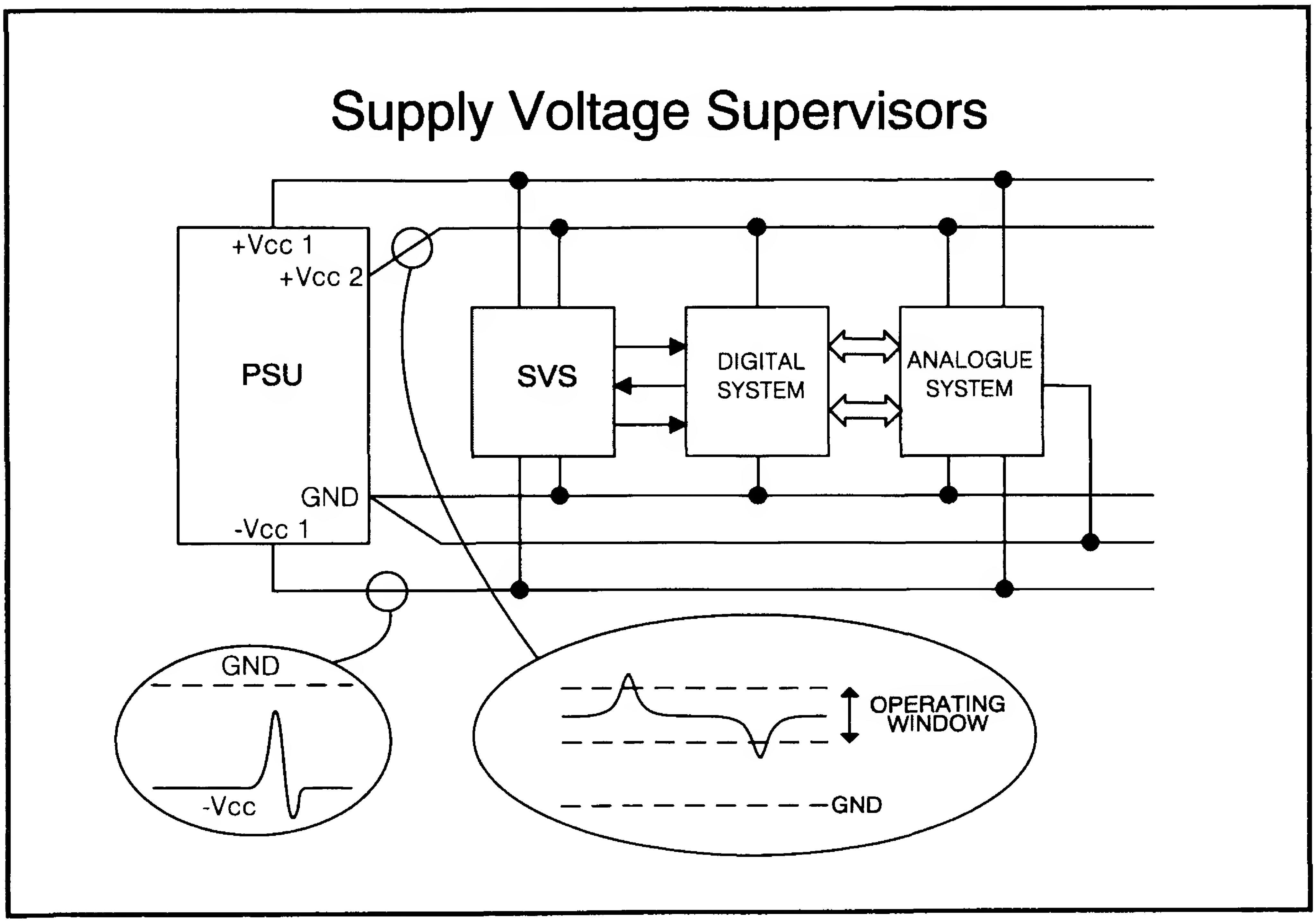
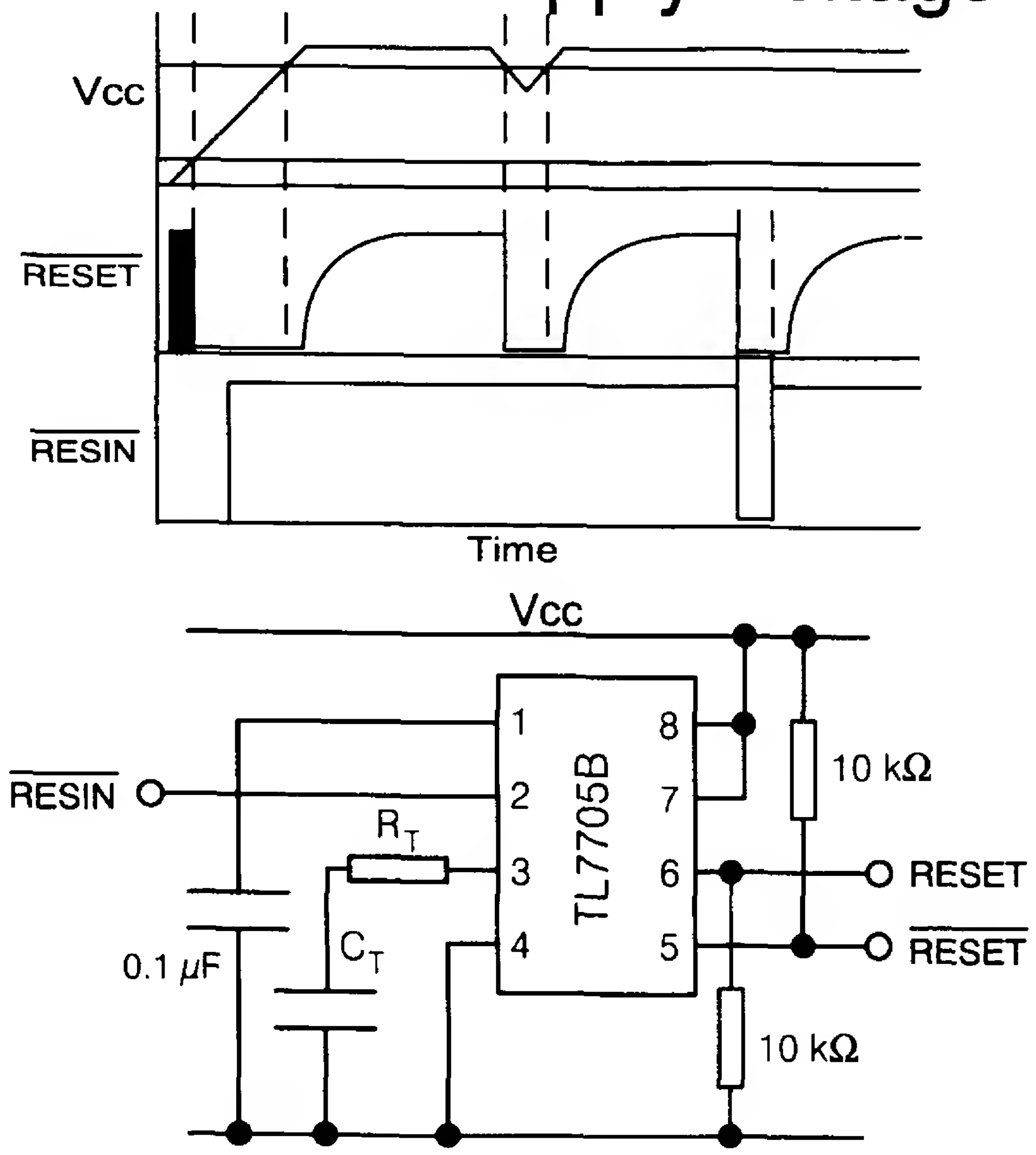


Figure 2.17 - System Supply Voltage Supervision

A power supply fault can affect any of the digital bits from the MSB to the LSB and therefore could change the output by a factor of 2. The undervoltage condition is the most common since each time the power supply is turned on, the output voltage takes time to settle to its required value and therefore the digital system will be powered up before the supply has settled within its designed window. Linear Regulators for example can normally cope with an increase in supply voltage, but when the supply falls below the drop-out voltage of the regulator, the output from the regulator generally tracks the input voltage, causing a negative spike on the output to occur. This is commonly known as an undervoltage fault condition.

Supply Voltage Supervisors


Vcc
$\overline{\text{RESET}}$
$\overline{\text{RESIN}}$
Time
Vcc
$\overline{\text{RESIN}}$
R_T
0.1 µF
C_T
1
2
3
4
8
7
6
5
TL7705B
10 kΩ
RESET
$\overline{\text{RESET}}$
10 kΩ

Device	Supply	Tolerance
TL7702A	Prog.	1%
TL7705A	5 V	
TL7709A	9 V	
TL7712A	12 V	
TL7715A	15 V	
TL7702B	Prog.	
TL7705B	5 V	
TL7757	5 V	2.6%
TL7759	5 V	
TL7770-5	5 V + Prog.	1%
TL7770-12	12 V + Prog.	
TL7770-15	15 V + Prog.	

Figure 2.18 - Supply Voltage Supervisors

The function of a Supply Voltage supervisor (SVS) is to monitor the supply voltage to a system and to flag the micro processor through its enable / disable facility if the supply goes out of its defined operating window. The supply voltage supervisor can also be used to ensure that a digital system is powered up correctly by applying a reset to the system until the supply has stabilised. In this function, the supply voltage supervisor must have an output which is defined for very low supply voltages for obvious reasons.

4.1 TL7702B and TL7705B

Texas Instruments pioneered the monolithic SVS with the introduction of the TL77XXA family of SVS's. Texas Instruments released the TL7702B (programmable) and TL7705B (fixed 5 V). The TL770XB have complementary positive and negative reset outputs which gives them greater flexibility in interfacing to a number of reset and enable pins associated with various microprocessors for example. The outputs are "open collector" which allows coupling to microprocessors which use bi-directional control. The RESET output is active high whereas $\overline{\text{RESET}}$ is active low in the fault condition. An external capacitor C_T can be used to programme a delay between the "fault to no-fault" (V_{T+} Threshold) condition and reset outputs being de-activated. This ensures that the supply voltage has fully stabilised before the reset system is removed. The TL770XB family also has an external reset facility named $\overline{\text{RESIN}}$, which when pulled low will discharge V_{CT} and place the outputs in the fault condition. This can be simply configured as a "System Reset" by using an external switch.

4.1.1 Difference between the "A" and "B" version.

The TL7705B and TL7702B offers a marked improvement in performance over the existing TL77XXA versions.

The TL7702B and TL7705B has a defined RESET and $\overline{\text{RESET}}$ output with a supply voltage of only 1 V. This ensures that there is no possibility of errors occurring in the system during power-up since the general minimum high level control voltage for digital is 2.4 V. The TL77XXA family's output is only defined with a supply voltage of greater than 3.6 V. As digital electronics move to supply voltages that can either be 3 V or 5 V, this parameter will become increasingly important.

The TL7702B and TL7705B offers significant increases in output switching speeds compared to the TL77XXA family. For example, the rise and fall times of the "B" version is in the range of 50 ns - 200 ns where as the "A" version offers a switching speed in the range of 200 ns - 350 ns. With the increase in switching speeds, the propagation delay of the TL7702B and TL7705B has also been significantly reduced from 1.5 µs (typical) for the TL77XXA, to 270 ns (typical) for the TL7702B and TL7705B. This offers a marked increase in system response to faster transients on the supply and reduces the possibility of noise on the supply causing miss-triggering due to slow response times through the threshold voltage.

Figure 2.19 shows the typical rise time for the TL77xxA and TL770XB devices with various pull-up resistors. It can be seen from the graph that as the pull-up resistance reduces, the rise time also reduces. However, with the TL77XXA family, with pull-up resistance's of less than 2 kΩ will see a marked increase in the rise time of the device. Therefore the TL7702B and TL7705B are ideally suited to systems which require high output currents for resetting.

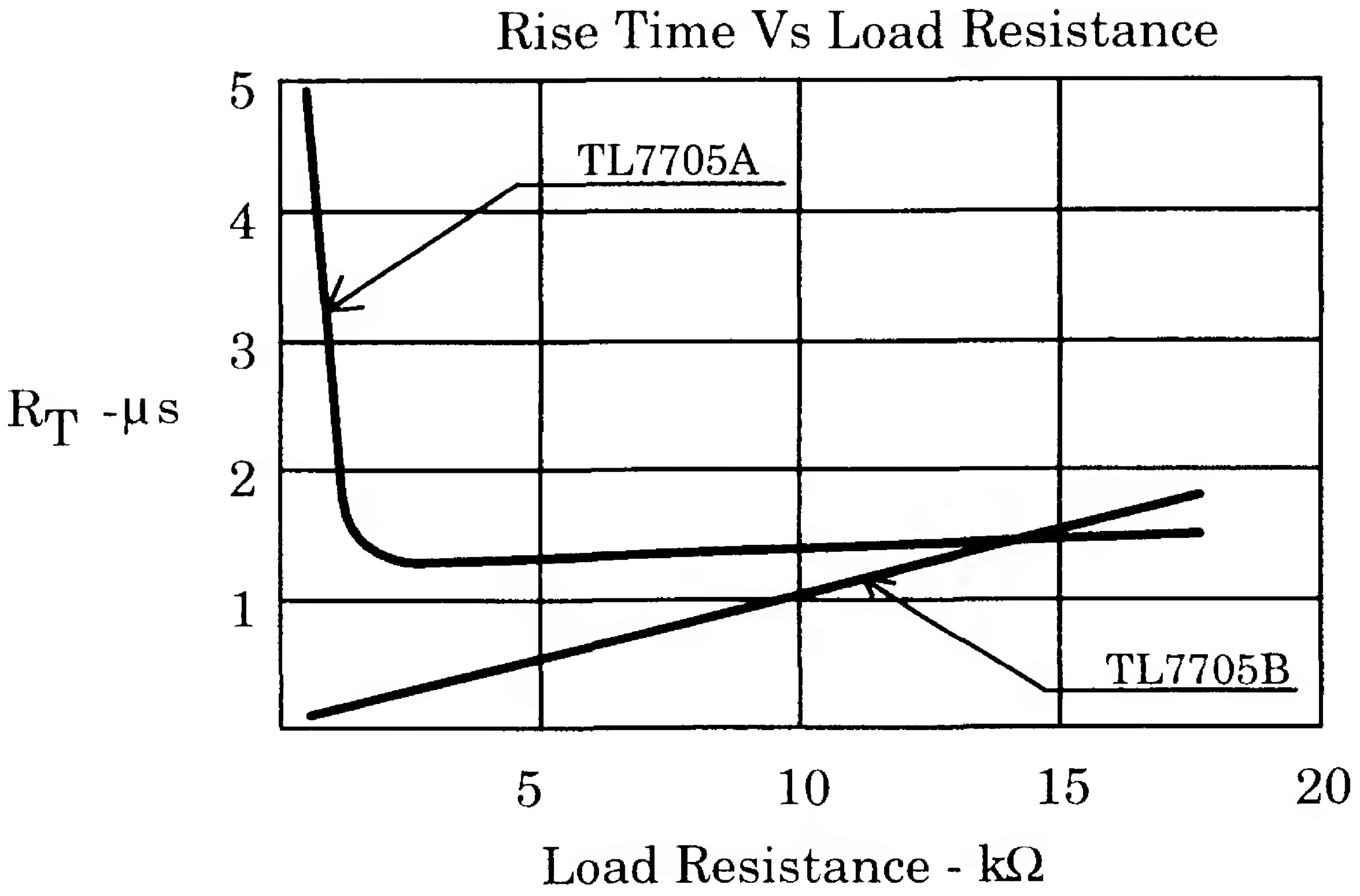


Figure 2.19

Both of the devices are pin to pin compatible which allows the designer to enhance the performance of existing applications by simply replacing the "A" version products with the "B" version.

4.1.2 Why the use of R_T for the TL770XXB and TL7770-XX

Texas Instruments recommends using an external resistor R_T to ensure accurate operation of the device. The TL7702B and TL7705B could erroneously indicate a fault (outputs will be driven active) if the C_T pin is driven more positive than the V_{CC} pin. At first glance of the circuit, this would not be expected to occur in a typical application because the C_T pin is normally connected to an external timing capacitor. During normal operation (no fault condition), the timing capacitor is charged by the on-board current source. The capacitor C_T will be charged to approximately V_{CC} or to an internal voltage clamp (7.1 V zener) whichever is less. If the circuit is then exposed to an under voltage fault condition where V_{CC} is slewed rapidly down, the voltage on the C_T pin will exceed that on the V_{CC} pin. This forward biases a "sneak path" internally which falsely activates the outputs. A fault will be indicated when V_{CC} drops below V_{CT}, not when V_{SENSE} falls below V_{T}-. This does not have any adverse effects on the reliability of the device.

It has been found that 1.4 mA must be forced into the C_T pin to trigger this false reset. The device is 100% tested to ensure that the outputs do not switch with 1 mA forced into the C_T pin. One proven way to eliminate this behaviour is to add a series resistor between the capacitor and pin 3. This will change the duration of the reset pulse, but not by a significant amount. The resistor extends the discharge of C_T, but also skews the V_{CT} threshold. These two effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent on the duration of the supply voltage fault condition.

The Calculation of R_T is shown below. (V_T-) is the lesser of the supply voltage (Vcc) and the internal clamp voltage of 7.1 V. The negative going threshold voltage (V_T-) is subtracted from V_I and then divided by the maximum allowable current (1 mA) in to pin C_T which will not cause a miss-trigger.

$$R_T \geq \frac{(V_I) - (V_T -)}{1 \text{ x } 10^{-3}}$$

The time delay is also affected by the inclusion of R_T within the circuit. The new time delay (t_d) can be calculated as follows:-

$$t_d = \frac{1.3 - \left(1\text{x}10^{-4} \bullet R_T\right)}{1\text{x}10^{-4}} \bullet C_T$$

4.1.3 Design Ideas

4.1.4 Negative Supply Control

The feedback/shutdown of LT1054 (pin 1) can be controlled via the TL7702 supply voltage supervisor. Due to the power up and power down characteristics of the LT1054, the addition of the TL7702 will ensure that the output voltage of the LT1054 will be between -5 V ±5% at all times. This is accomplished by setting the reference of the TL7702 to approx. 4.5 V, thus when the supply voltage is below this threshold voltage, the output open collector of the TL7702 is held low. This in turn will hold the FB / SD pin low. which places the LT1054 into the shut-down mode. When the LT1054 is in this mode, the reference/regulator is turned off and the switching stops. The quiescent current in the shutdown mode drops to approximately 100 µA. When the system supply voltage increases above 4.5 V, the output of the TL7702 is driven high (or in this case open circuit) and the LT1054 fires up to produce the -5 V supply that is required.

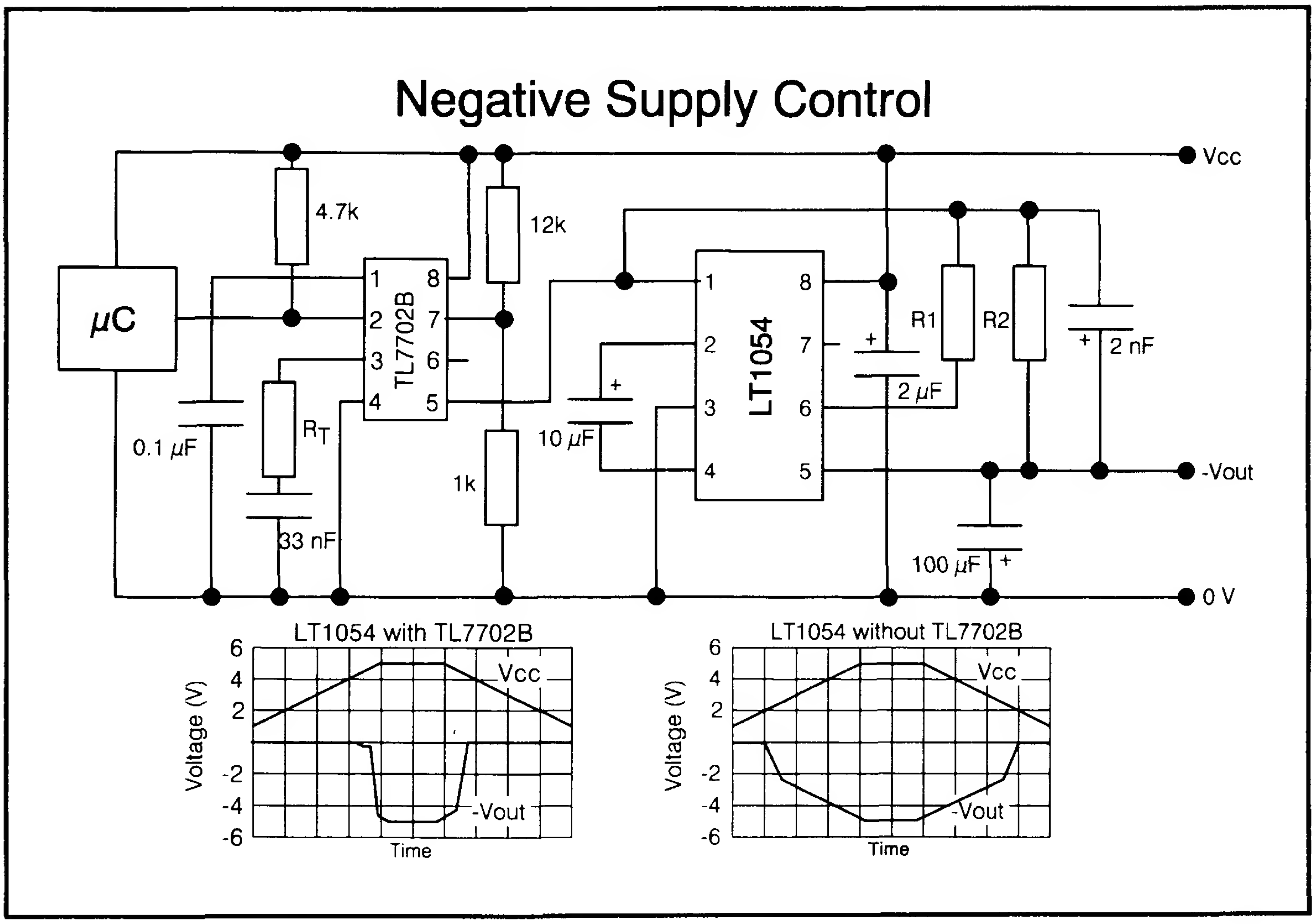

Negative Supply Control
µC
4.7k
12k
TL7702B
1
2
3
4
8
7
6
5
RT
0.1 µF
33 nF
1k
10 µF
LT1054
1
2
3
4
8
7
6
5
2 µF
R1
R2
2 nF
100 µF
Vcc
-Vout
0 V
LT1054 with TL7702B
LT1054 without TL7702B
Voltage (V)
6
4
2
-2
-4
-6
Vcc
-Vout
Time

Figure 2.20 - Negative Supply control

The circuit has been designed so that the negative rail can be powered up independently when required. This has been accomplished by connecting $\overline{\text{RESIN}}$ to a micro controller or a mechanical re-start switch. This will then enable the designer to power up the negative supply rail only when required, thus potentially saving on system power.

4.2 TL7770-XX

An increasing requirement of many new systems is the ability to monitor multiple supply rails. A typical application would be in a computer system where three voltage supplies are required. The microprocessor requires 5 V, but RS232 for the printer drivers and receivers require ±12 V. The multiple supply rails should be monitored to ensure that each part of the system is powered up and operating in the correct voltage window.

Another area which is expanding rapidly is mixed supply applications in digital systems where both 5 V and 3.3 V are used. The TL7770-XX family was designed for these mixed supply applications. Each member of the family is a dual SVS with inputs to monitor both under voltage (1VSU and 2VSU) and over voltage (1VSO and 2VSO) on each of the two channels.

Undervoltage

The TL7770-XX's 1VSU has an internal resistor network which makes the voltage supervisor switch when the supply voltage is greater than the pre-set voltage. The second undervoltage sense pin (2VSU) is programmable and therefore an external resistor network can be used. The external resistor values of R1 and R2 can be found from the following formulae;

$$R_1 = \frac{R_2(V_{CC} - VSU)}{VSU}$$

Where VSU is the under voltage threshold level which is typically 1.5 V. V_{CC} is the supply voltage at which the designer wants the supervisor to switch the outputs. The optimum resistance values can be found with the ratio of R_1 and R_2 known. The undervoltage fault condition is similar to the TL770XB family in that two open collector outputs (RESET and $\overline{\text{RESET}}$) are available.

Overvoltage

As digital electronics become less tolerant to over voltage conditions, the TL7770-5 supply voltage supervisor has the facility for this also to be monitored. Two Programmable over voltage pins are assigned to the TL7770-5 (1VSO & 2VSO). When the supply voltage passes through the over voltage threshold level, the SCR Drive output is taken active high. An SCR triac could be controlled from this pin which would then be used to short out the supply rails through a low "dummy" load thus blowing the power supply fuse. Since the SCR pin is active high and capable of sourcing current, this pin could also be used to drive a NPN transistor or as an over voltage system flag pin.

4.2.1 Design Ideas

3.3 V and 5 V Systems Protection

During the transition from 5 V to 3.3 V supply voltages, designers are faced with the challenge of integrating the two voltage levels and combining the new lower power, high speed 3.3 V logic chips with existing 5 V products in their new designs. These mixed mode circuits dictate the need for multiple supply rail supervision. Figure 2.21 shows a simple way to monitor both 5 V and 3.3 V power supplies and to generate separate RESET signals when either supply experiences an under or over voltage fault.

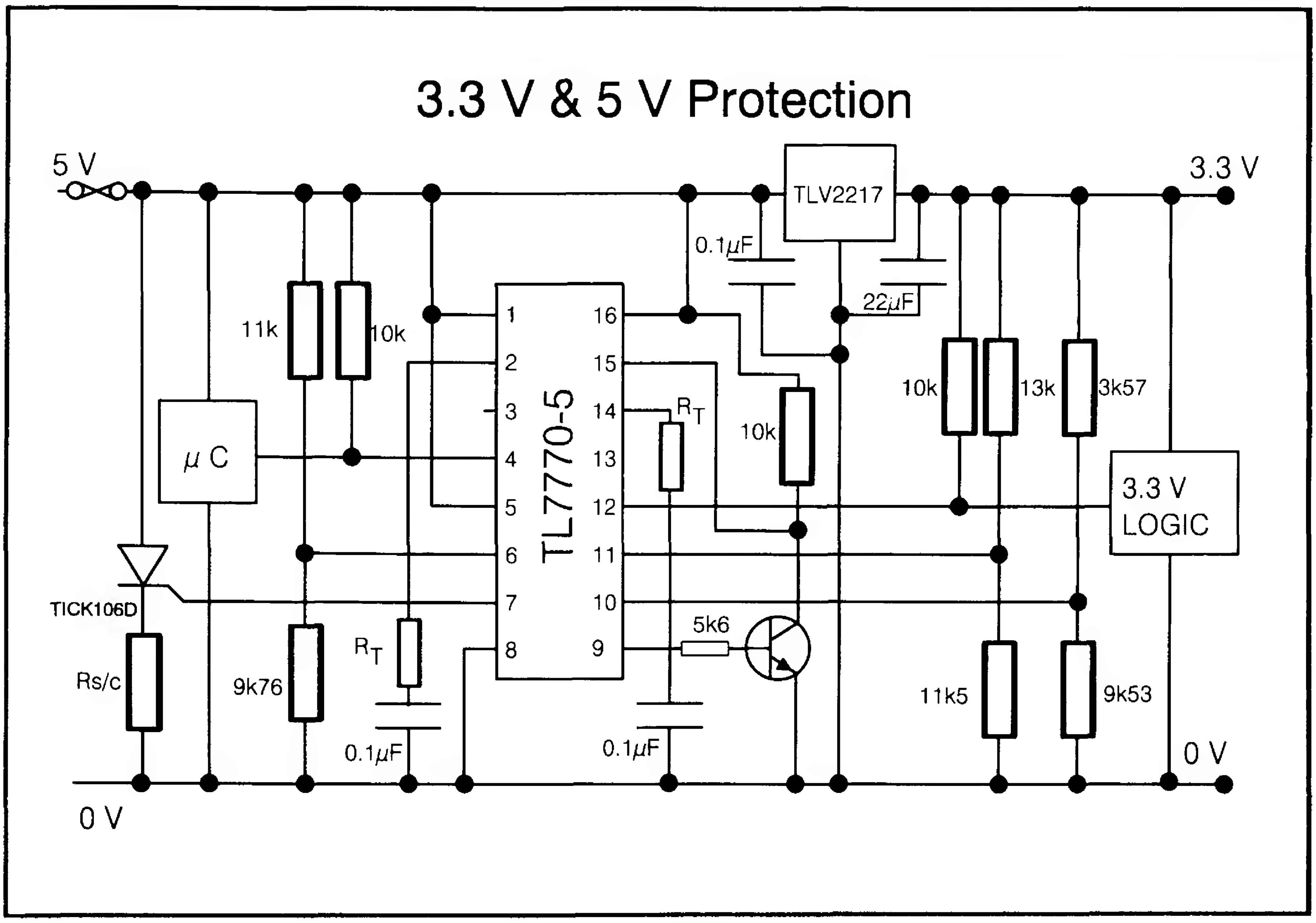


Figure 2.21 - 3 V and 5 V Supply supervision

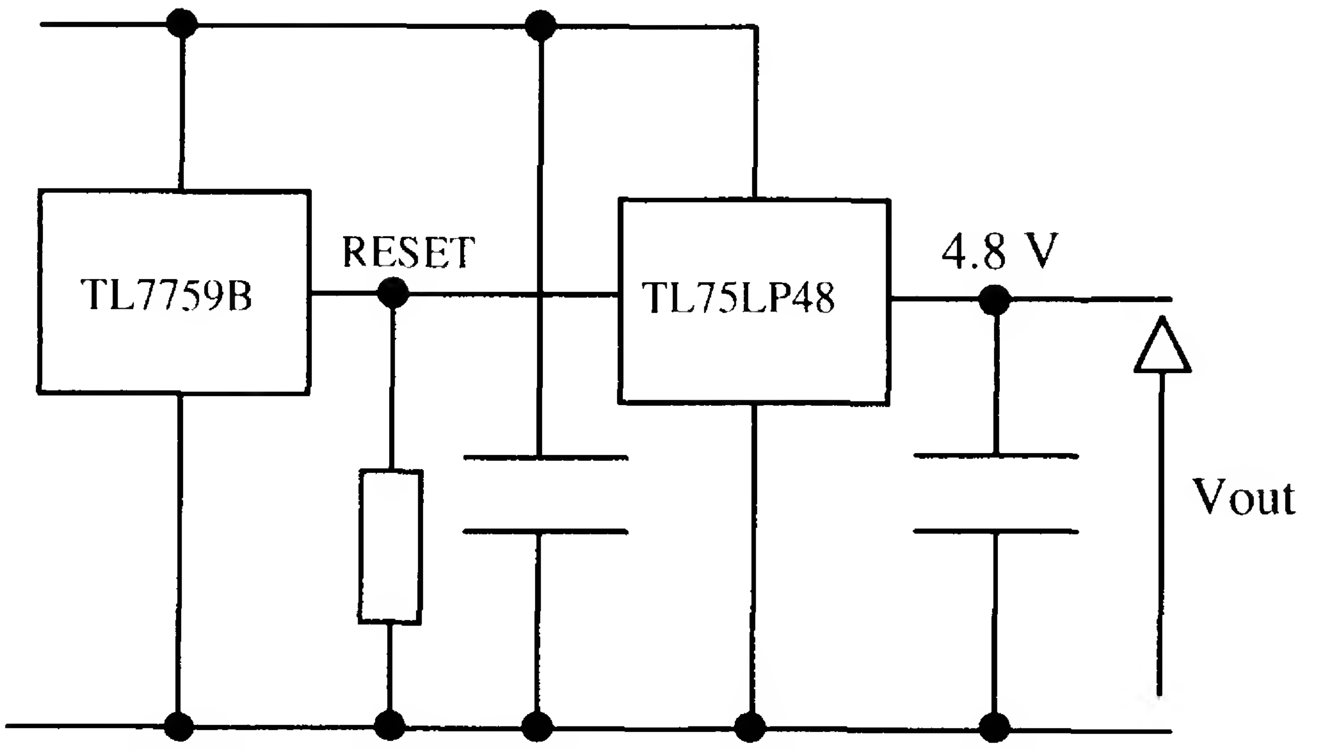
The TL7770-5 features a 5 V pre-set under voltage (1VSU) supervisor and a programmable under voltage (2VSU) supervisor. It also features two overvoltage sense inputs. During power-up, the active low $\overline{\text{RESET}}$ outputs are guaranteed low after V_{CC} reaches 1 V. When the voltage on 1VSU passes through the threshold voltage of 4.55 V, a time delay is initiated, after which the RESET outputs are de-activated. During an undervoltage condition, when 1VSU again drops below 4.55 V, the 1RESET and $\overline{\text{1RESET}}$ are immediately asserted, and remain so for a period of time after the undervoltage condition expires. The over voltage (1VSO) monitoring the 5 V supply has been designed to switch a triac on which will blow the 5 V supply fuse if the supply voltage exceeds 5.5 V. The overvoltage (2VSO) monitoring the 3.3 V supply will pull $\overline{\text{RESIN}}$ low if the supply voltage exceeds 3.5 V. This will activate the reset outputs and flag the 3.3 V logic system.

4.3 TL7757 & TL7759

As low powered battery equipment becomes more and more popular, a need arises to reduce the typical supply current of 1.8 mA of the TL7705 family. In response to this, Texas Instruments has designed two new supply voltage supervisors, the TL7757 and the TL7759. These have a low standby current of just 40 µA max. and are designed for 5 V power supplies. The major difference between the two is that the TL7757 has only one $\overline{\text{RESET}}$ output, where as the TL7759 has two (RESET and $\overline{\text{RESET}}$) outputs. These devices do not require any timing capacitors or resistor divider networks, only a pull-up / pull-down resistor for the open collector output(s). This reduces the system complexity and saves on valuable board space in portable, battery operated equipment.

4.3.1 Design Ideas

The following applications are not intended to document the specific design of a circuit, but rather to generate ideas in the minds of Engineers and Engineering Managers.



Enable regulator controlled with an SVS.

Figure 2.22

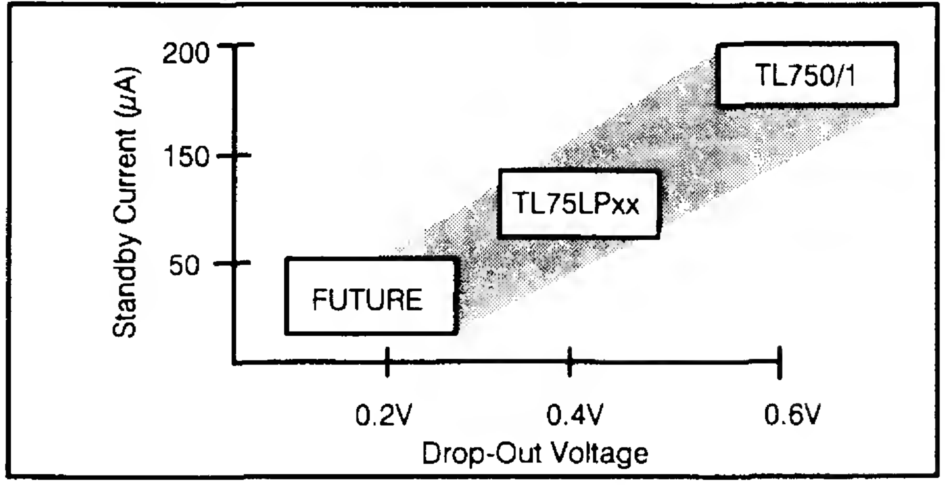
With the supply voltage below 1 V, the reset output is undefined. Once the input voltage passes the 1 V voltage reset (Vres) threshold voltage, the reset output will be pulled high (active high). The TL75LP48QPWLE enable pin is TTL compatible and therefore will place the regulator into its standby mode. As the supply voltage passes through the "turn on" threshold voltage (V_{T^-}) of 4.55 V, the reset will be pulled low which will turn the regulator on and provide a fixed output voltage. This circuit eliminates the problems encountered with the high start-up currents that are associated with Low Drop-out voltage regulators.

5 Summary

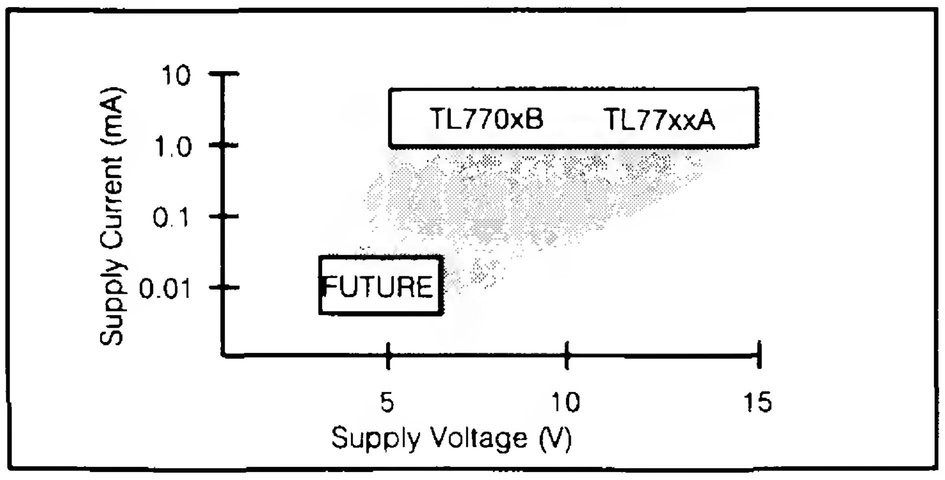
Texas Instruments is investing a high percentage of resource in product design to provide components which will be required in the future for battery powered and power conscious systems. For example, Texas Instruments is committed to providing even lower dropout voltages, standby and quiescent currents for linear regulators which the battery and portable markets require. Coupled with this, design engineers are concentrating on providing a new family of supply voltage supervisors and switching regulators which will offer lower supply and standby currents, higher switching speeds and more integration with smaller package options.

Future Trend & Developments

Low-Drop-Out Regulators



Supply Voltage Supervisors



- Focus on reduced power consumption
  - Lower drop out voltage
  - Smaller bias currents
  - Lower standby current
- Increased functionality
  - On chip supervision
- Reduced supply voltage to 3 volt operation
- Reduced power consumption
- Smaller packages e.g. TSSOP and beyond

Figure 2.22 - Future Trend & Development

Section 3
Data Conversion

Section Contributions by:
John Walliker of UCL
Julian Daley of UCL
Elwyn Davies
Dave Cox
Edited by: Dave Cox

TEXAS
INSTRUMENTS

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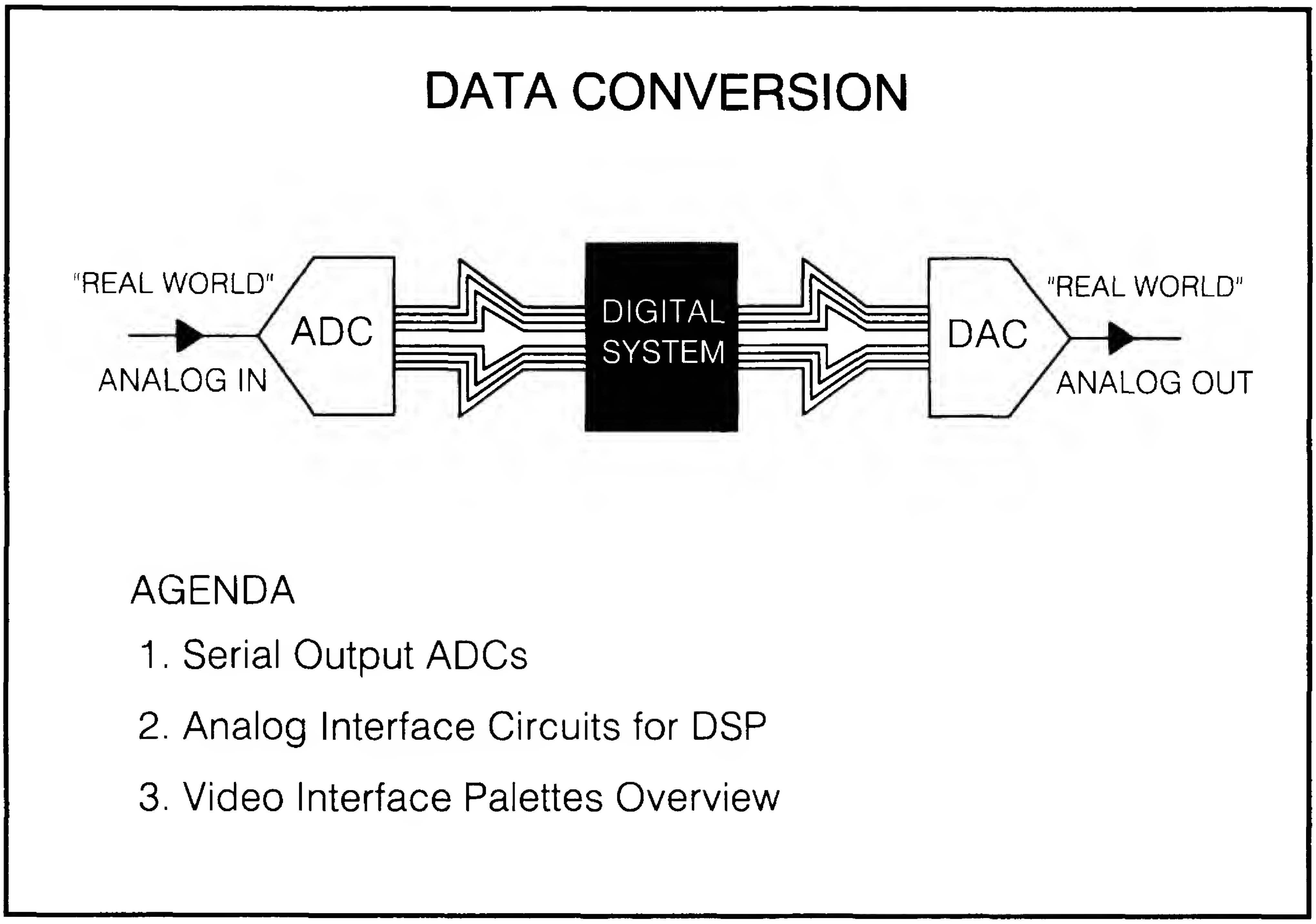
1 Introduction



DATA CONVERSION

AGENDA

1. Serial Output ADCs
2. Analog Interface Circuits for DSP
3. Video Interface Palettes Overview

Figure 3.1 - Data Conversion

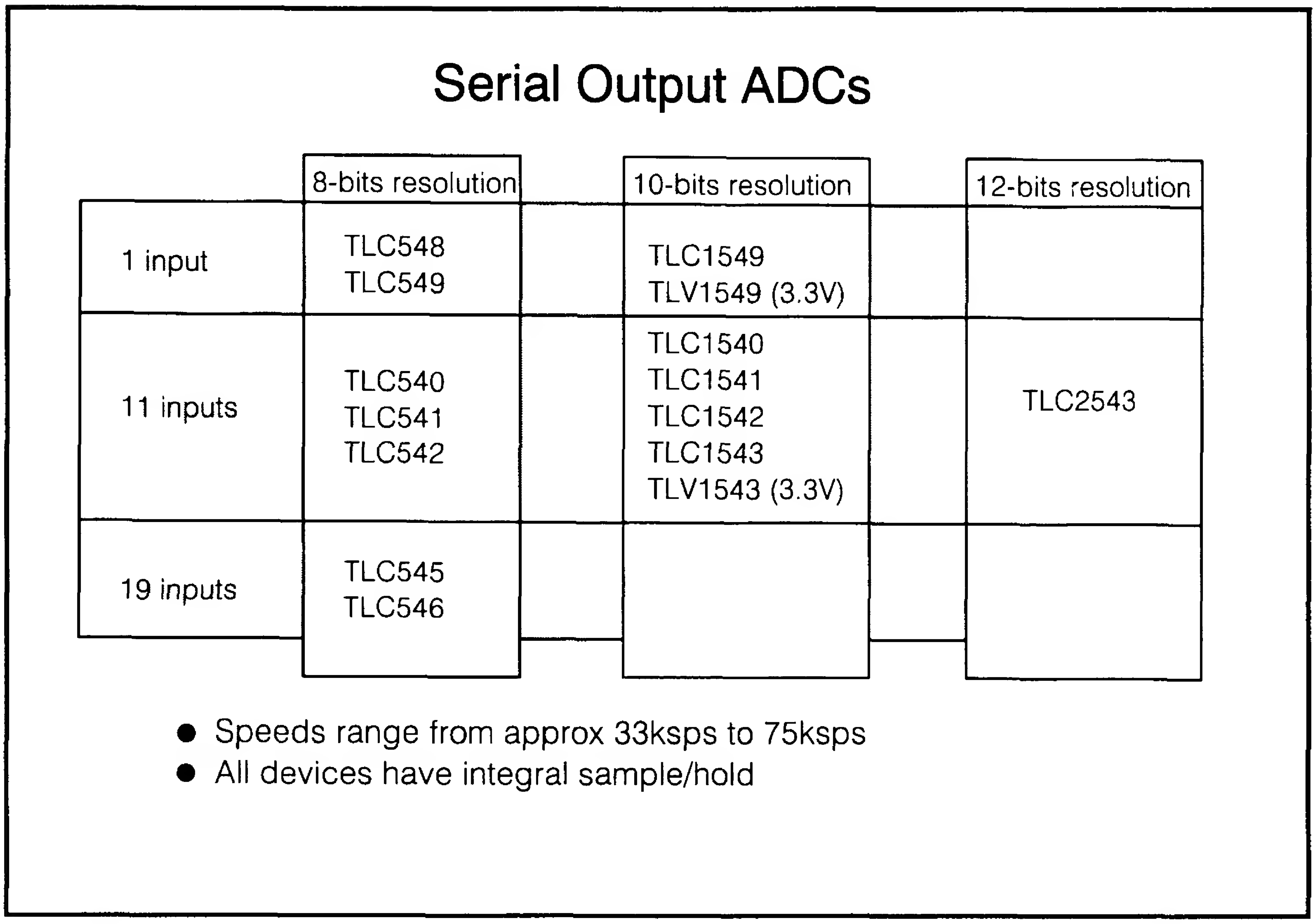
The Data Conversion section of the seminar concentrates on two families of data converters. They are serial output Analog to Digital Converters (ADCs) and Analog Interface Circuits (AICs).

Detailed applications information describing how to interface serial output ADCs to various microcontrollers and how to interface AICs to the serial port of TI's DSPs is discussed. In addition, the interface of these devices to real world analog signals and the maintenance of the required accuracy and dynamic range is described.

A brief overview of Video Interface Palettes completes the section.

2 Serial Output ADCs

2.1 Overview



Serial Output ADCs

	8-bits resolution	10-bits resolution	12-bits resolution
1 input	TLC548 TLC549	TLC1549 TLV1549 (3.3V)	
11 inputs	TLC540 TLC541 TLC542	TLC1540 TLC1541 TLC1542 TLC1543 TLV1543 (3.3V)	TLC2543
19 inputs	TLC545 TLC546		

- Speeds range from approx 33ksps to 75ksps
- All devices have integral sample/hold

Figure 3.2 - Serial Output ADCs Overview

TI produces a family of serial output ADCs offering 8, 10 and 12-bit resolution. There are versions available with 1, 11 and 19 analog inputs. In addition to the standard 5-V supply operation, some of the devices are specified for 3.3-V supplies and 2 parts are specified for 3V to 6V operation.

All these devices use the switched capacitor successive approximation method of conversion and consequently they have an integral sample-and-hold.

Figure 3.3 presents a selection guide for this family of ADCs.

Serial Output ADC Selection Guide

DEVICE	BITS	T_{CONV} (us)	No. OF INPUTS	TOTAL UNADJUSTED ERROR	INTERNAL SYSTEM CLOCK	MAX I/O CLOCK (MHz)	POWER SUPPLY VOLTAGE
TLC548	8	17	1	± 0.5 LSB	YES	2.048	3 - 6
TLC549	8	17	1	± 0.5 LSB	YES	1.1	3 - 6
TLC540	8	9	11	± 0.5 LSB	NO	2.048	5±10%
TLC541	8	17	11	± 0.5 LSB	NO	1.1	5±10%
TLC542	8	20	11	± 0.5 LSB	YES	1.1	5±10%
TLC545	8	9	19	± 0.5 LSB	NO	2.048	5±10%
TLC546	8	17	19	± 0.5 LSB	NO	1.1	5±10%
TLC1549	10	21	1	± 1.0 LSB	YES	2.1	5±10%
TLV1549	10	21	1	± 1.0 LSB	YES	2.1	3.3±10%
TLC1540	10	21	11	± 0.5 LSB	NO	1.1	5±10%
TLC1541	10	21	11	± 1.0 LSB	NO	1.1	5±10%
TLC1542	10	21	11	± 1.0 LSB *	YES	2.1	5±10%
TLC1543	10	21	11	± 1.0 LSB *	YES	2.1	5±10%
TLV1543	10	21	11	± 1.0 LSB	YES	1.1	3.3±10%
TLC2543	12	10	11	± 2.0 LSB **	YES	4.1	5±10%

* The TLC1542 is selected to have ± 0.5LSB zero offset, linearity error and fullscale error compared to ± 1.0LSB for the TLC1543.

** The TLC2543 has less than 1LSB differential linearity error with no missing codes

Figure 3.3 - Serial Output ADCs Selection Guide

2.1.1 Conversion Cycle

Although the details vary from device to device, they all have a similar timing sequence for control and data output. The cycle is divided into two periods: The first, controlled by the I/O clock, clocks out the previous conversion result, clocks in the input address for the current conversion and sets up the sampling time for the current conversion. The second period is the actual conversion time (T_{CONV}) of the successive approximation process itself.

Figure 3.4 illustrates a conversion cycle for a typical member of the family, the TLC1543 10-bit resolution, 11-input ADC.

With the chip select ($\overline{CS}$) inactive high, the ADDRESS INPUT and I/O CLOCK inputs are initially disabled and the DATA OUT output is in the high impedance state. When the $\overline{CS}$ goes active low, the data conversion sequence begins with the enabling of ADDRESS INPUT and I/O CLOCK and the removal of DATA OUT output from the high impedance state. The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS INPUT (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for six I/O CLOCK periods. The sample is held on the falling edge of the 10th I/O CLOCK and the successive approximation conversion begins. The MSB of the previous conversion result appears on DATA OUT on the falling edge of $\overline{CS}$ and the remaining bits are shifted out on the next nine falling edges of I/O CLOCK.

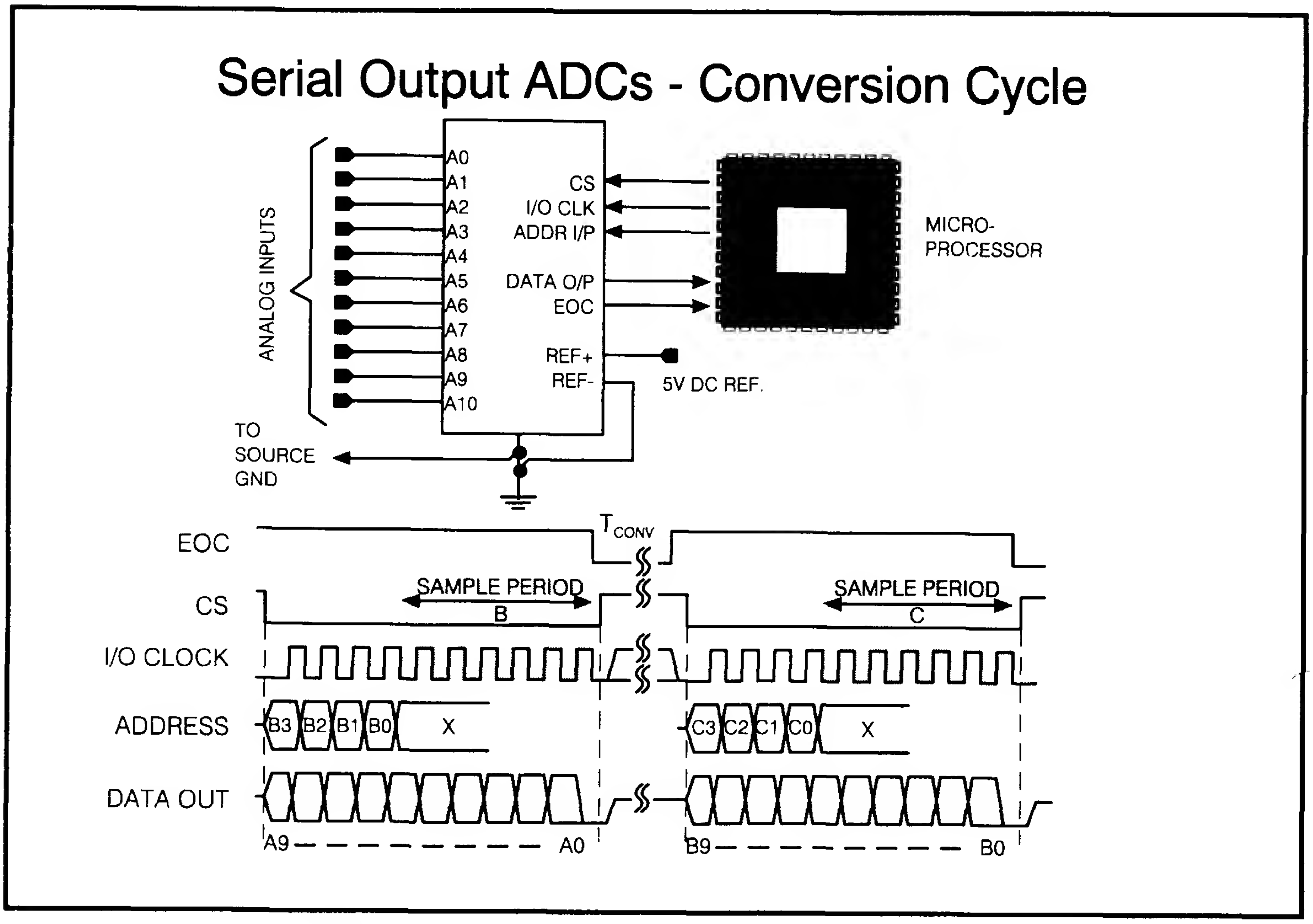

Serial Output ADCs - Conversion Cycle
ANALOG INPUTS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CS
I/O CLK
ADDR I/P
DATA O/P
EOC
REF+
REF-
MICRO-
PROCESSOR
5V DC REF.
TO
SOURCE
GND
EOC
T CONV
CS
SAMPLE PERIOD
B
SAMPLE PERIOD
C
I/O CLOCK
ADDRESS
B3
B2
B1
B0
X
C3
C2
C1
C0
X
DATA OUT
A9
A0
B9
B0

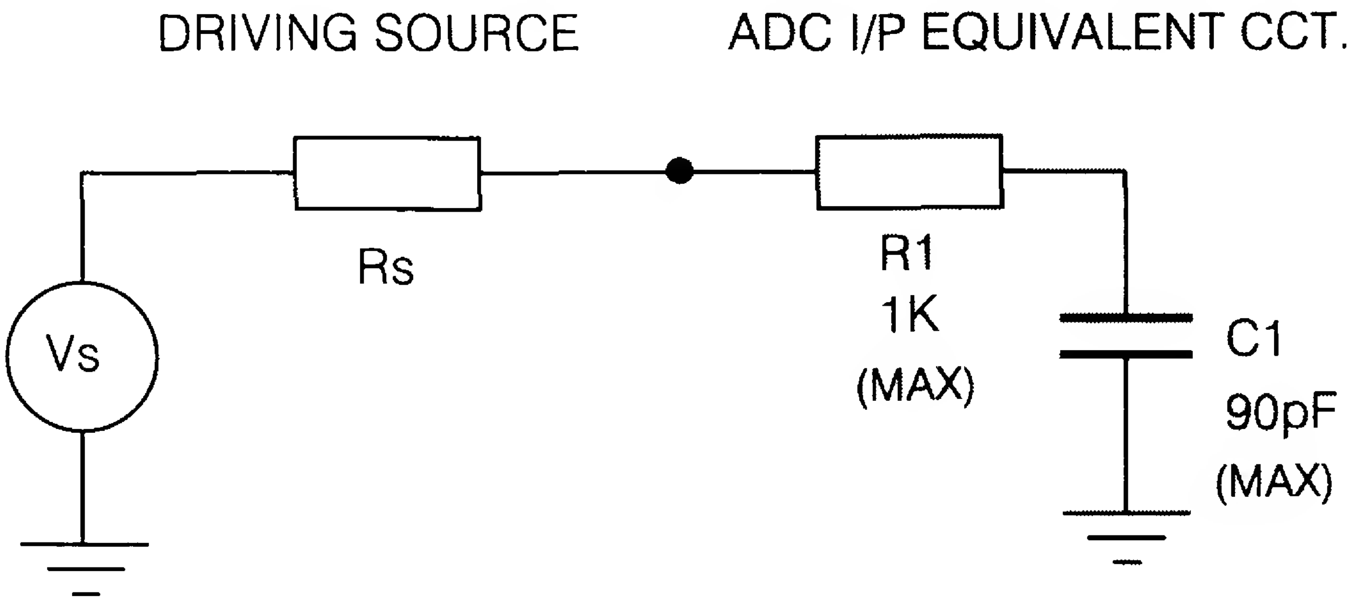
Figure 3.4 - TLC1543 Conversion Cycle Timing

2.1.2 Driving the Sample-and-Hold

The switched capacitor architecture used for TI's ADCs has an integral sample-and-hold function. At the analog input, this looks like a capacitor to ground during the sampling phase of the cycle and an open-circuit during the conversion phase of the cycle. In addition, there is a resistance in series with the analog input due to the ESD protection circuitry.

Driving the I/P of a switched capacitor ADC

- Driving source needs to charge C1 to within 1/2 LSB during sampling time
- Time to charge to 1/2 LSB = TC x ln(2 x resolution)
- ≃ 7.6 x TC for a 10-bit converter, or 9 x TC for a 12-bit converter



Time constant (TC) = (Rs + R1) x C1

Figure 3.5 - Driving the Input of a Switched Capacitor ADC

For correct operation of the ADC, the capacitor must be charged to the required accuracy of 1/2 LSB or more (depending on your system error budget) during the sampling phase of the ADC cycle.

The voltage V_C on capacitor C1 is given by:-

$$V_C = V_S \ (1 - e^{-t/TC})$$

where TC is the time constant $C_1(R_S+R_1)$

So:-

$$e^{-t/TC} = (1 - \frac{V_C}{V_S})$$

$$-t/TC = \ln(1 - \frac{V_C}{V_S})$$

Hence, for a full scale change in I/P voltage, the time taken to settle to 1/2 LSB is:-

$$t = -TCx\ln(1-\frac{V_S - \frac{1}{2}LSB}{V_S}) = TCx\ln(2xRESOLUTION)$$

For a 10 bit converter the time taken to settle to 1/2 LSB would be:-

$$TC \ x \ ln(2 \ x \ 1024) \approx 7.6 \ x \ TC.$$

This therefore sets a maximum limit on the source impedance when driving into a capacitive ladder ADC (or a limit on the maximum speed for a given source impedance). For this family of ADCs, the maximum value of C1 is 90 pF and there is an internal series resistance of approximately 1 kΩ for ESD protection.

For example, if we consider the case of the TLC1543 ADC working with its maximum I/O CLOCK speed of 2.1 MHz, then the sample time will be

$$6x \, {}^{1}\!/_{2.1x10^6} = 2.86\mu s$$

Substituting this sampling time into the above equation we get:-

$$2.86x10^{-6} = 7.6x90x10^{-12}xR$$

$$\therefore R|_{MAX} = \frac{2.86x10^{-6}}{7.6x90x10^{-12}} \approx 4.2\ k\Omega$$

As there is already an internal resistance of approximately 1 kΩ, the maximum source impedance for full speed operation is 3.2 kΩ. However, in order to compensate for internal switch resistance and external temperature variations, it is recommended that the maximum source resistance should be no greater than half this value.

In addition to this, one also needs to take into consideration the settling time of the signal conditioning stages which precede the ADC.

2.2 Interfacing the TLV1549 to 3.3 V Microcontrollers

2.2.1 The TLV1549

The TLV1549 is a single input, 10-bit ADC which operates from a 3.3-volt (± 0.3 volt) single supply. It has a conversion time of 21us and a maximum I/O CLOCK of 2.1 MHz.

This section describes how to interface the TLV1549 to three popular microcontrollers which operate from a single 3.3 volt supply rail. They are the 68HC05, the TMS70C02 and the 80C51-L.

2.2.2 Interface Timing

The timing for each of the interfaces is as illustrated in Figure 3.6. It uses one chip-select ($\overline{CS}$) pulse for each 10-bit conversion and includes 16 I/O CLOCK pulses between each $\overline{CS}$.

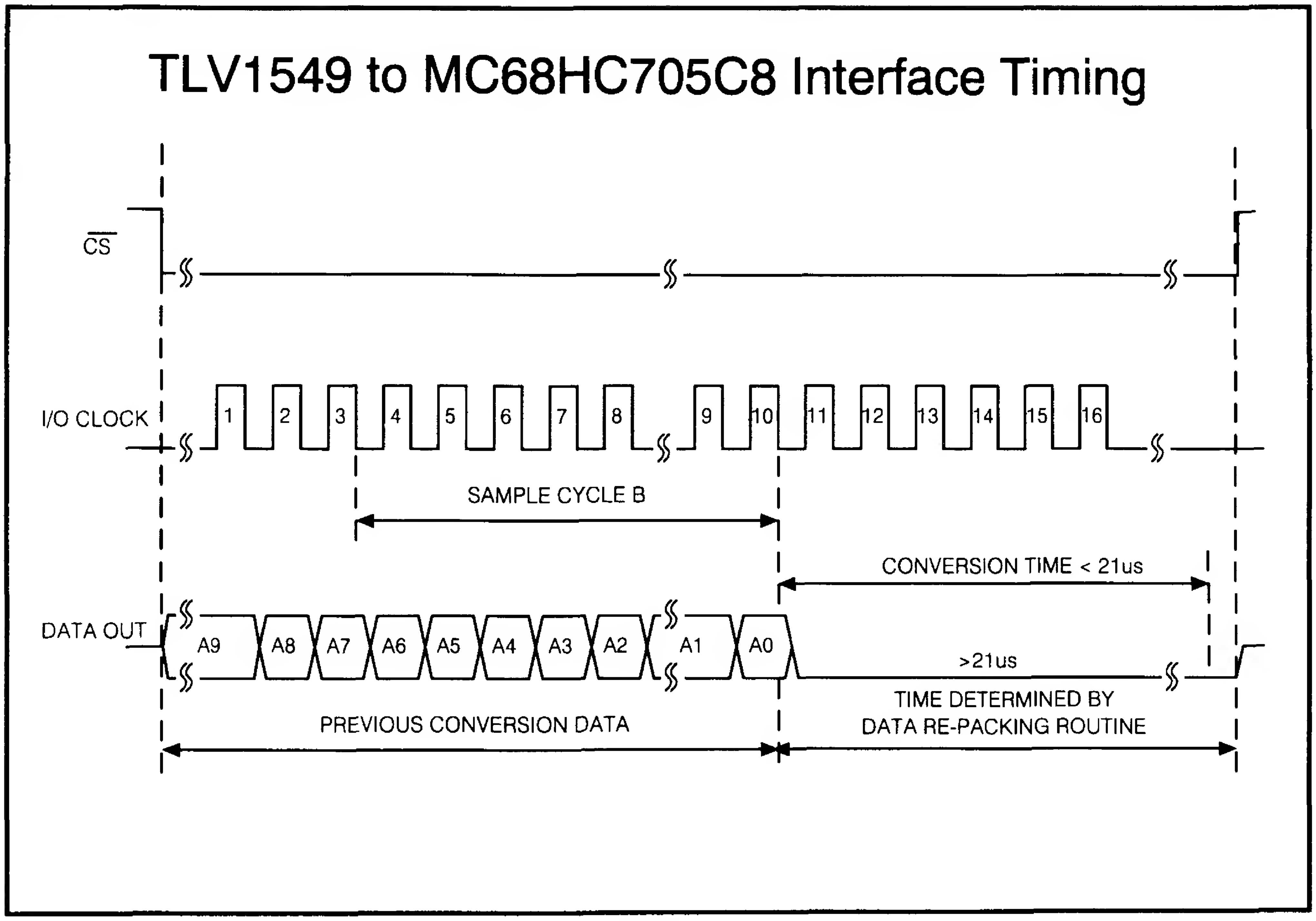

TLV1549 to MC68HC705C8 Interface Timing
CS
I/O CLOCK
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
SAMPLE CYCLE B
CONVERSION TIME < 21us
DATA OUT
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
>21us
TIME DETERMINED BY
DATA RE-PACKING ROUTINE
PREVIOUS CONVERSION DATA

Figure 3.6 - TLV1549 to MC68HC705C8 Interface Timing

2.2.3 Use of Software Subroutines

The subroutines shown here have been developed, as much as possible, as relocateable pieces of software. It should be noted that they include a provision for setting the number of consecutive conversions to be performed. This is either set in the main program as in the TMS7000 and 80C51-L examples or inside the subroutine as used in the 68HC05 example, by programming the number of conversions into "COUNT". It is recommended that at least two conversions are performed either after a power-up reset or after a protracted time interval from the last conversion. This enables the TLV1549's on-board sample-hold to acquire the most recent signal level during the first conversion cycle before outputting the digital result during the second cycle.

2.2.4 Data Format

In whatever format the data arrives at the microcontroller, it is important to ensure that any reformatting, if required, puts the data into a convenient final format. The software examples included in this seminar place the most significant byte of the conversion result in one byte of random access memory (RAM) and the least significant byte in an adjacent byte of RAM. The two least significant bits of the 10-bit result are placed in the least significant bit locations of their RAM location.

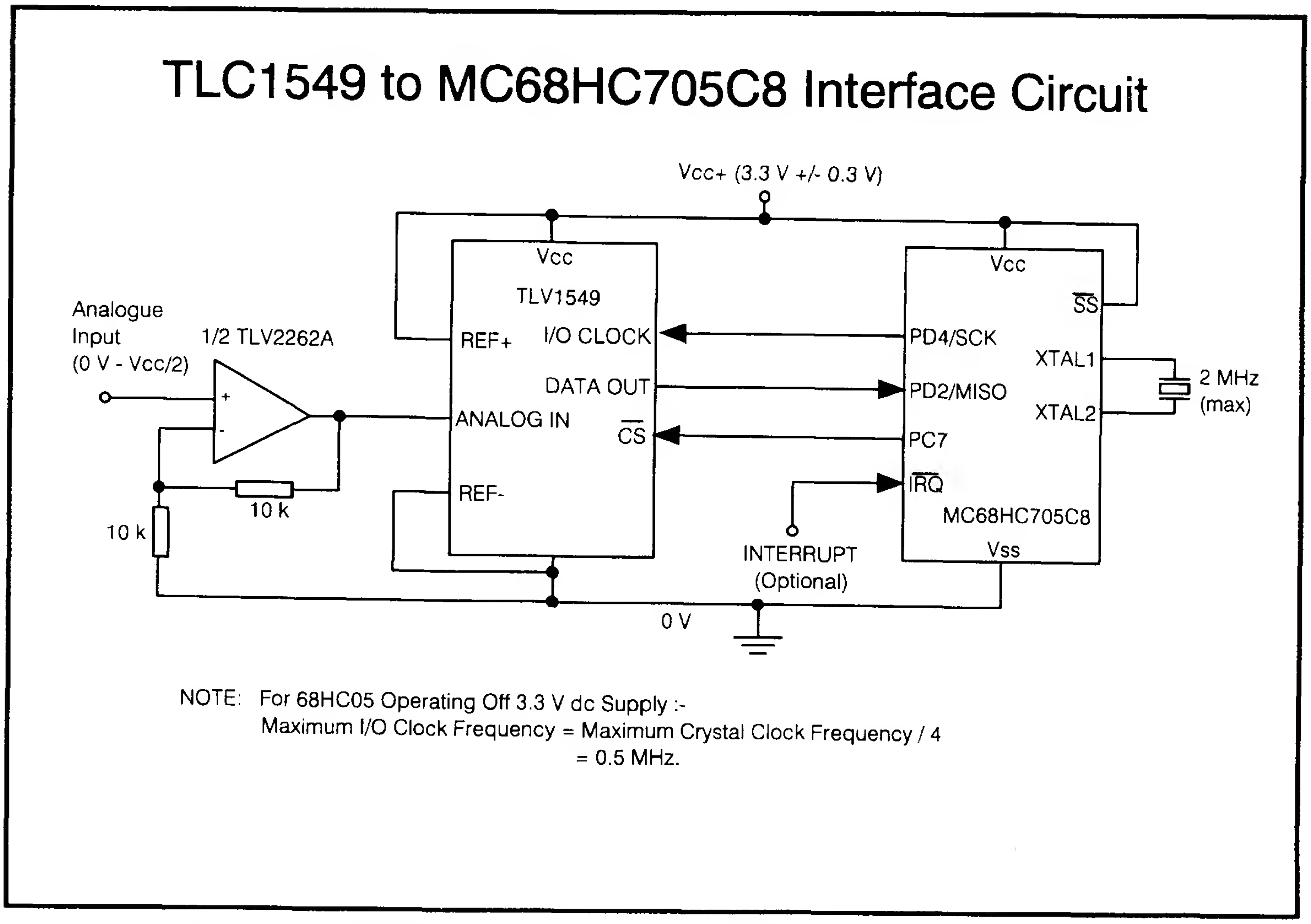
This format gives the user the flexibility to use only 8-bit precision data if so required , to add the MS and LS bytes together for use in 16 bit wide architectures, to view the 2 least significant bits of the result for fine tuning applications or to reformat into another format more convenient to his specific needs.

2.3 TLV1549 - 68HC05 Interface

2.3.1 Microcontroller Features

The M68HC05 family of microcontrollers consists of several different product variants of the basic architecture. It is important that the correct product type is specified to ensure that it contains all the features and attributes necessary to fulfil all its eventual system requirements.

In the case of its suitability for interfacing to the TLV1549 serial out ADC, the M68HC05 product type should contain a Serial Peripheral Interface (SPI). Several types contain this feature including the MC68HC705C8 which is used in this example.


TLC1549 to MC68HC705C8 Interface Circuit
Vcc+ (3.3 V +/- 0.3 V)
Vcc
TLV1549
REF+
I/O CLOCK
DATA OUT
ANALOG IN
$\overline{CS}$
REF-
Analogue Input (0 V - Vcc/2)
1/2 TLV2262A
+
-
10 k
10 k
Vcc
$\overline{SS}$
PD4/SCK
XTAL1
PD2/MISO
XTAL2
PC7
$\overline{IRQ}$
MC68HC705C8
Vss
2 MHz (max)
INTERRUPT (Optional)
0 V

NOTE: For 68HC05 Operating Off 3.3 V dc Supply :-
Maximum I/O Clock Frequency = Maximum Crystal Clock Frequency / 4
= 0.5 MHz.

Figure 3.7 - TLV1549 Interface to the MC68HC705C8 Microcontroller

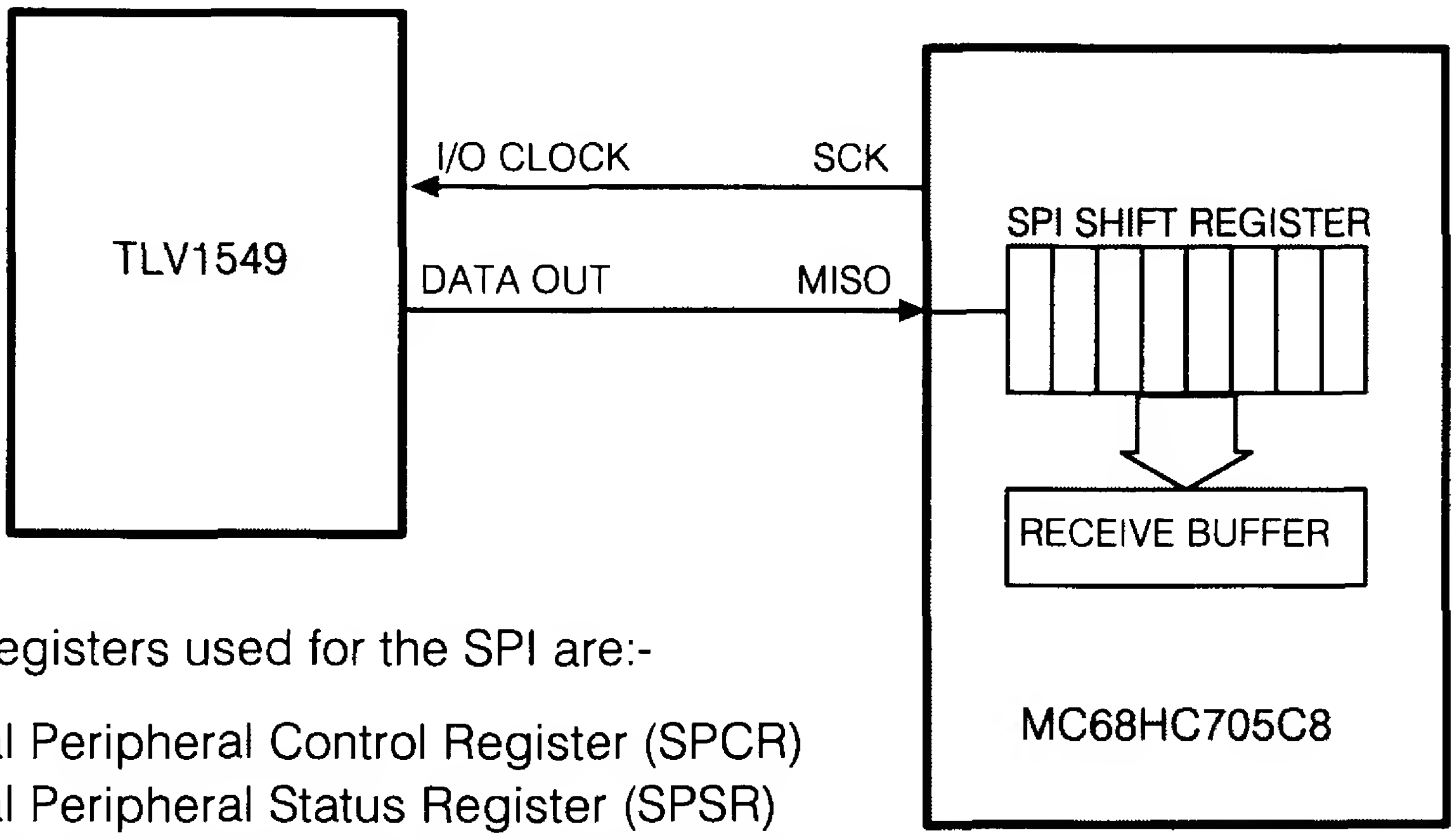
2.3.2 Interface Circuit

Figure 3.7 shows the circuit interconnections for the TLV1549 - MC68HC705C8 microcontroller interface. Note that no glue logic is required. The positive reference to the TLV1549 is provided directly from the Vcc+ supply. The analog signal is scaled by an appropriate factor (a gain of 2 in this case) and buffered by one half of a TLV2262A dual operational amplifier.

The three digital interface pins, I/O CLOCK, DATA OUT and $\overline{CS}$, of the TLV1549 connect directly to PD4/SCK, PD2/MISO and PC7 pins respectively of the microcontroller. When the SPI is enabled PD4 becomes SCK, which is the serial clock output, and PD2 becomes the MISO which is the Master In Slave Out pin. When programmed to be a master device, the microcontroller receives serial data at its MISO pin.

Figure 3.8 shows the shift register operation of the SPI when connected to a serial output peripheral component such as the TLV1549. Note that the MC68HC705C8 is operating as the master device and the TLV1549 is acting as the slave.

Shift Register Operation of the SPI



- The 3 registers used for the SPI are:-
  - Serial Peripheral Control Register (SPCR)
  - Serial Peripheral Status Register (SPSR)
  - Serial Peripheral data I/O Register (SPDR)

Figure 3.8 - Shift Register Operation of the Serial Peripheral Interface (SPI)

2.3.3 Software Considerations

The three registers which are used for SPI communications are :-

Serial Peripheral Control Register	(SPCR)
Serial Peripheral Status Register	(SPSR)
Serial Peripheral Data I/O Register	(SPDR)

Serial Peripheral Control Register (SPCR)

Bits 0 and 1 of SPCR program the SPI master bit rate. With bits 0 and 1 set to 0, SCK runs at the Internal Processor Clock/2. This means that SCK operates at one quarter of the microcontroller's XTAL frequency.

Bit 2 determines the phase relationship between the clock transmitted at SCK and the data appearing on the MISO pin. If 0 is placed in bit 3, SCK idles low. This is the correct condition for the TLV1549. Putting a 1 in bit 6 of SPCR enables the SPI and 0 in bit 6 disables the SPI. Putting a 1 in bit 4 (MSTR) confers the status of master on the microcontroller.

Serial Peripheral Status Register (SPSR)

The most important bit of SPSR is bit 7 (SPIF) which, when set to 1, indicates that a data transfer between the TLV1549 and the microcontroller has been completed. SPIF is automatically cleared when SPSR is read and the SPI data register is accessed.

Serial Peripheral Data I/O Register (SPDR)

When SPIF of SPSR is 1, SPDR contains the received byte of information from the converter. The contents of SPDR can then be read into a suitable register or location.

2.3.4 Program Flow

Figure 3.9 shows the programme flow chart and List 1 is the program listing for the TLV1549 to MC68HC705 interface. Note that COUNT has been set to 2. This ensures that two conversions are performed each time the "ADC" subroutine is used. The first conversion flushes out potentially erroneous data from the converter output registers. For test purposes the main program simply performs continuous repeat jumps to the ADC subroutine.

Note that the SPI expects the most significant bit of each received byte to arrive first. This is compatible with the order of TLV1549 output bit stream. Therefore no reformatting of the most significant byte of the 10-bit conversion result is required. However the least significant byte does need to be shifted right by 6 bits if the two LSBs of the conversion result are to be given their correct weighting factor for separate 8-bit processing.

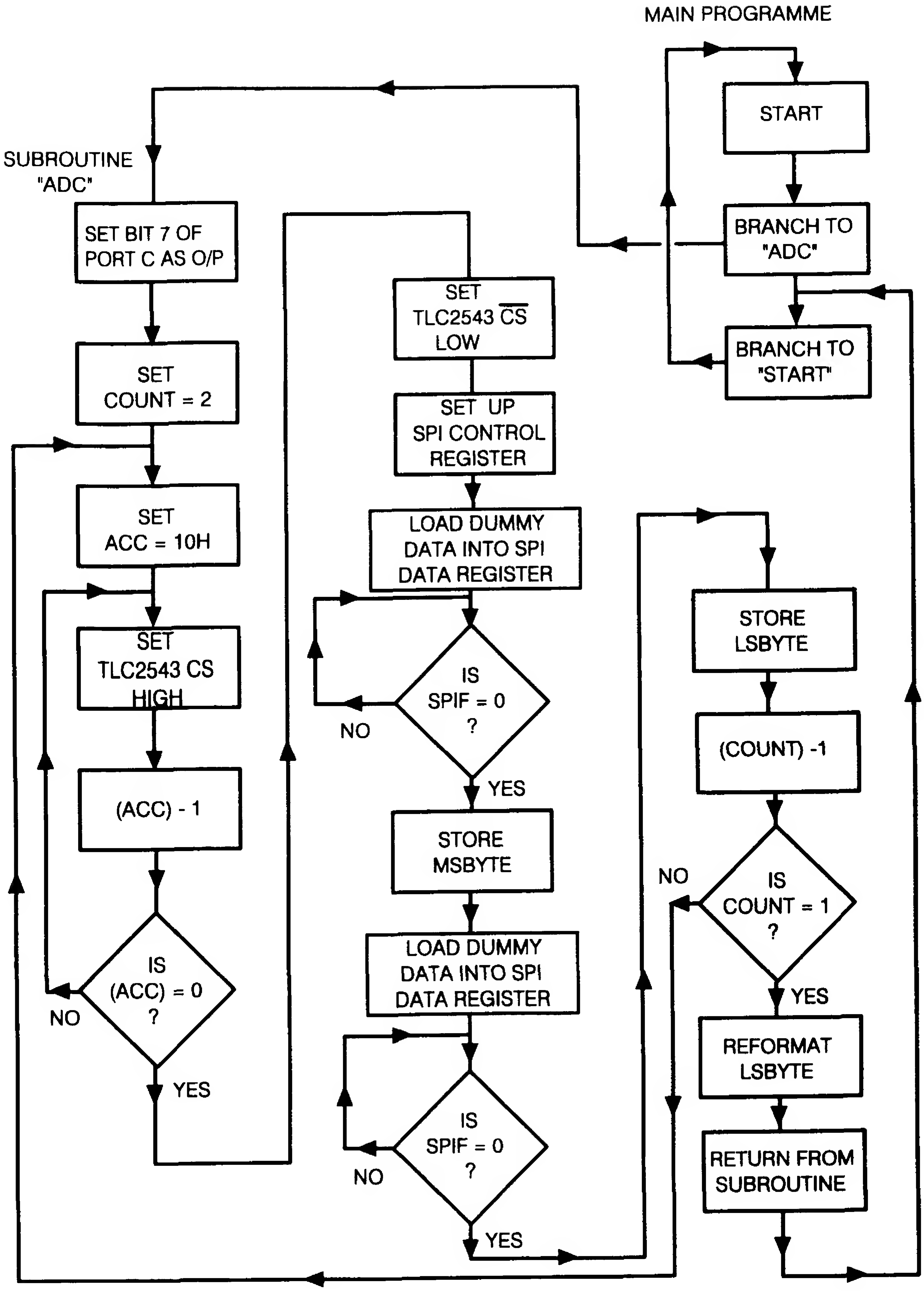

MAIN PROGRAMME
START
BRANCH TO "ADC"
BRANCH TO "START"
SUBROUTINE "ADC"
SET BIT 7 OF PORT C AS O/P
SET COUNT = 2
SET ACC = 10H
SET TLC2543 CS HIGH
(ACC) - 1
IS (ACC) = 0 ?
NO
YES
SET TLC2543 $\overline{CS}$ LOW
SET UP SPI CONTROL REGISTER
LOAD DUMMY DATA INTO SPI DATA REGISTER
IS SPIF = 0 ?
NO
YES
STORE MSBYTE
LOAD DUMMY DATA INTO SPI DATA REGISTER
IS SPIF = 0 ?
NO
YES
STORE LSBYTE
(COUNT) -1
IS COUNT = 1 ?
NO
YES
REFORMAT LSBYTE
RETURN FROM SUBROUTINE

Figure 3.9 - Programme Flow Chart

List 1. Program listing for the TLV1549 to MC68HC705 Interface

```
               *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *
               *                                                         *
               *     TLV1549 - MC68HC705C8 Interface Program             *
               *                                                         *
               *  This program contains a subroutine "ADC" which reads   *
               *  the serial data from two conversions of the TLV1549    *
               *  and places the MS Byte in address 50H and the LS Byte    *
               *  in address 51H.                                        *
               *  The data from the first conversion (potentially        *
               *  erroneous) is overwritten by the result from the       *
               *  second conversion.                                     *
               *                                                         *
               *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *
000A           SPCR    EQU 0AH         *  *  *  *  *  *  *  *  *  *  *
000B           SPSR    EQU 0BH         *                             *
000C           SPDR    EQU 0CH         *                             *
0002           PORTC   EQU 02H         *   Names Peripheral and      *
0006           DDRC    EQU 06H         *   Control Registers         *
0011           SCDAT   EQU 11H         *                             *
000E           SCCR1   EQU 0EH         *                             *
000F           SCCR2   EQU 0FH         *                             *
0010           SCSR    EQU 10H         *  *  *  *  *  *  *  *  *  *  *
0050           MSBYTE  EQU 50H         *  *  *  *  *  *  *  *  *  *  *
0051           LSBYTE  EQU 51H         * Names working RAM addresses *
1FFE           RESETH  EQU 1FFEH       *                             *
1FFF           RESETL  EQU 1FFFH       *                             *
0052           COUNT   EQU 52H         *  *  *  *  *  *  *  *  *  *  *
0160                   ORG 160H        Start Program at 160H
0160 A601              LDA #01H
0162 C71FFE            STA RESETH      Load Reset Vector High Byte
0165 A660              LDA #60H
0167 C71FFF            STA RESETL      Load Reset Vector Low Byte
016A CD016F    START   JSR ADC
016D 20FB              BRA START
016F A602      ADC     LDA #02H
0171 B752              STA COUNT
0173 A610      CONVERT LDA #10H
0175 1E06      CSHIGH  BSET 7,DDRC     Set Port C bit 7 (TLV1549 CS) high
0177 4A                DECA
0178 26FB              BNE CSHIGH
017A 1F06              BCLR 7,DDRC     Reset TLV1549 CS (Low)
017C A650              LDA #50H        Load accumulator with 50H
017E B70A              STA SPCR        Load SPI control register
0180 A600              LDA #00H        Load dummy data into accumulator
0182 B70C              STA SPDR        Receive SPI data
0184 0F0BFD    HBYTE   BRCLR 7,SPSR,HBYTE
0187 B60C              LDA SPDR
0189 B750              STA MSBYTE      Put MS Byte in Location 50
018B A600              LDA #00H        Load dummy data into accumulator
018D B70C              STA SPDR        Receive SPI data
018F 0F00FD    LBYTE   BRCLR 7,0B,LBYTE
0192 B60C              LDA SPDR
0194 B751              STA LSBYTE      Put LS Byte in Location 51
0196 3A52              DEC COUNT
0198 B652              LDA COUNT
019A 26D7              BNE CONVERT     If COUNT=1, do another conversion
019C A606              LDA #06H        *  *  *  *  *  *  *  *  *
019E 98        FORMAT  CLC             *                        *
019F 3651              ROR LSBYTE      *  Reformats LSBYTE      *
01A1 4A                DECA            *                        *
01A2 26FA              BNE FORMAT      *  *  *  *  *  *  *  *  *
01A4 81                RTS
01A5                   END
```

2.4 TLV1549 - TMS7000 Interface

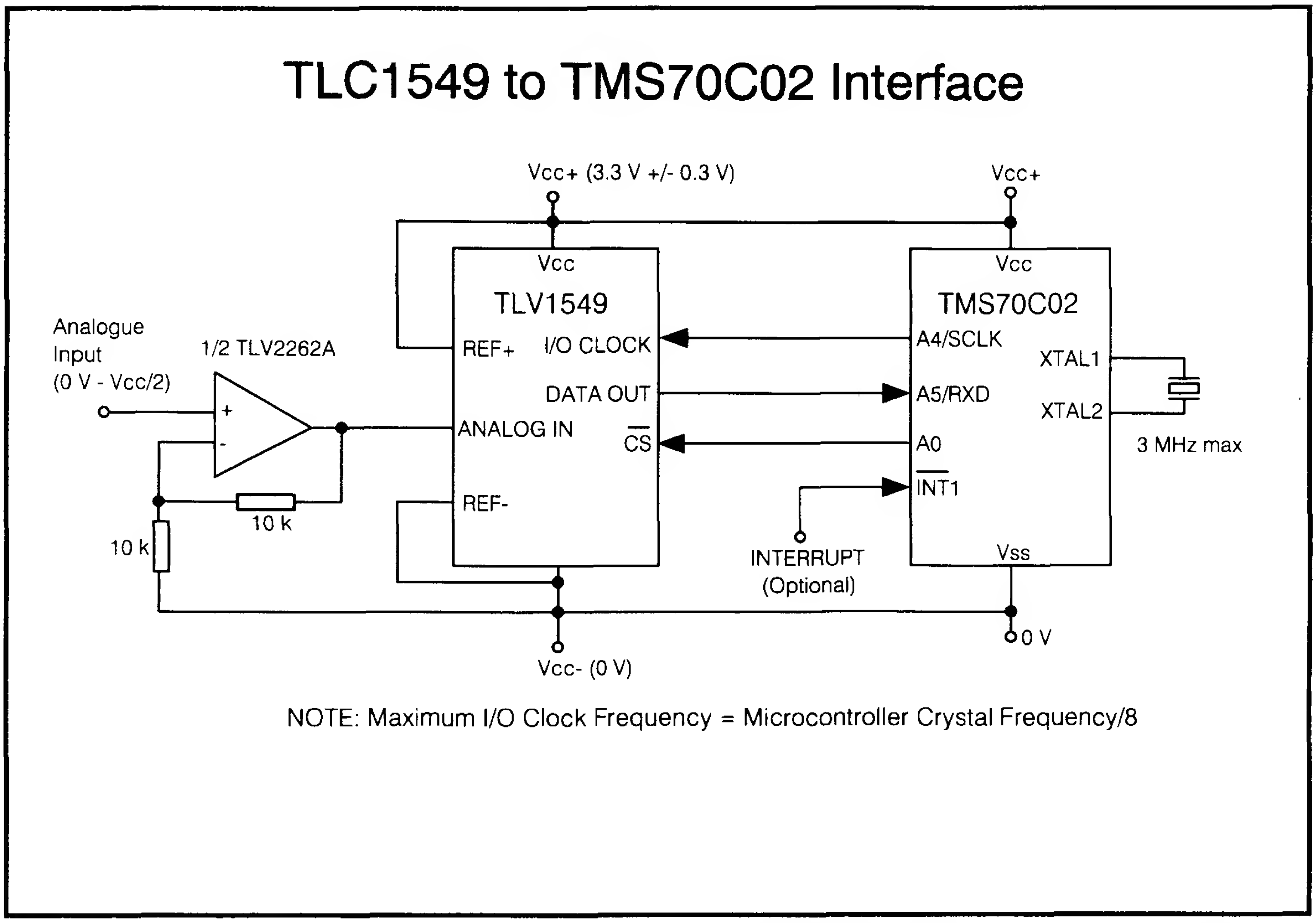
2.4.1 Microcontroller Features

The entire range of TMS7000 microcontrollers can be operated with a 3 volt supply. However the maximum crystal frequency which they will tolerate at this supply voltage over the full temperature range is 3 MHz. The inherently longer instruction cycle times which this yields should be taken into account when deciding how many software delay loops are necessary to produce the required delay.

Within the family of TMS7000 microcontrollers three types are available which have a serial port. These are the TMS70Cx2, TMS77C82 and TMS70Cx8. This application report refers to the TMS70Cx2 but any one of these three types could be chosen to efficiently implement a serial interface to the TLV1549.

Three modes of serial communication are available for the serial port. These are the asynchronous mode, isosynchronous mode and the serial I/O mode. The most suitable of these for interfacing the TMS70Cx2 to the TLV1549 is the serial I/O mode.

2.4.2 Interface Circuit


TLC1549 to TMS70C02 Interface
Vcc+ (3.3 V +/- 0.3 V)
Vcc+
Vcc
TLV1549
REF+
I/O CLOCK
DATA OUT
ANALOG IN
$\overline{CS}$
REF-
Vcc
TMS70C02
A4/SCLK
XTAL1
A5/RXD
XTAL2
A0
$\overline{INT1}$
Vss
3 MHz max
Analogue Input (0 V - Vcc/2)
1/2 TLV2262A
+
-
10 k
10 k
INTERRUPT (Optional)
Vcc- (0 V)
0 V

NOTE: Maximum I/O Clock Frequency = Microcontroller Crystal Frequency/8

Figure 3.10 - TLV1549 10 Bit Serial Out ADC to TMS70C02 Microcontroller Interface

The TLV1549 to TMS70C02 interface circuit is shown in Figure 3.10. The chip select ($\overline{CS}$) of the TLV1549 is controlled by the output from A0 (bit 0 of Peripheral Port A).

Serial I/O Mode

Four peripheral registers are used to set up and control the serial I/O mode of the microcontroller. These are :

Serial Mode Register	(SMODE)
Serial Control Register 0	(SCTL0)
Serial Control Register 1	(SCTL1)
Serial Port Status Register	(SSTAT)

The contents of the SMODE register determine the data format and type of communication mode (serial I/O for example). In the serial I/O mode the frame format of each character is five to eight data bits followed by a stop bit. Setting the number of bits to eight can simplify the software necessary to implement the interface.

SCTL0 enables either transmit or receive communication. SCTL1 determines the source of SCLK and programs the frequency of SCLK

SSTAT is a read-only register which is used for checking the status of the serial port. Bit 1 (RXRDY) of SSTAT is 0 when the receive buffer (RXBUF) is empty and 1 when RXBUF is full.

Provision of TLV1549 Chip Select $(\overline{CS})$

On power-up and/or system reset the TLV1549 chip select pin $(\overline{CS})$ should be initialised to a high level. To provide this, one of the bi-directional peripheral port bits can be programmed as an output and set to a 1 for a period of at least 21 µs. This period is provided by a delay loop at the beginning of the ADC subroutine. Note that the number of times around the loop required to achieve at least 21 µs is dependent on the clock frequency of the microcontroller and the number of instruction cycles contained within the delay loop. The example shown in List 2. uses 16 times but less than this can be used to optimise conversion throughput rate.

On completion of this delay loop the particular peripheral port bit is reset to 0 and the converter is now ready to send out data from the previously performed conversion.

Data Reformatting and Storage

Having checked that RXBUF is full its contents can be read to a suitable register for subsequent access and processing. In the case of the 10-bit conversion result from the TLV1549 two successive bytes of data are received and each are placed in RXBUF to be read consecutively into two convenient memory locations.

The TLV1549 sends the digital result of each conversion with the most significant bit first and the least significant bit last. This is the reverse order to that which the TMS70C02 expects. A few software instructions are therefore inserted near the end of the conversion subroutine which reformat the data into the correct order for interpretation by the microcontroller.

Other Software Considerations

The subroutine which services the TLV1549 conversion should be located in a convenient area of memory which is compatible with the rest of system. For example, all serial port versions of the TMS7000 family have 8K of EPROM. This EPROM is located between addresses E000H (Hex) and FFFFH. A converter subroutine start address which is half way through this EPROM memory space may be convenient in that it leaves the first half of this space for the location of the main program. The example software listing (List 2) uses a start location of F006 which was convenient for the emulation system it was developed on.

On system reset the stack pointer is at location 0001H. In programs which include nested subroutines, where the number of RAM locations taken up by the stack becomes large, the stack may interfere with other useful or even critical RAM locations. It is therefore prudent to reposition the stack pointer, immediately after reset, at a higher address in RAM such as 0060H. This allows the stack plenty of room to grow and avoids interference with lower address RAM locations.

2.4.3 Software Listing

The software shown in List 2 reads in the results of two 10-bit conversions from the TLV1549. The software routine "ADC" actually reads in the results from N conversions, where N is the contents of register "COUNT". The first conversion in a sequence of conversions may well be erroneous because the data received is derived from a previous (probably invalid) sample of the analog signal. It will often be useful to flush out this first spurious reading before receiving a second valid conversion result.

The setting of the contents of COUNT is performed within the main program and should normally be set to a minimum of 2.

List 2. Program listing for TLV1549 to TMS70C02 Microcontroller Interface

```
           * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
           *            TLV1549 - TMS70C02 Interface Program                 *
           *                                                                 *
           *  This program contains a subroutine "ADC" which reads in the   *
           *  serial data from two conversions of the TLV1549. The data     *
           *  (potentially erroneous) from the first conversion is          *
           *  overwritten by the data from the second conversion.           *
           *  The most significant byte is placed in register 16            *
           *  The least significant byte is placed in register 17           *
           * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
     0004  APORT EQU P4         *  *  *  *  *  *  *  *  *  *  *  *  *  *
     0005  ADDR  EQU P5
     0014  SMODE EQU P20        *                                       *
     0015  SCTL0 EQU P21
     0016  SSTAT EQU P22        *     Name Peripheral Registers         *
     0018  SCTL1 EQU P24
     0019  RXBUF EQU P25        *                                       *
     001A  TXBUF EQU P26
     0009  COUNT EQU R9         *     Name Count and Result Registers   *
     0010  MSBYTE       EQU R16
     0011  LSBYTE       EQU R17         *  *  *  *  *  *  *  *  *  *  *  *  *  *
F006                 AORG >F006     Set start address of program
F006    52 START MOV %>60,B         Set stack register
F007    60
F008    0D           LDSP
F009    A2           MOVP %>11,ADDR Set up Port A Data Direction Register
F00A    11
F00B    05
F00C    A2           MOVP %>0C,SMODE       Set up Serial Mode Register
F00D    0C
F00E    14
F00F    72           MOV %>02,COUNT Set COUNT = 2
F010    02
F011    09
F012    8E           CALL @ADC      Call Subroutine "ADC"
F013  F017
F015    E0           JMP START      On return from Subroutine ADC, jump to START
F016    EF
F017    22 ADC       MOV %>03,A     Put 03 in register A
```

```
     F018   03
0031 F019   A2  CSHIGH      MOVP %>01,APORT      TLV1549 Chip Select goes high
     F01A   01
     F01B   04
0032 F01C   B2       DEC A          Decrement the contents of Register A by 1
0033 F01D   E6       JNZ CSHIGH     and jump to CSHIGH if result is not zero
     F01E   FA
0034 F01F   A2       MOVP %>00,APORT        TLV1549 Chip Select goes low
     F020   00
     F021   04
0035 F022   A2       MOVP %>16,SCTL0        Set up Serial Control Register 0
     F023   16
     F024   15
0036 F025   A2       MOVP %>C0,SCTL1        Set up Serial Control Register 1
     F026   C0
     F027   18
0037 F028   80  LABEL1      MOVP SSTAT,A    Put contents of Serial Status Reg in A
     F029   16
0038 F02A   26       BTJO %>2,A,LABEL2      If bit 1 of A is 1, jump to LABEL2
     F02B   02
     F02C   02
0039 F02D   E0       JMP LABEL1             and if not, jump to LABEL1
     F02E   F9
0040 F02F   80  LABEL2      MOVP RXBUF,A    Put contents of RXBUF (MS Byte) in A
     F030   19
0041 F031   D0       MOV A,R10      Put contents of A into Register 10
     F032   0A
0042 F033   A2       MOVP %>16,SCTL0        Set up serial control Register 0
     F034   16
     F035   15
0043 F036   A2       MOVP %>C0,SCTL1        Set uo serial control Register 1
     F037   C0
     F038   18
0044 F039   80  LABEL3      MOVP SSTAT,A    Put contents of Serial Status Reg in A
     F03A   16
0045 F03B   26       BTJO %>2,A,LABEL4      If bit 1 of A is 1, jump to LABEL1
     F03C   02
     F03D   02
0046 F03E   E0       JMP LABEL3             and if not, jump to LABEL3
     F03F   F9
0047 F040   80  LABEL4      MOVP RXBUF,A    Put contents of RXBUF (LS Byte) in A
     F041   19
0048 F042   D0       MOV A,R11      Put contents of A in Register 11
     F043   0B
0049 F044   D2       DEC COUNT      (COUNT) - 1
     F045   09
0050 F046   E6       JNZ ADC        If COUNT is not zero do another conversion
     F047   CF
0051 F048   B0       CLRC           Clear carry bit
0052 F049   DD       RRC R11        *  *  *  *  *  *  *  *  *  *  *  *  *  *
     F04A   0B
0053 F04B   E7       JNC LSBIT0     *  Reformats Least Significant Byte     *
     F04C   03
0054 F04D   74       OR %>2,R11     *  *  *  *  *  *  *  *  *  *  *  *  *  *
     F04E   02
     F04F   0B
0055 F050   42  LSBIT0      MOV R11,LSBYTE Put reformatted LSByte in LSBYTE
     F051   0B
     F052   11
0056 F053   D5       CLR R12        Clear register 12
     F054   0C
0057 F055   D5       CLR R14        and   register 14
     F056   0E
0058 F057   22       MOV %>8,A      Set contents of A to 8
     F058   08
0059 F059   42       MOV R10,R12    Put contents of register 10 in register 12
     F05A   0A
     F05B   0C
0060 F05C   B0  FORMAT      CLRC        *  *  *  *  *  *  *  *  *  *  *  *  *  *
0061 F05D   DD       RRC R12
     F05E   0C
0062 F05F   DF       RLC R14        *  Reformats Most Significant Byte      *
```

```
     F060   0E
0063 F061   B2          DEC A
0064 F062   E6          JNZ FORMAT       *  *  *  *  *  *  *  *  *  *  *  *  *  *
     F063   F8
0065 F064   42          MOV R14,MSBYTE Put reformatted MSByte into MSBYTE
     F065   0E
     F066   10
0066 F067   0A          RETS             Return from subroutine "ADC"
0067 FFFE               AORG >FFFE       Configure Reset vector
0068 FFFE F006          DATA START       to point to START
0069                    END
```

2.5 TLV1549 - 80C51-L Interface

2.5.1 Microcontroller Features

The 80C51-L is the 3.3 volt supply version of the 80C51 family of microcontrollers. Various 3.3 volt supply versions of the 80C51 architecture are available from different manufacturers. Individual data sheets should be consulted to establish at which maximum crystal frequency each specific device type can operate.

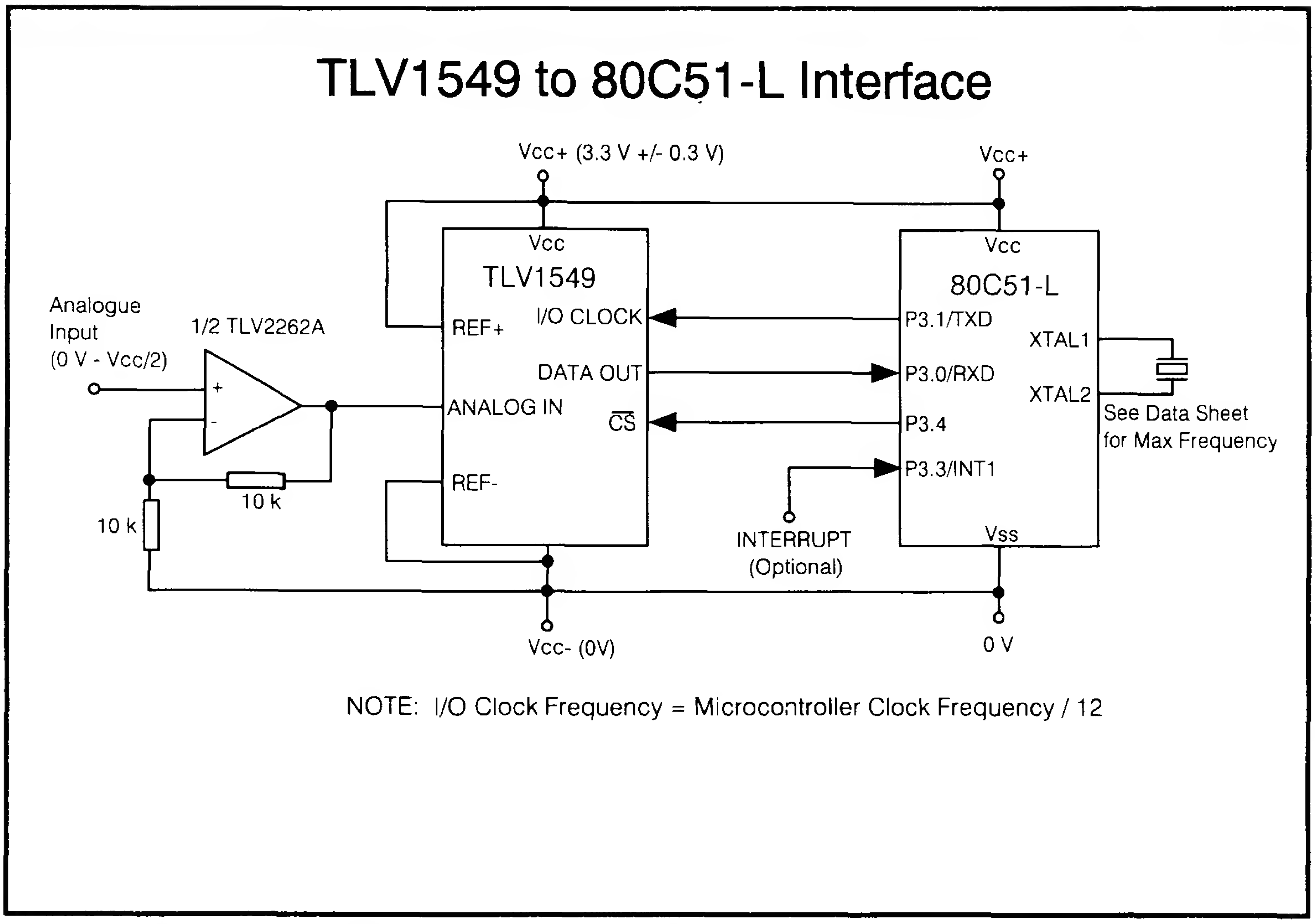
As indicated for the previously described interfaces, the most suitable method of receiving the serial output from the TLV1549 is to configure the serial port of the microcontroller to perform like an 8-bit shift register. The same is true for the 80C51-L

2.5.2 Serial I/O Mode 0

The type of serial communication to and from the 80C51-L is determined by the data inserted into the Serial Port Control Register (SCON). The contents of the most significant bits of SCON (bits 7 and 6) determine which of four modes (0, 1, 2 and 3) the serial port operates in.

Mode 0 is the shift register and is programmed by 0 in each of bits 7 and 6 of SCON. Bit 4 (REN) of SCON is the receive enable bit. This is set to 1, while bit 1 (RI) of SCON is 0, to receive serial data. In this configuration data is received at bit 0 of Port 3 (P3.0). The synchronising signal for clocking in this data is output at TXD which is bit 1 of Port 3 (P3.1).

When configured for Mode 0, eight bits are received with no trailing stop bit for each enabling of serial reception. The data is received with the least significant bit expected first, the reverse of the order in which the TLV1549 serial data arrives. Reformatting of the received data is therefore necessary.


TLV1549 to 80C51-L Interface
Vcc+ (3.3 V +/- 0.3 V)
Vcc+
Vcc
TLV1549
REF+
I/O CLOCK
DATA OUT
ANALOG IN
CS
REF-
Vcc
80C51-L
P3.1/TXD
P3.0/RXD
P3.4
P3.3/INT1
XTAL1
XTAL2
Vss
See Data Sheet
for Max Frequency
Analogue
Input
(0 V - Vcc/2)
1/2 TLV2262A
+
-
10 k
10 k
INTERRUPT
(Optional)
Vcc- (0V)
0 V

NOTE: I/O Clock Frequency = Microcontroller Clock Frequency / 12

Figure 3.11. - TLV1549 10-bit Serial Out ADC to 80C51-L Microcontroller

2.5.3 Interface Circuit

Figure 3.11 shows the interconnections necessary to implement the interface of the TLV1549 to the 80C51-L microcontroller. Note that $\overline{CS}$ of the TLV1549 is driven by bit 4 of Port 3 (P3.4) of the 80C51-L.

2.5.4 Software Listing

In a similar manner to the previously described program listings, List 3 contains the subroutine "ADC" which reads into the 80C51-L the ten bits of serial data resulting from a single conversion of the TLV1549. The number of consecutive conversions performed for each jump to subroutine "ADC" is equal to the number placed in "COUNT". The result of each conversion is overwritten by that of the next conversion in the sequence.

List 3. Program listing for the TLV1549 to 80C51-L Interface

```
LOC   OBJ            LINE     SOURCE

                              ;*  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *
                              ;*                                                 *
                              ;*      TLV1549 - 80C51-L Interface Program        *
                              ;*                                                 *
                              ;*  This program contains a subroutine "ADC" which *
                              ;*  reads in the serial data from the TLV1549      *
                              ;*  10-bit ADC and places                          *
                              ;*  the most significant byte in address 20H       *
                              ;*  and least significant byte in address 21H      *
                              ;*  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *

```

```
  0020          MSBYTE   EQU 20H          ;*  *  *  *  *  *  *  *  *  *
  0021          LSBYTE   EQU 21H          ;*  Name data destinations   *
  REG           COUNT    EQU R3           ;*  and COUNT register       *
                ;                          *  *  *  *  *  *  *  *  *  *
0022                     ORG 22H          ;Set start address
0022 7B02       START:   MOV COUNT,#02H   ;Set COUNT=2 (Do 2 conversions)
0024 020029              JMP ADC          ;Jump to subroutine ADC
0027 80F9                JMP START        ;Repeat above again
0029 D2B4       ADC:     SETB P3.4        ;*  *  *  *  *  *  *  *  *  *
002B 7410                MOV A,#10H       ;* Set Port3 (bit 4) high    *
002D 14         DELAY:   DEC A            ;*(Sets CS of TLV1549 high)  *
002E 70FD                JNZ DELAY        ;*  *  *  *  *  *  *  *  *  *
0030 C2B4                CLR P3.4
0032 759810              MOV SCON,#10H
0035 3098FD     LABEL1:  JNB SCON.0,LABEL1        ;Read in
0038 C298                CLR SCON.0               ;most significant
003A A899                MOV R0,SBUF              ;byte, place in R0
003C 3098FD     LABEL2:  JNB SCON.0,LABEL2        ;Read in
003F C29C                CLR SCON.4               ;least significant
0041 C298                CLR SCON.0               ;byte,
0043 A999                MOV R1,SBUF              ;place in R1
0045 1B                  DEC COUNT        ;COUNT-1
0046 EB                  MOV A,COUNT      ;
0047 70E0                JNZ ADC          ;If COUNT not =0,
                                          ;do another conversion
0049 7C08                MOV R4,#08H      ;Put 08H in R4
004B AA00                MOV R2,00H
004D C3         LOOP:    CLR C            ;*  *  *  *  *  *  *  *
004E E8                  MOV A,R0         ;*                      *
004F 13                  RRC A            ;*                      *
0050 F8                  MOV R0,A         ;*  Reformats MSByte    *
0051 EA                  MOV A,R2         ;*                      *
0052 33                  RLC A            ;*                      *
0053 FA                  MOV R2,A         ;*                      *
0054 1C                  DEC R4           ;*                      *
0055 EC                  MOV A,R4         ;*                      *
0056 70F5                JNZ LOOP         ;*  *  *  *  *  *  *  *
0058 EA                  MOV A,R2         ;
0059 F520                MOV 20H,A        ;
005B E9                  MOV A,R1         ;*  *  *  *  *  *  *  *
005C 13                  RRC A            ;*                      *
005D F521                MOV 21H,A        ;*  Reformats LSByte    *
005F 9209                MOV 21H.1,C      ;*                      *
0061 C20F                CLR 21H.7        ;*  *  *  *  *  *  *  *
0063 22                  RET              ;Return from subroutine
                         END
```

2.6 Analog Considerations

2.6.1 Analog Reference for the TLV1549

The Ref+ pin of the TLV1549 can be directly connected to the Vcc rail of the device. This produces accurate results for analog input signals right up to the supply rail. However, if the operational amplifier driving the input is supplied from the same single supply as the ADC the op amp's output may not be linear all the way to the rail voltage. If this is a concern a lower reference voltage as shown in Figure 3.12 may be applied to Ref+ thus providing more headroom for the amplifier.

The output of the TLC2262A, 3-V single supply operational amplifier can swing to within 10 mV of its positive supply rail. This will effectively lose only two least significant bits (LSBs) off the top of the digital output range of the TLV1549 when both amplifier and ADC are powered from the same 3.3-V supply. Using Figure 3.12 to provide a 2.5-V reference to the converter restores those bits to the digital output of the TLV1549 while the maximum analog input swing is now reduced to 2.5 V.

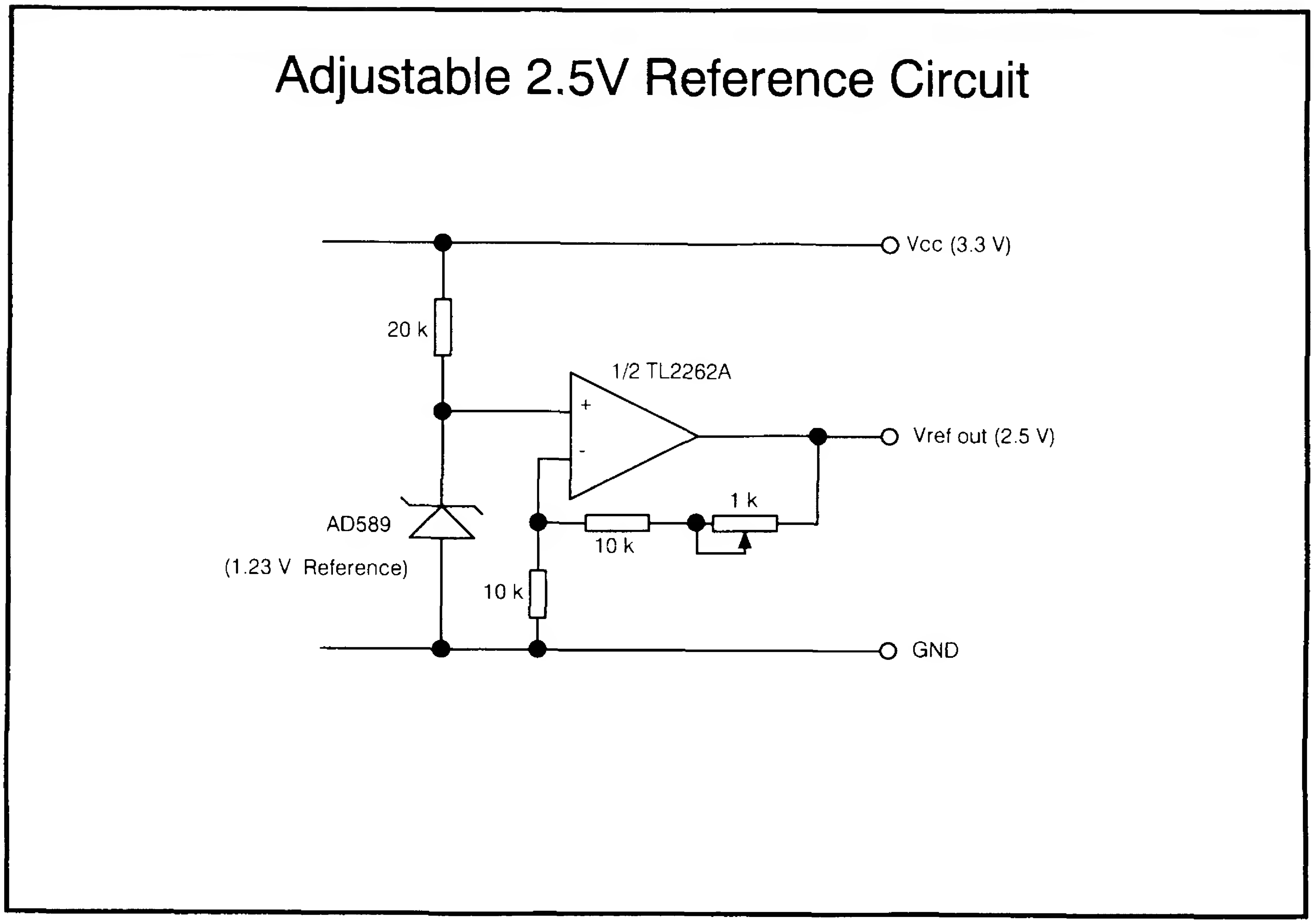

Adjustable 2.5V Reference Circuit
Vcc (3.3 V)
20 k
1/2 TL2262A
+
-
Vref out (2.5 V)
1 k
AD589
(1.23 V Reference)
10 k
10 k
GND

Figure 3.12 - User Adjustable 2.5V Reference Circuit

PCB Layout

As with all precision analog components, care should be taken in laying out the printed circuit board on which the TLV1549 and chosen microcontroller are placed. The interaction between digital and analog signal paths should be minimised by keeping them as far apart as is physically possible within the constraints of the dimensions of the PCB.

Grounding and Decoupling

Each supply pin to both the TLV1549 and the microcontroller should be decoupled by a ceramic capacitor of approximately 100 nF in value, situated close to the pin of the device. Digital and analog ground return paths should be kept separate to prevent any digitally generated currents from corrupting the analog signal.

References

MC68HC705C8 Technical Data Manual (1990)	Motorola
M68HC05 Applications Guide	Motorola
TLV1549 Data Sheet	Texas Instruments
TMS7000 Family Data Manual (1991)	Texas Instruments
Embedded Microcontrollers and Processors Vol 1	Intel Corporation

2.7 Interfacing the TLC2543 to Popular Microcontrollers

2.7.1 The TLC2543

The TLC2543 is a 12-bit analog to digital converter which uses the switched capacitor successive approximation technique to perform the conversion process. Any one of eleven analog input channels can be selected by programming the four most significant bits (MSBs) of the eight bit channel/mode control byte applied serially to the DATA INPUT pin of the device. In addition three test voltages, [Vref-, Vref+ and {(Vref+)-(Vref-)}/2], can be applied to the converter for calibration or other purposes by applying the appropriate code to the same four MSBs.

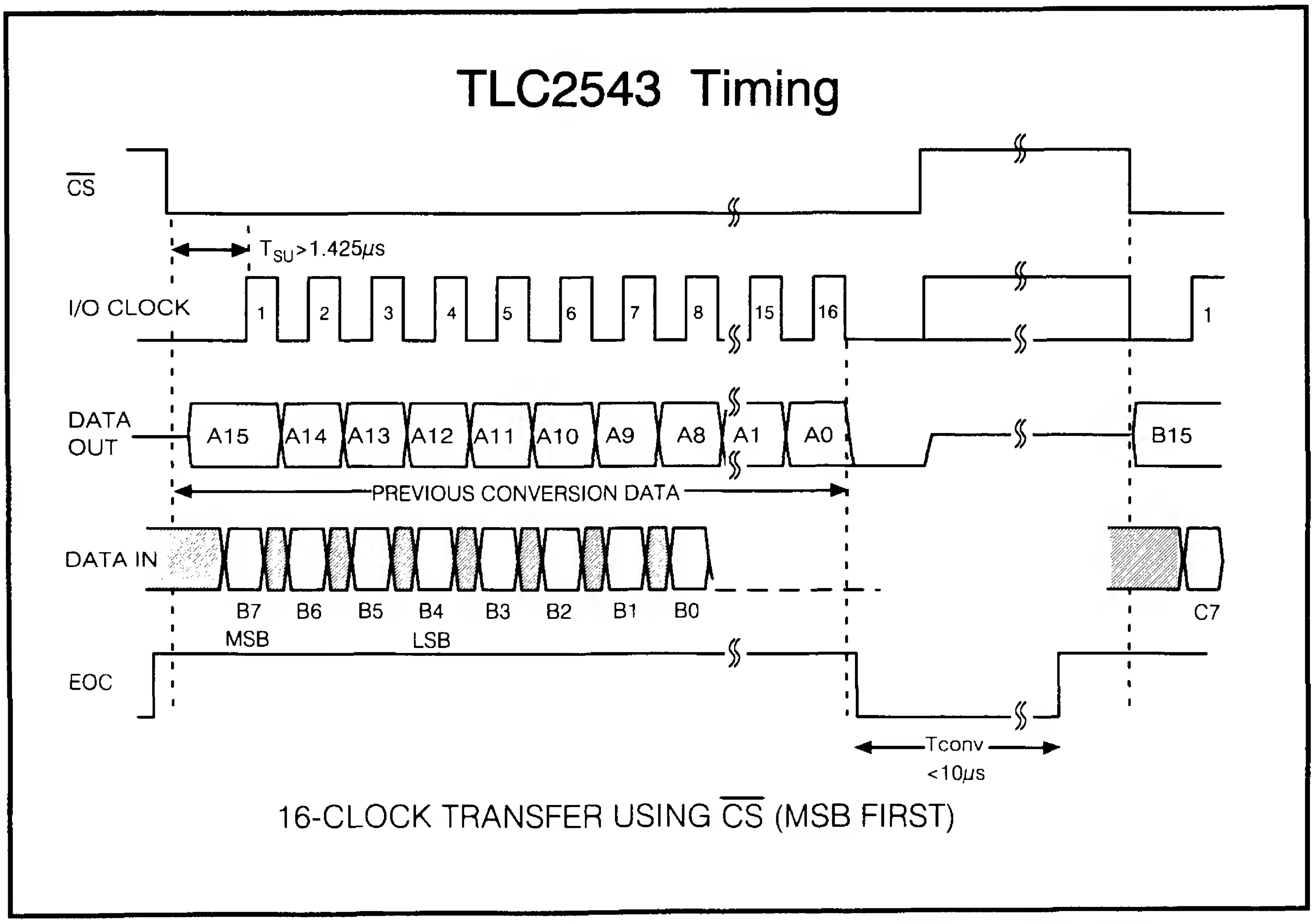

TLC2543 Timing
$\overline{CS}$
T_{SU}>1.425µs
I/O CLOCK
1
2
3
4
5
6
7
8
15
16
1
DATA OUT
A15
A14
A13
A12
A11
A10
A9
A8
A1
A0
B15
PREVIOUS CONVERSION DATA
DATA IN
B7
B6
B5
B4
B3
B2
B1
B0
MSB
LSB
C7
EOC
Tconv
<10µs
16-CLOCK TRANSFER USING $\overline{CS}$ (MSB FIRST)

Figure 3.13 - Timing for 16 Clock Transfer Using $\overline{CS}$ With MSB First

The four least significant bits (LSBs) of the channel/mode control byte are used to select the output data length (8, 12 or 16 bits), the output data order (MSB first or LSB first) and whether unipolar (binary) or bipolar (2's complement) format is required.

2.7.2 Interface Timing

Four transfer methods are available for obtaining the full 12 bits of resolution from the TLC2543. Either 12 or 16 clock cycles can be used for each conversion and data transfer.

A chip select (CS) pulse can be inserted at the start of each conversion or only once at the beginning of each sequence of conversions with CS remaining low until the sequence is completed.

Figure 3.13 shows the timing for the method which uses 16 clock cycles for each conversion and data transfer cycle and which inserts CS between each of these transfer cycles. Figure 3.14 shows the timing for the method which uses 16 clock cycles for each conversion and data transfer cycle but inserts CS only once at the start of each sequence of conversions.

This seminar text describes various microcontroller interfaces, each of which uses 16 clock cycles for each conversion data transfer. CS is applied at the start of each conversion and data transfer. This method allows for the general case where one or more conversions may be required. It also simplifies the required software.

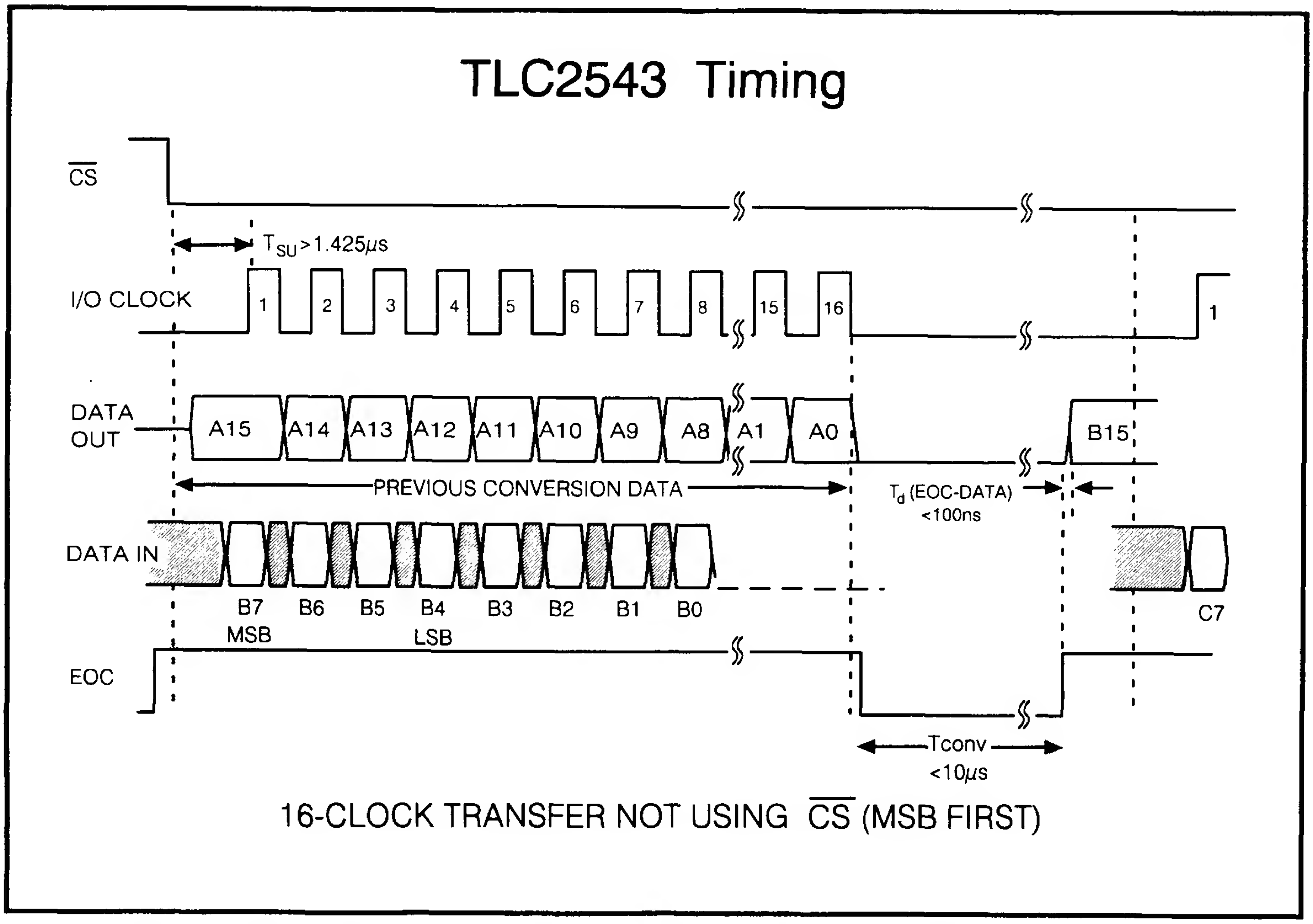

TLC2543 Timing
CS
T_SU>1.425µs
I/O CLOCK
1
2
3
4
5
6
7
8
15
16
1
DATA OUT
A15
A14
A13
A12
A11
A10
A9
A8
A1
A0
B15
PREVIOUS CONVERSION DATA
T_d (EOC-DATA) <100ns
DATA IN
B7 MSB
B6
B5
B4 LSB
B3
B2
B1
B0
C7
EOC
Tconv <10µs
16-CLOCK TRANSFER NOT USING CS (MSB FIRST)

Figure 3.14 - Timing for 16 Clock Transfer Not Using $\overline{CS}$ With MSB First

2.7.3 Minimum Number of Data Transfers per Channel

It should be noted that in any single data transfer cycle between the TLC2543 and the chosen microcontroller the data output from the ADC is the result of the previous conversion. The software listings included in this application report have been written for the general case where the conversion results may be required for any individual channel or sequence of channels. In this case the program included for each microcontroller interface must be run at least twice per channel so that valid data corresponding to the required analog input channel and ADC mode is delivered.

Software can be written to implement the consecutive channel scanning mode of operation of the TLC2543. In this case the result from the first analog to digital conversion should be ignored or overwritten.

2.7.4 Serial Peripheral Interface (SPI)

The fastest and most efficient method of implementing a data transfer between the TLC2543 and a microcontroller is to use the serial peripheral interface (SPI) of the microcontroller, if this is available.

The TMS370 (Texas Instruments), H8/300 (Hitachi) and MC68HC11 (Motorola) all offer SPI's (or the equivalent) in a subset of each of these families of microcontrollers. The H8/300 offers a Serial Communications Interface (SCI) which can be configured to operate in a similar way to that of the standard SPI's offered by the TMS370 and MC68HC11.

The principle features of the SPI are :

- Simultaneous serial data input and output.
- Synchronous operation.
- Provision of frequency programmable serial clock.
- Data transfer complete flag.

Figure 3.15 shows the structure of the SPI. In this case the TMS370C010 is used to illustrate the main elements of the interface. The microcontroller can be configured by software to perform as the SPI "master" or "slave". When operating as the master, data is input to the SPI shift register (SPIDAT) via the SOMI (Slave Out Master In) pin. At the same time data is output from the SPIDAT via the SIMO (Slave In Master Out) pin.

The SPI functions as follows. The SPIDAT should be loaded with the first byte of data to be sent. This automatically initiates the transmission of this byte. During this transmission time data is received at the other end of the SPIDAT shift register. The SPI INT FLAG is regularly checked. As soon as the last bit of the input data byte is received the SPI INT FLAG is set to 1. This then signals that the received byte can be read from the Serial Input Buffer (SPIBUF) and that the SPIDAT is ready to accept the next byte of data to be transmitted.

Additional SPI features which apply to the specific microcontrollers are described in their respective sections which follow.

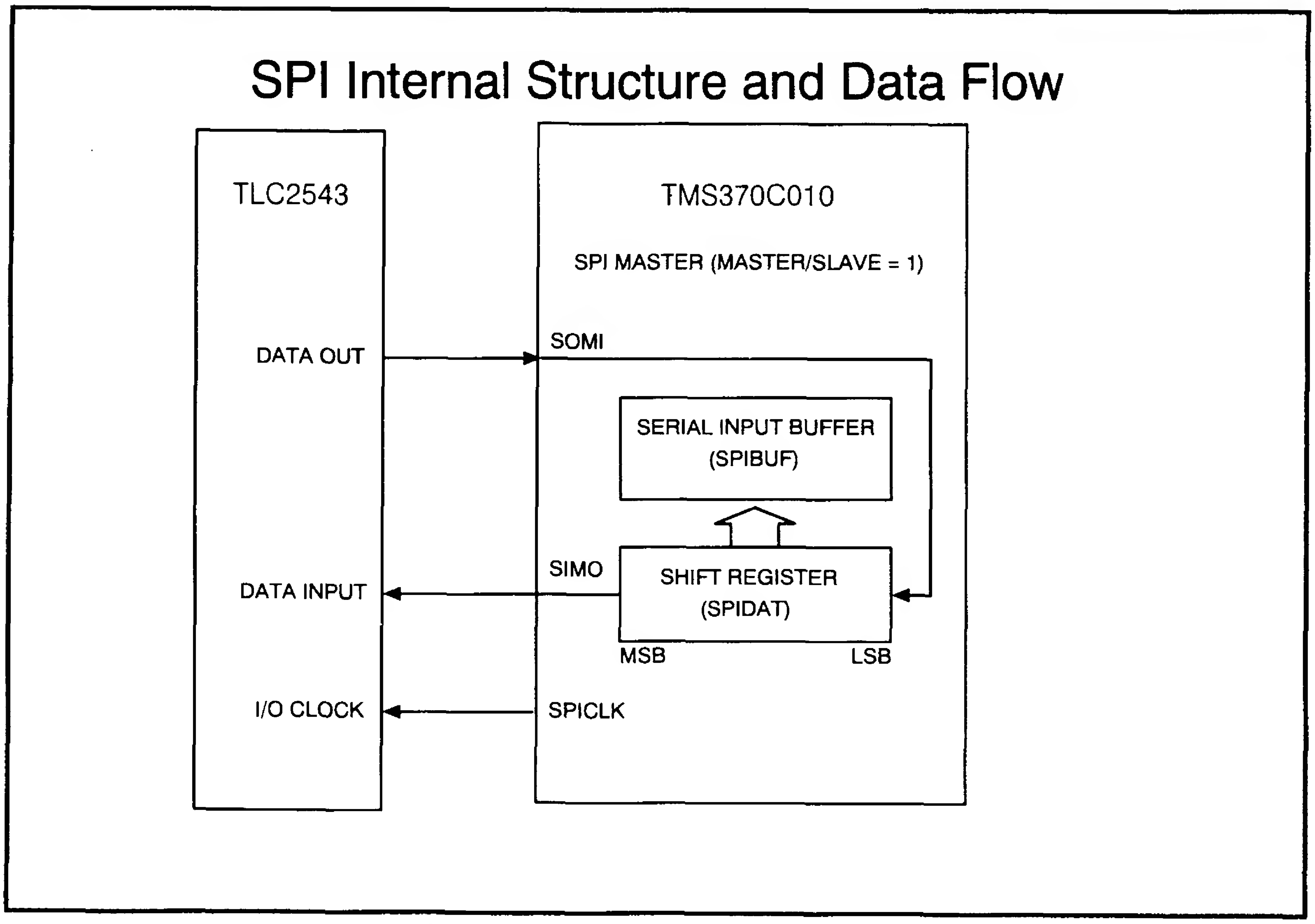

SPI Internal Structure and Data Flow
TLC2543
DATA OUT
DATA INPUT
I/O CLOCK
TMS370C010
SPI MASTER (MASTER/SLAVE = 1)
SOMI
SERIAL INPUT BUFFER (SPIBUF)
SIMO
SHIFT REGISTER (SPIDAT)
MSB
LSB
SPICLK

Figure 3.15 - Serial Peripheral Interface - Internal Structure and Data Flow

2.7.5 TLC2543 to SPI Interface Timing

The timing diagram for the 16 clock transfer TLC2543 to SPI interface is shown in Figure 3.16. The channel select/mode data is read into the TLC2543 on the positive going edges of the I/O clock and analog to digital conversion results are read into the microcontroller on the negative going edges of the I/O clock.

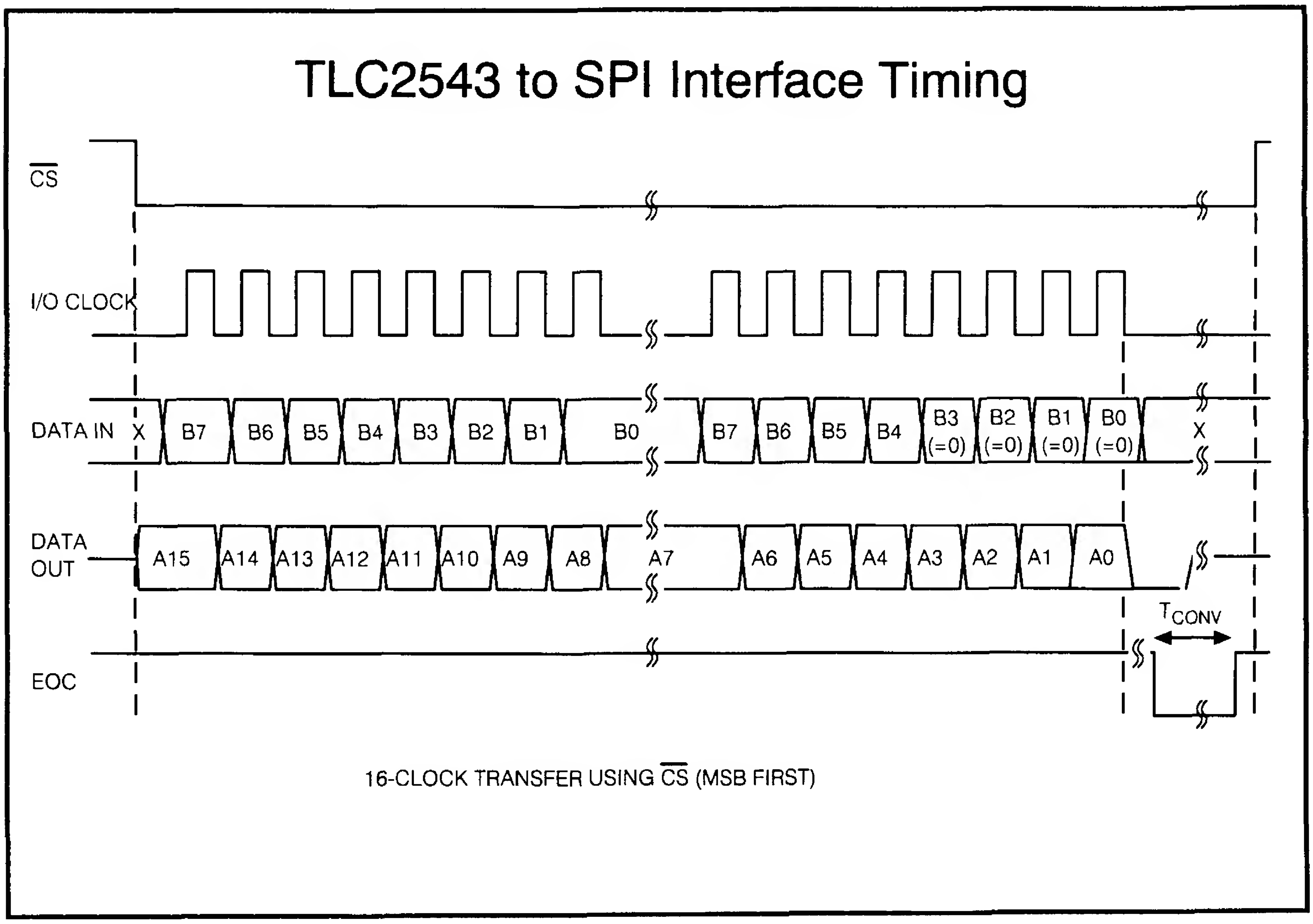
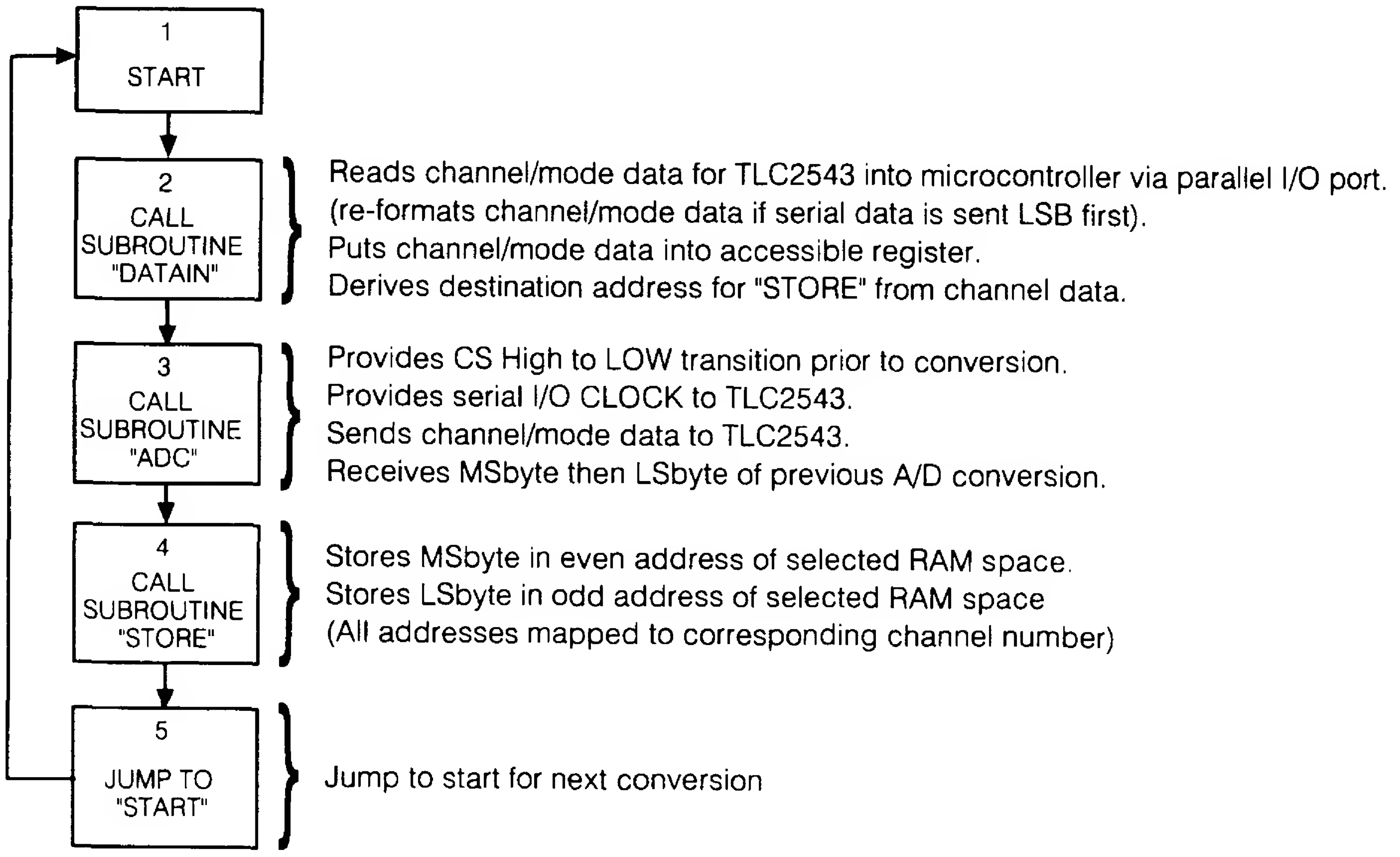

TLC2543 to SPI Interface Timing
$\overline{CS}$
I/O CLOCK
DATA IN
X
B7
B6
B5
B4
B3
B2
B1
B0
B7
B6
B5
B4
B3 (=0)
B2 (=0)
B1 (=0)
B0 (=0)
X
DATA OUT
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
EOC
T_CONV
16-CLOCK TRANSFER USING $\overline{CS}$ (MSB FIRST)

Figure 3.16 - TLC2543 to SPI Interface Timing

2.8 Software Structure

The contents of the programmes written for the four TLC2543-to-microcontroller interfaces included in this seminar are not identical. However they do contain a number of common features and the method by which they achieve their function can be understood by referring to the flow charts shown in Figures 3.17, 3.18 and 3.19. These flow charts apply directly to the software written for the TLC2543 to TMS370C010 microcontroller.



Reads channel/mode data for TLC2543 into microcontroller via parallel I/O port.
(re-formats channel/mode data if serial data is sent LSB first).
Puts channel/mode data into accessible register.
Derives destination address for "STORE" from channel data.

Provides CS High to LOW transition prior to conversion.
Provides serial I/O CLOCK to TLC2543.
Sends channel/mode data to TLC2543.
Receives MSbyte then LSbyte of previous A/D conversion.

Stores MSbyte in even address of selected RAM space.
Stores LSbyte in odd address of selected RAM space
(All addresses mapped to corresponding channel number)

Jump to start for next conversion

Figure 3.17 - Flowchart for Main Programme of TLC2543 to TMS370C010 Interface

Three functions should be performed by each interface programme. These are :-

- Reception of channel select and TLC2543 mode control data.
- Control of the analog to digital converter and the data flow to and from it.
- Storage of the conversion results in a convenient form.

The software described by the flowcharts in Figures 3.17, 3.18 and 3.19 performs these three functions using three separate subroutines named "DATAIN", "ADC" and "STORE" respectively which are called up consecutively by the main programme. The main programme is described in Figure 3.17 Subroutines "DATAIN" and "STORE" are shown in Figure 3.18 and the subroutine "ADC" is illustrated in Figure 3.19.

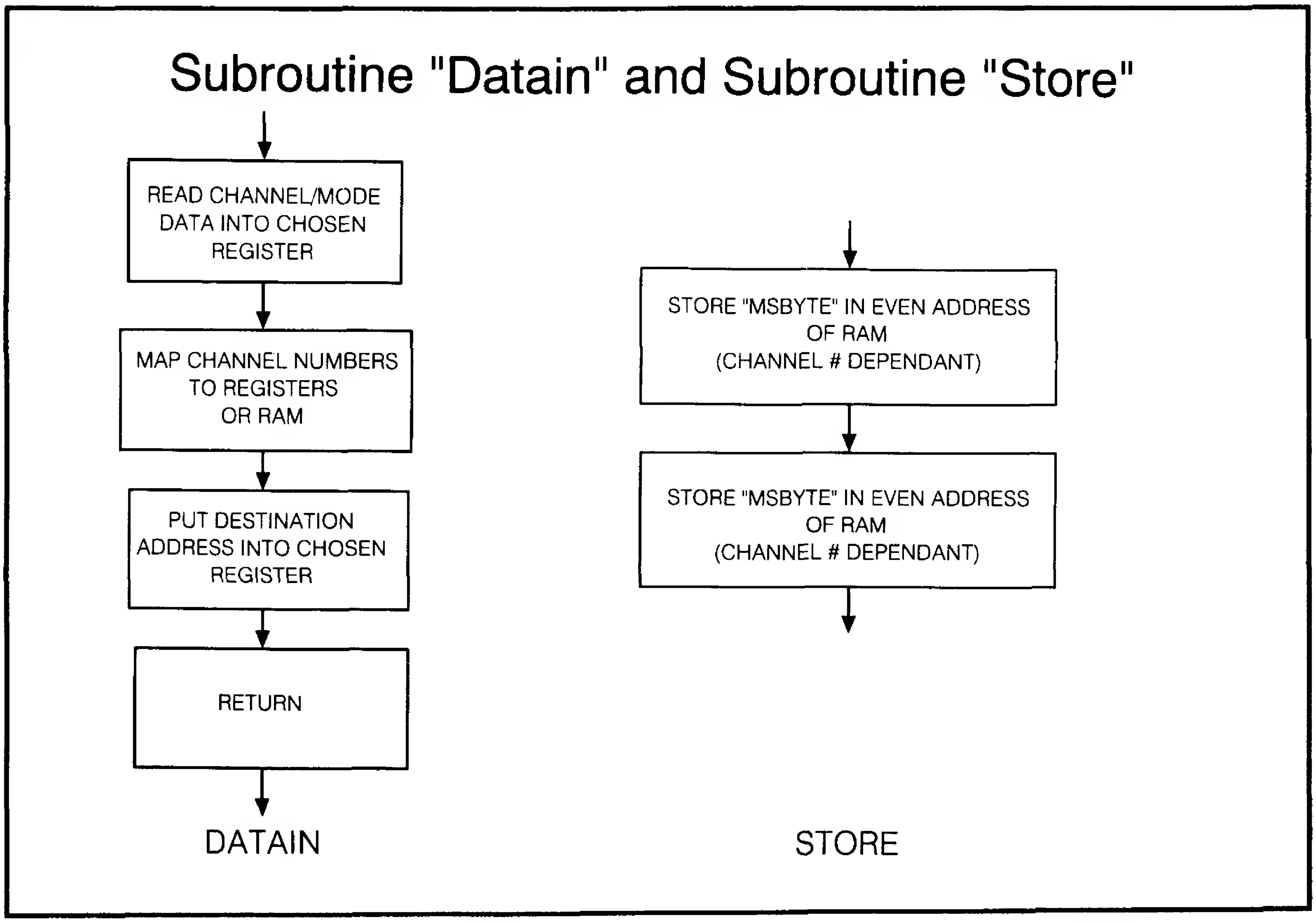

Subroutine "Datain" and Subroutine "Store"
READ CHANNEL/MODE DATA INTO CHOSEN REGISTER
MAP CHANNEL NUMBERS TO REGISTERS OR RAM
PUT DESTINATION ADDRESS INTO CHOSEN REGISTER
RETURN
DATAIN
STORE "MSBYTE" IN EVEN ADDRESS OF RAM (CHANNEL # DEPENDANT)
STORE "MSBYTE" IN EVEN ADDRESS OF RAM (CHANNEL # DEPENDANT)
STORE

Figure 3.18 - Subroutines "DATAIN" and "STORE" for TLC2543 to TMS370C010 Interface Software

The software includes the facility for the conversion results from the eleven analog input channels and three internally applied voltage levels to be stored conveniently in contiguous locations of RAM. The RAM address corresponding to each channel is "mapped" by a series of instructions which create a channel dependent vector. This vector is placed in a holding register to be used later in the programme to store the conversion results in their correct RAM locations. The TLC2543 to TMS370C010 interface programme performs this mapping function within the subroutine "DATAIN". Other interface programmes described in this seminar text perform the same function in their respective "STORE" subroutines.

Apart from controlling the actual analog to digital conversion function and handling of data to and from the TLC2543, the subroutine "ADC" also checks the state of the LSBF (Least Significant Bit First) bit of the channel select/mode byte (bit 1). The subroutine thus determines whether to expect conversion results in MSByte first or LSByte first order from the TLC2543.

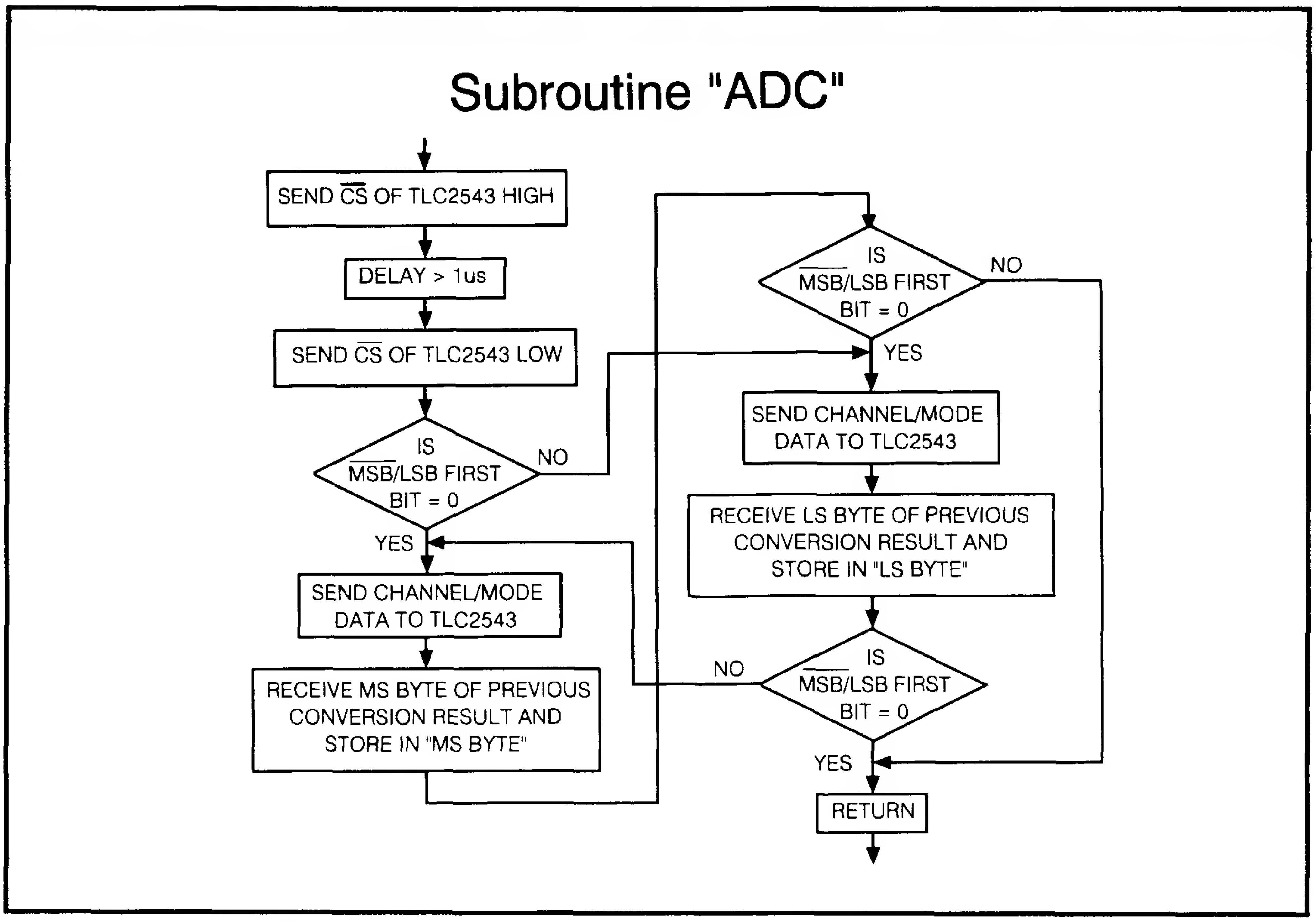

Subroutine "ADC"
SEND $\overline{CS}$ OF TLC2543 HIGH
DELAY > 1us
SEND $\overline{CS}$ OF TLC2543 LOW
IS $\overline{MSB}$/LSB FIRST BIT = 0
NO
YES
SEND CHANNEL/MODE DATA TO TLC2543
RECEIVE MS BYTE OF PREVIOUS CONVERSION RESULT AND STORE IN "MS BYTE"
IS $\overline{MSB}$/LSB FIRST BIT = 0
NO
YES
SEND CHANNEL/MODE DATA TO TLC2543
RECEIVE LS BYTE OF PREVIOUS CONVERSION RESULT AND STORE IN "LS BYTE"
NO
IS $\overline{MSB}$/LSB FIRST BIT = 0
YES
RETURN

Figure 3.19 - Subroutine "ADC" for the TLC2543 to TMS370C010 Interface Software

2.9 TLC2543 to TMS370 Microcontroller Interface

2.9.1 Microcontroller Features

Within the family of TMS370 microcontrollers there are several versions which contain a serial peripheral interface (SPI) facility. One of these versions should be chosen to implement the interface method described below. One such version is the TMS370C010 which is used to illustrate the method.

2.9.2 Interface Circuit

Figure 3.20 shows the circuit interconnections for the TLC2543 - TMS370C010 microcontroller interface. Note that no extra logic is required to implement this interface. It is possible to program the idle level of the SPI clock to be either high or low, thus eliminating the need for an external inverter to be added at the SPI clock output of the TMS370.

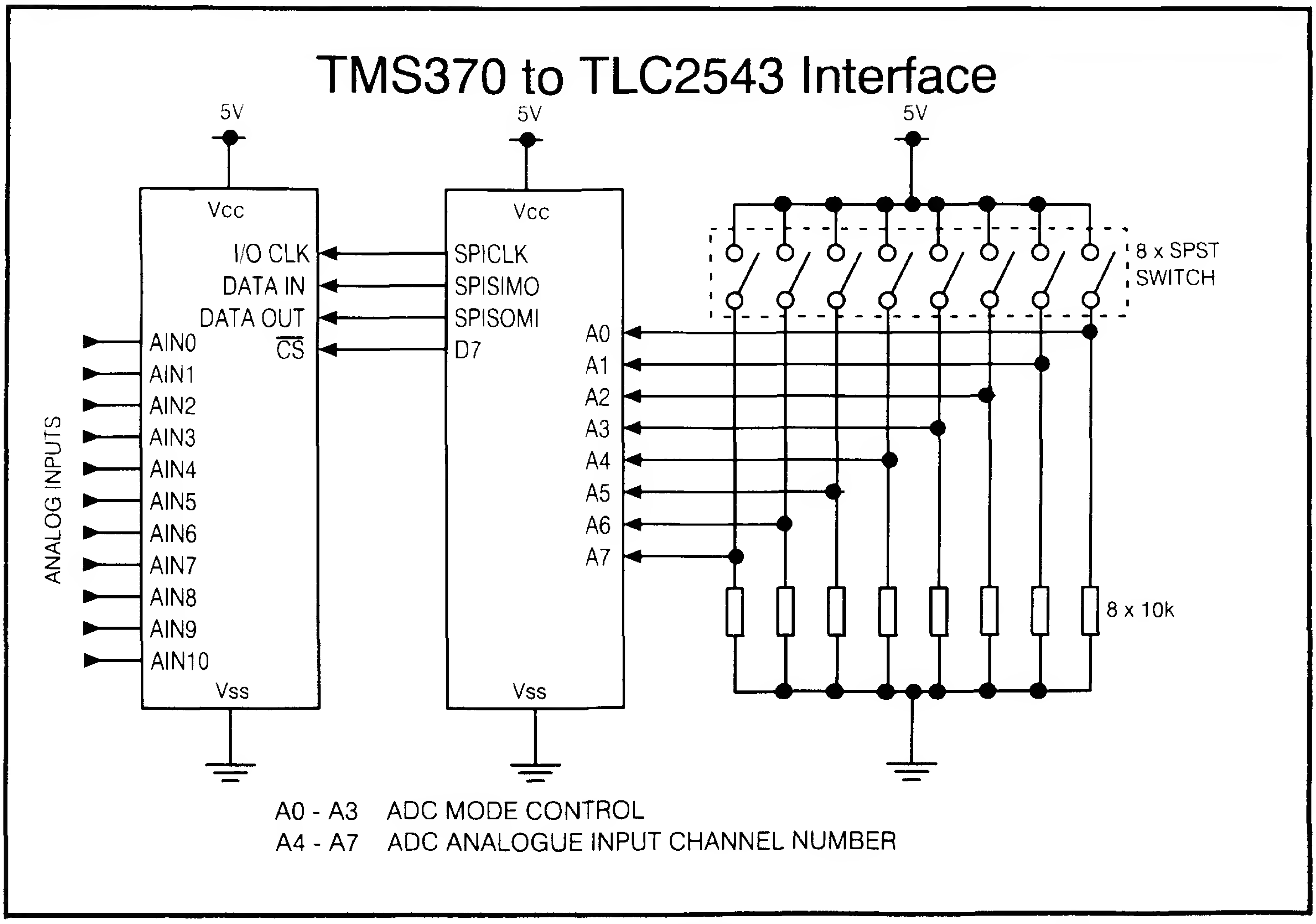

TMS370 to TLC2543 Interface
5V
5V
5V
Vcc
I/O CLK
DATA IN
DATA OUT
CS
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
AIN8
AIN9
AIN10
Vss
ANALOG INPUTS
Vcc
SPICLK
SPISIMO
SPISOMI
D7
A0
A1
A2
A3
A4
A5
A6
A7
Vss
8 x SPST SWITCH
8 x 10k
A0 - A3 ADC MODE CONTROL
A4 - A7 ADC ANALOGUE INPUT CHANNEL NUMBER

Figure 3.20 - TLC2543 to TMS370C010 Interface Circuit

Depending upon the layout of the particular printed circuit board used it may be necessary to insert a small value capacitor of between 50 and 100 pF between the I/O CLOCK input of the TLC2543 and ground. This has the effect of ensuring that data applied to the DATA INPUT pin of the TLC2543 is valid before the positive going transition of the I/O clock.

The positive reference, REF+, to the TLC2543 is provided directly from the Vcc+ supply.

The four digital interface pins, I/O CLOCK, DATA INPUT, DATA OUT and CS, of the TLC2543 connect directly to the SPICLK, SPISIMO, SPISOMI and D7 pins respectively of the TMS370C010.

The operation mode and channel number of the TLC2543 is determined by the serial data which is sent to its DATAIN pin.

2.9.3 Software Description

List 4. contains the software listing for the program which controls the interface illustrated in Figure 3.20 The software consists of the main program and three subroutines called "DATAIN", "ADC" and "STORE". "DATAIN" reads in the channel select and mode control data into a holding register and maps the channel select number to a corresponding pair of registers between R64 and R91. The mapping vector is held in register R10. "ADC" provides the chip select pulse, controls the SPI operation and puts the MSByte and LSByte of each conversion result into registers R20 and R21 respectively. "STORE" puts the MSByte into the even number register and the LSByte into the odd number register mapped by the contents of register R10.

The user can put channel select and ADC mode control data into the holding register within the microcontroller, via the 8-bit wide Port A bi-directional I/O port, using a bank of eight toggle switches as shown in Figure 3.20. Alternatively, the mode and channel data can be sent to the microcontroller holding register via the asynchronous serial communications interface (SCI). This option is available only on those versions of the TMS370, such as the TMS370C020, which include both SPI and SCI interfaces. Additional software to control the SCI must be appended to the software shown in List 4. to provide this method of control.

2.9.4 Opto-Isolated 12-bit Data Acquisition System

The serial nature of the data flow between the TLC2543 analog to digital converter and the accompanying microcontroller makes this ADC an ideal choice for isolated 12-bit data acquisition. Figure 6. shows an opto-isolated system which uses four optocouplers to provide a 3 kV isolation barrier.

Note that the optocoupler which routes conversion result data from the TLC2543 to the microcontroller is a single device and does not share the same piece of silicon with any of the other opto-couplers used. This ensures that the full 3 kV of isolation is maintained between ADC and microcontroller.

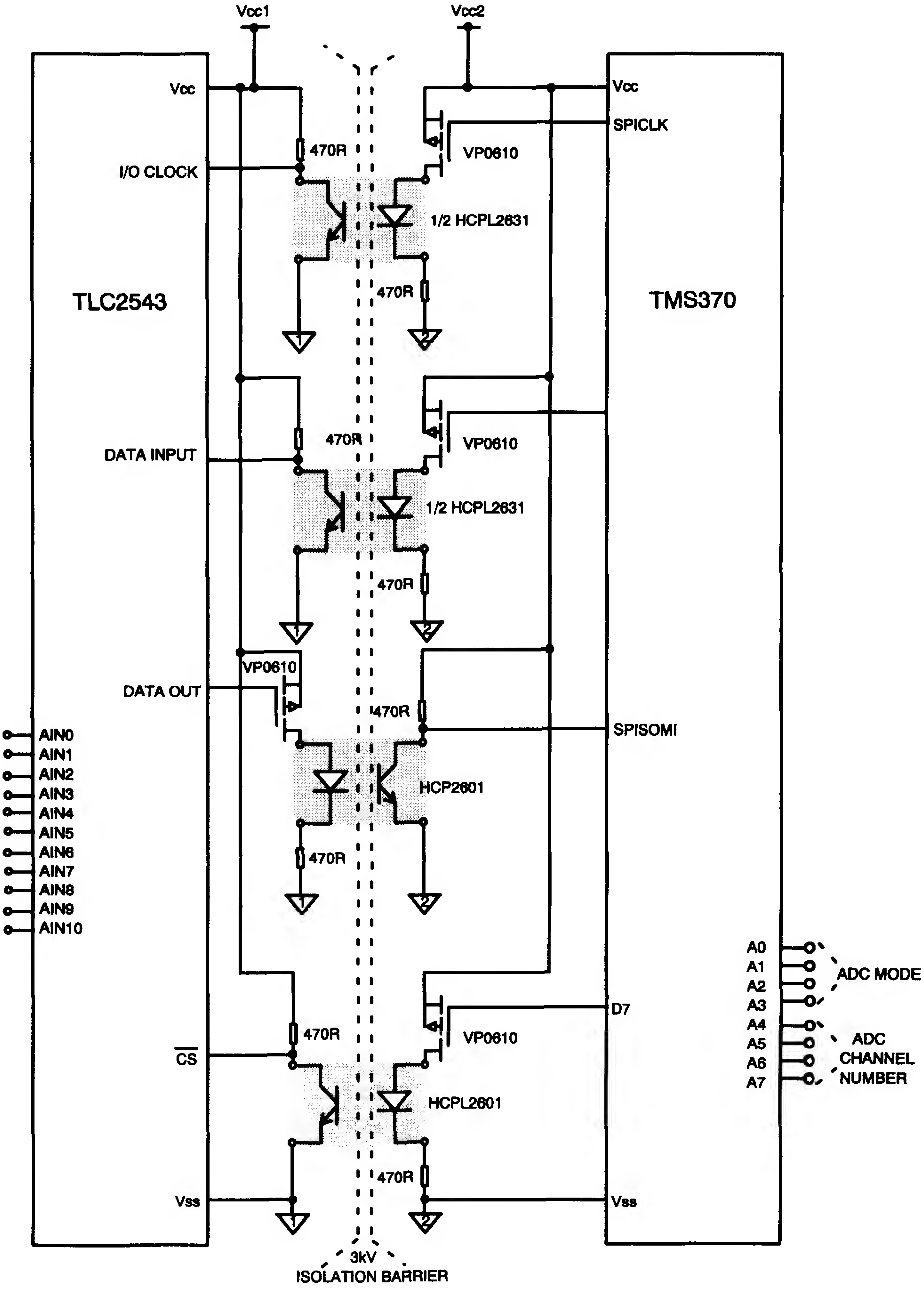

Vcc1
Vcc2
Vcc
I/O CLOCK
DATA INPUT
DATA OUT
CS
Vss
TLC2543
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
AIN8
AIN9
AIN10
470R
VP0610
1/2 HCPL2631
HCP2601
HCPL2601
Vcc
SPICLK
SPISOMI
D7
Vss
TMS370
A0
A1
A2
A3
A4
A5
A6
A7
ADC MODE
ADC CHANNEL NUMBER
3kV ISOLATION BARRIER

Figure 3.21 - Opto-Isolated 12-bit Data Acquisition System

List 4.

```
LINE    LOC    OBJ                  SOURCE

  1                                ;* * * * * * * * * * * * * * * *
  2                                ;*                              *
  3                                ;* TLC2543 to TMS 370Cx10 Interface Program   *
  4                                ;*                              *
  5                                ;* This program reads channel select and mode *
  6                                ;* control data (provided by toggle switches) *
  7                                ;* into the microcontroller, using subroutine *
  8                                ;* DATAIN.                                    *
  9                                ;* It then provides the control signals to the*
 10                                ;* TLC2543 to perform a 12 bit analog to      *
 11                                ;* conversion, using subroutine ADC.          *
 12                                ;* It finally stores the MSByte and LSByte of *
 13                                ;* each conversion in consecutive even and odd*
 14                                ;* number registers respectively starting at  *
 15                                ;* R64 corresponding to channel 0, using      *
 16                                ;* subroutine STORE.                          *
 17                                ;* * * * * * * * * * * * * * * *
 18          0030                  SPICCR  .EQU P030        ;* * * * * * * *
 19          0031                  SPICTL  .EQU P031        ;*               *
 20          0037                  SPIBUF  .EQU P037        ;*               *
 21          0039                  SPIDAT  .EQU P039        ;*               *
 22          003d                  SPIPC1  .EQU P03D        ;*               *
 23          003e                  SPIPC2  .EQU P03E        ;* Name Peripheral *
 24          003f                  SPIPRI  .EQU P03F        ;* Registers     *
 25          0021                  APORT2  .EQU P021        ;*               *
 26          0022                  ADATA   .EQU P022        ;*               *
 27          0023                  ADIR    .EQU P023        ;*               *

LINE   LOC   OBJ                   SOURCE

 28          002c                  DPORT1  .EQU P02C        ;*               *
 29          002d                  DPORT2  .EQU P02D        ;*               *
 30          002e                  DDATA   .EQU P02E        ;*               *
 31          002f                  DDIR    .EQU P02F        ;* * * * * * * *
 32          7ffe                  RESET   .EQU 7FFEH       ;Reset vector named
 33          2e                    CSBIT   .DBIT 7,DDATA    ;TLC2543 Chip Select bit
 34                                                         ;named CSBIT
 35                                ;
 36                                ;
 37
 38  4000                                  .TEXT 4000H      ;Start program at 4000H
 39                                ;Main Program
 40  4000    5260                  START   MOV #60H,B       ;
 41  4002    fd                            LDSP             ;Set SP to address 60H
 42  4003  * 88400000                      MOVW #4000H,A
 43  4007    8b7ffe                        MOV A,RESET      ;Set reset vector
 44  400a    b5                            CLR A
 45  400b    2121                          MOV A,APORT2
 46  400d    2123                          MOV A,ADIR
 47  400f    f7802f                        MOV #080H,DDIR
 48  4012    2280                          MOV #80H,A
 49  4014    2130                          MOV A,SPICCR
 50  4016    2207                          MOV #07,A        ;Configure SPI for 8-bit
 51  4018    2130                          MOV A,SPICCR     ;character length.
 52  401a    2203                          MOV #03,A        ;Configure SPICLK
 53  401c    213d                          MOV A,SPIPC1     ;function and direction.
 54  401e    2222                          MOV #22H,A       ;Configure SPISOMI and
 55  4020    213e                          MOV A,SPIPC2     ;SPISIMO pin functions.
 56          31                    SPIF    .DBIT 6,SPICTL   ;SPI INT FLAG named SPINTF
 57          0b                    MSLSB   .DBIT 1,R11      ;Bit 1 of R11 named MSLSB
 58  4022   '8e402d                        CALL DATAIN
 59  4025   '8e403e                        CALL ADC
 60  4028   '8e409d                        CALL STORE
 61  402b   '00d3                          JMP START
 62
 63                                ;
 64                                ;Subroutine :- DATAIN
```

```
                   ;
402d   9122        DATAIN   MOV ADATA,B      ;Read ADC mode/channel
402f   d10b                 MOV B,R11        ;Put ADC mode/channel
                                             ;in R11
4031   53f0                 AND #0F0H,B      ;Retain channel number
4033   cc                   RR B             ;*  *  *  *  *  *  *  *  *
4034   cc                   RR B             ;* Map channel numbers   *
4035   cc                   RR B             ;* to registers R64-R91  *
4036   cc                   RR B             ;* R10 contains storage  *
4037   5c02                 MPY #002,B       ;* address               *
4039   5840                 ADD #40H,B       ;* Even numbers - MS Byte*
403b   d10a                 MOV B,R10        ;* Odd numbers - LS Byte *
                                             ;*  *  *  *  *  *  *  *  *
403d   f9                   RTS
                   ;
                   ;Subroutine :- ADC
                   ;
403e   2203        ADC      MOV #003H,A
4040   a4802e               SBIT1 CSBIT      ;Set ADC Chip Select high.
4043   b2          LOOP1    DEC A            ;Chip Select stays high
4044  '06fd                 JNE LOOP1        ;while A is not 0.
4046   c5                   CLR B
4047   512e                 MOV B,DDATA      ;CS goes low
4049   2207                 MOV #7,A
404b   2131                 MOV A,SPICTL     ;Enable SPI transmission
404d  '76020b19             JBIT1 MSLSB,LS1ST
4051   120b                 MOV R11,A
4053   2139                 MOV A,SPIDAT
                   ;        MOV R11,SPIDAT   ;Send mode/channel data
                                             ;to TLC2543
4055  'a74031fc    FLAG1    JBIT0 SPIF,FLAG1;If SPIF=0, repeat check.
4059   a21437               MOV SPIBUF,R20   ;Put received MS Byte
                                             ;in R20
405c   71390b               MOV R11,SPIDAT   ;Send mode/channel data
                                             ;to TLC2543
405f  'a74031fc    FLAG2    JBIT0 SPIF,FLAG2;If SPIF=0, repeat check.
4063   a21537               MOV SPIBUF,R21   ;Put received LS Byte
                                             ; in R21
4066  '77020b32             JBIT0 MSLSB,RETURN ;If MSLSB=0, go
                                               ;to RETURN
406a   120b        LS1ST    MOV R11,A
406c   2139                 MOV A,SPIDAT
406e  'a74031fc    FLAG3    JBIT0 SPIF,FLAG3;If SPIF=0, repeat check.
4072   a21537               MOV SPIBUF,R21   ;Put received LS Byte
                                             ;in R21
4075   120b                 MOV R11,A
4077   2139                 MOV A,SPIDAT
4079  'a74031fc    FLAG4    JBIT0 SPIF,FLAG4;If SPIF=0, repeat check.
407d   a21437               MOV SPIBUF,R20   ;Put received MS Byte
                                             ;in R20
4080   2208                 MOV #08,A        ;*  *  *  *  *  *  *  *
4082   d516                 CLR R22          ;*                     *
4084   dd14        LOOP2    RRC R20          ;*  Reformat MS Byte   *
4086   df16                 RLC R22          ;*                     *
4088   b2                   DEC A            ;*  Put result in R20  *
4089  '06f9                 JNZ LOOP2        ;*                     *
408b   421614               MOV R22, R20     ;*  *  *  *  *  *  *  *
408e   2208                 MOV #08,A        ;*  *  *  *  *  *  *  *
4090   d517                 CLR R23          ;*                     *
4092   dd15        LOOP3    RRC R21          ;*  Reformats LS Byte  *
4094   df17                 RLC R23          ;*                     *
4096   b2                   DEC A            ;*  Put result in R21  *
4097  '06f9                 JNZ LOOP3        ;*                     *
4099   421715               MOV R23,R21      ;*  *  *  *  *  *  *  *
409c   f9          RETURN   RTS
                   ;
                   ;Subroutine :- STORE
                   ;
409d   1214        STORE    MOV R20,A        ;Put MS Byte into even
409f   9b0a                 MOV A,@R10       ;address contained in R10
40a1   d30a                 INC R10          ;(R10)+1
40a3   1215                 MOV R21,A        ;Put LS Byte into odd
```

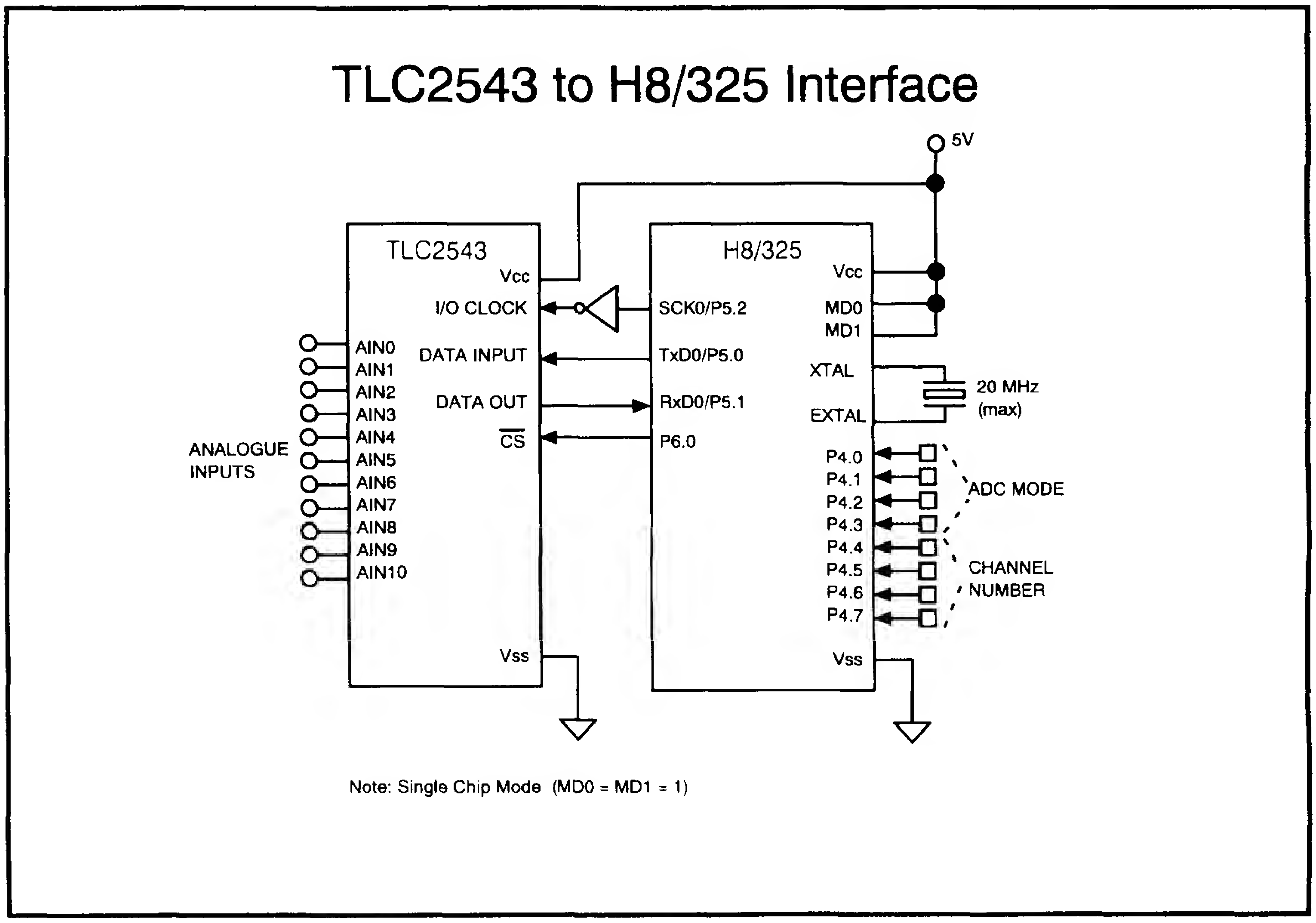
```
40a5    9b0a                        MOV A,@R10      ;address contained in R10
40a7    f9                          RTS
                                    .END
```

2.10 TLC2543 to H8/325 Microcontroller Interface

2.10.1 Microcontroller Features

The individual members of the H8 family of microcontrollers can be differentiated by various criteria, for example the inclusion or otherwise of an on-board 8 bit resolution analog to digital converter (ADC). Those members which include an ADC generally cost between 10 and 20 percent more than their counterparts which do not.

System requirements such as ADC resolution, remote location of ADC, flexibility and total cost all influence the final choice of microcontroller architecture. The H8/325, used for this application report, does not include on-board ADC but provides 1K of RAM, 32K of ROM and two serial I/O ports. It is therefore well suited to interfacing with the TLC2543 serial output ADC.


TLC2543 to H8/325 Interface
5V
TLC2543
Vcc
I/O CLOCK
DATA INPUT
DATA OUT
$\overline{CS}$
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
AIN8
AIN9
AIN10
ANALOGUE INPUTS
Vss
H8/325
Vcc
SCK0/P5.2
TxD0/P5.0
RxD0/P5.1
P6.0
MD0
MD1
XTAL
EXTAL
20 MHz (max)
P4.0
P4.1
P4.2
P4.3
P4.4
P4.5
P4.6
P4.7
ADC MODE
CHANNEL NUMBER
Vss

Note: Single Chip Mode (MD0 = MD1 = 1)

Figure 3.22 - TLC2543 to H8/300 Microcontroller Interface Circuit

2.10.2 Interface Circuit

Figure 3.22 illustrates a typical 12-bit data acquisition system which uses the H8/325 microcontroller to co-ordinate the operation of the TLC2543 ADC via one of its serial (SCI) ports. The circuit uses the H8's 8 bit parallel I/O Port 4 to route ADC channel and mode information into the microcontroller. This information could be provided by a host system data bus or, as in Figure 3.20, by a bank of eight manually operated toggle switches situated on the same printed circuit board as the microcontroller.

2.10.3 Software Description

List 5. shows the program which was written to co-ordinate the interface. It uses three subroutines to implement the overall interface to the TLC2543. The first of these is called "DATAIN" which reads ADC channel and mode information into the microcontroller. It also maps converter channel numbers to corresponding addresses in RAM where conversion results can be stored. In this case the addresses from 0040H to 0067H were chosen to store the results. The most significant byte of each result is placed in an even address and the least significant byte of each result is placed in the corresponding adjacent odd address.

The conversion result of each channel is stored in left justified format and therefore occupies the upper 12 bits of the 16 bit words which occupy even addresses from 0040H up to 0066H.

The second subroutine to be used is "ADC". This begins by producing a chip-select high pulse. The trailing negative edge of this pulse is rapidly followed by the transmission of channel and mode information to the converter.

List 5.

```
 LOC   OBJ      SOURCE

               ;*  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *
               ;*                                                           *
               ;*     TLC2543 to H8 Microcontroller Interface Program.      *
               ;*                                                           *
               ;*  This program contains subroutines "DATAIN", "ADC",       *
               ;*  "FORMAT" and "STORE".                                    *
               ;*  "DATAIN" reads channel number and mode data into the     *
               ;*   microcontroller via Port4. "ADC" controls A to D        *
               ;*   conversion. "FORMAT" changes conversion results from    *
               ;*   LSB first format to MSB first format. "Store" places    *
               ;*   results in memory addresses 40 to 5B (MS Bytes in even *
               ;*   addresses, LS Bytes in odd addresses) according to      *
               ;*   channel number.                                         *
               ;*  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *
               ;
               ;  * Define special function register names *
               ;
FFDD           RDR     EQU H'FFDD              ;Receive Data Register - RDR
FFDB           TDR     EQU H'FFDB              ;Transmit Data Register - TDR
FFD8           SMR     EQU H'FFD8              ;Serial Mode Register - SMR
FFDA           SCR     EQU H'FFDA              ;Serial Control Register - SCR
FFDC           SSR     EQU H'FFDC              ;Serial Status Register - SSR
FFD9           BRR     EQU H'FFD9              ;Bit Rate Register - BRR
FFB8           P5DDR   EQU H'FFB8              ;Port5 Data Direction Register
FFBA           P5DR    EQU H'FFBA              ;Port5 Data Register - P5DR
FFB5           P4DDR   EQU H'FFB5              ;Port4 Data Direction Register
FFB7           P4DR    EQU H'FFB7              ;Port4 Data register - P4DR
FFB9           P6DDR   EQU H'FFB9              ;Port6 Data Direction register
FFBB           P6DR    EQU H'FFBB              ;Port6 Data Register


1000                   ORG H'1000              ;Sets start of program
               ;
               ;  * Main Program *
               ;
1000 79001000          MOV.W #H'1000, R0
               ;       MOV.W R0, @H'0000       ;Sets reset vector to START
1004 7907FD00          MOV.W #H'FD00, SP       ;Sets contents of Stack Pointer
1008 F984      START   MOV.B #H'84, R1L        ;* * * * * * * * * * * * * * * *
```

```
100A 39D8                   MOV.B R1L, @SMR:8       ;* Sets up serial port         *
100C F931                   MOV.B #H'31,R1L         ;* registers for simultaneous*
100E 39DA                   MOV.B R1L, @SCR:8       ;* transmit and receive        *
1010 F901                   MOV.B #H'01,R1L         ;*                             *
1012 39D9                   MOV.B R1L, @BRR:8       ;* * * * * * * * * * * * * * * *
1014 F901                   MOV.B #H'01, R1L        ;Sets R1(Low Byte) to 01H
1016 6A89FFB9               MOV.B R1L, @P6DDR       ;Set Bit0 of Port6 as Output
101A 5E001082               JSR @DATAIN:16          ;Read in ADC channel/mode data
101E 5E00102C               JSR @ADC:16             ;Do A/D conversion
1022 5E0010B4               JSR @FORMAT:16          ;Reformat A/D conversion result
1026 5E0010AC               JSR @STORE:16           ;Store A/D conversion result
102A 40DC                   BRA START               ;Repeat above routine.
                   ;
                   ; * Subroutine "ADC" which controls the conversion process *
                   ;
102C FA05          ADC      MOV.B #H'05, R2L        ;Put 05 in R2L
102E 7FBB7000               BSET #0, @P6DR:8        ;TLC2543 chip select goes high
1032 1A0A          CSHIGH   DEC R2L                 ;(R2L) - 1
1034 46FC                   BNE CSHIGH              ;If not zero, CS stays high
1036 7FBB7200               BCLR #0, @P6DR:8        ;TLC2543 chip select goes low
103A 6A0CFFB7               MOV.B @P4DR, R4L        ;Puts channel/mode data in R4L
103E 731C                   BTST #1, R4L            ;Is LSBF of channel/mode data 0
1040 461E                   BNE LSBYTE              ;If not, do LSBYTE first
1042 7EDC7370      MSBYTE   BTST #7, @SSR:8         ;Is TDR empty ?
1046 47FA                   BEQ MSBYTE              ;If not empty, repeat check.
1048 34DB                   MOV.B R4H, @TDR:8       ;Put channel/mode data in TDR
104A 7FDC7270               BCLR #7, @SSR:8         ;Reset TDRE bit of SSR to 0
104E 7EDC7360      TESTB61  BTST #6, @SSR:8         ;Is receive shift reg. empty ?
1052 47FA                   BEQ TESTB61             ;If not empty, repeat check
1054 23DD                   MOV.B @RDR:8, R3H       ;Put MS Byte of conversion
                                                    ;result in R3H
1056 7FDC7260               BCLR #6, @SSR:8         ;Reset RDRF bit of SSR to 0
105A 68D3                   MOV.B R3H, @R5          ;Put MS Byte in even address
                                                    ;mapped by channel number.
105C 731C                   BTST #1, R4L            ;Is LSBF of channel/mode data 0
105E 4620                   BNE RETURN              ;If not, return from subroutine
1060 7EDC7370      LSBYTE   BTST #7, @SSR:8         ;Is TDR empty ?
1064 47FA                   BEQ LSBYTE              ;If not empty, repeat check
1066 34DB                   MOV.B R4H, @TDR:8       ;Put channel/mode data in TDR
1068 7FDC7270               BCLR #7, @SSR:8         ;Reset TDRE bit of SSR to 0
106C 7EDC7360      TESTB62  BTST #6, @SSR:8         ;Is receive shift reg. empty ?
1070 47FA                   BEQ TESTB62             ;If not empty, repeat check
1072 0A0D                   INC R5L                 ;(R5L) + 1
1074 2BDD                   MOV.B @RDR:8, R3L       ;Put LS Byte of conversion
                                                    ;result in R3L
1076 7FDC7260               BCLR #6, @SSR:8         ;Reset RDRF bit of SSR to 0
107A 68DB                   MOV.B R3L, @R5          ;Put LS Byte in odd address
                                                    ;mapped by channel number.
107C 731C                   BTST #1, R4L            ;Is LSBF of channel/mode data 0
107E 46C2                   BNE MSBYTE              ;If not, go to MSBYTE
1080 5470          RETURN   RTS                     ;Return from subroutine
                   ;
                   ; * Subroutine "DATAIN" which reads in ADC channel/mode data *
                   ;
1082 79040000      DATAIN   MOV.W #H'0000, R4
1086 79050000               MOV.W #H'0000, R5
108A 6A0CFFB7               MOV.B @P4DR, R4L        ;Puts channel/mode data in R4L
108E 0CCD                   MOV.B R4L, R5L          ;Puts (R4L) in R5L
1090 110D                   SHLR R5L                ;*  *  *  *  *  *  *  *  *  *
1092 110D                   SHLR R5L                ;* Retain only channel        *
1094 110D                   SHLR R5L                ;* number in R5L              *
1096 110D                   SHLR R5L                ;*  *  *  *  *  *  *  *  *  *
1098 79060002               MOV.W #0002, R6         ;*  *  *  *  *  *  *  *  *  *
109C 50E5                   MULXU R6L, R5           ;* Maps channel numbers to  *
109E 8D40                   ADD.B #H'40, R5L        ;* even addresses 40H to 5AH*
                                                    ;* Put address in R5L       *
                                                    ;*  *  *  *  *  *  *  *  *  *
10A0 F008                   MOV.B #H'08, R0H        ;Put 08 in R0H
10A2 110C          NEXTBIT  SHLR R4L                ;*  *  *  *  *  *  *  *  *  * *
10A4 1204                   ROTXL R4H               ;* Reformats channel/mode data*
10A6 1A00                   DEC R0H                 ;* from MSB first to LSB first*
10A8 46F8                   BNE NEXTBIT             ;*  *  *  *  *  *  *  *  *  * *
```

```
10AA 5470              RTS
               ;
               ; * Subroutine "STORE" stores A/D conversion results in RAM *
               ;
10AC 68D3      STORE   MOV.B R3H, @R5          ;Store MS Byte in even address
                                               ;corresponding to channel
                                               ;number
10AE 0A0D              INC R5L                 ;(R5) + 1
10B0 68DB              MOV.B R3L, @R5          ;Store LS Byte in odd address
                                               ;corresponding to channel
                                               ;number
10B2 5470              RTS                     ;Return from subroutine
               ;
               ; * Subroutine "FORMAT" changes received data format   *
               ; * ( LSB first ) into MSB first format                *
               ;
10B4 F008      FORMAT  MOV.B #H'08, R0H        ;Put 08 in R0H
10B6 1103      LOOP1   SHLR R3H                ;*  *  *  *  *  *  *  *  *
10B8 1207              ROTXL R7H               ;*                       *
10BA 1A00              DEC R0H                 ;*   Reformats MSBYTE    *
10BC 46F8              BNE LOOP1               ;*                       *
10BE 0C73              MOV.B R7H, R3H          ;*  *  *  *  *  *  *  *  *
10C0 F008              MOV.B #H'08, R0H        ;Put 08 in R0H
10C2 110B      LOOP2   SHLR R3L                ;*  *  *  *  *  *  *  *  *
10C4 120F              ROTXL R7L               ;*                       *
10C6 1A00              DEC R0H                 ;*   Reformats LSBYTE    *
10C8 46F8              BNE LOOP2               ;*                       *
10CA 0CFB              MOV.B R7L, R3L          ;*  *  *  *  *  *  *  *  *
10CC 5470              RTS                     ;Return from subroutine
10CE                   END
```

2.11 TLC2543 to MC68HC11 Microcontroller Interface

2.11.1 Microcontroller Features

All members of the MC68HC11 family of microcontrollers contain an SPI. As is the case for the TMS370, the user is able to set the idle level of the serial clock of the 68HC11. This obviates the need for an external inverter to be used to invert the microcontroller's serial clock output prior to its arrival at the TLC2543's serial clock input.

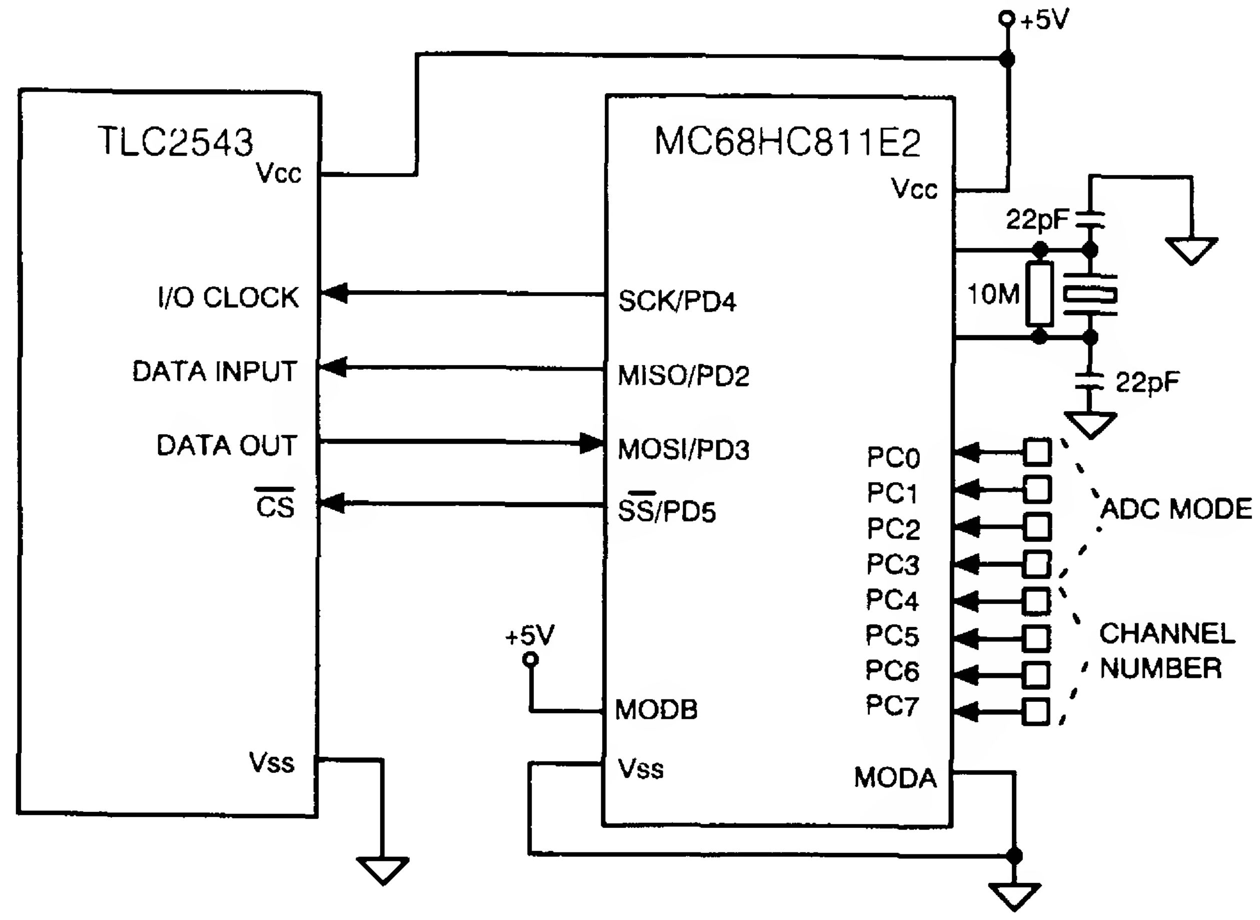
The 68HC11D0, 68HC11D3 and 68HC711D3 versions do not contain an on-board ADC. One of these three devices may prove to be the most cost effective choice when used with the TLC2543. All other versions contain either an 8 or 10 bit resolution ADC.

2.11.2 Interface Circuit

Figure 3.23. shows the circuit diagram of the interface between the 68HC11 and the TLC2543. The microcontroller device type used to illustrate this interface is the 48 pin dual in line version of the MC68HC811E2.

The Master In Slave Out (*MISO*), Master Out Slave In (*MOSI*) and Serial Clock (SCK) pins of the SPI are available as the alternative, user selectable, functions of port D pins *PD2, PD3*, and *PD4* respectively. When the SPI is configured to operate as a master, the *PD5/SS* pin can be used as an output to drive the chip select ($\overline{CS}$) pin of the TLC2543. This leaves all other bi-directional I/O ports of the microcontroller uncommitted and available for other uses. Note that no extra "glue" logic is required to implement the interface.

TLC2543 to 68HC11 Interface


+5V
TLC2543
Vcc
I/O CLOCK
DATA INPUT
DATA OUT
CS
Vss
MC68HC811E2
Vcc
SCK/PD4
MISO/PD2
MOSI/PD3
SS/PD5
+5V
MODB
Vss
MODA
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
22pF
10M
22pF
ADC MODE
CHANNEL NUMBER

NOTE: 1. CONFIGURED FOR SINGLE CHIP MODE OF OPERATION
2. MAXIMUM SPI DATA RATE = CRYSTAL FREQUENCY / 8

Figure 3.23 - TLC2543 to MC68HC811E2 Microcontroller Interface

2.11.3 Software Description

The listing of the program which was written to co-ordinate and control the interface between the TLC2543 and the 68HC811E2 is shown in List 6. The software consists of the main program and two subroutines named "TLC2543" and "STORE". "TLC2543" begins by providing the ADC's chip select pulse. It then reads in channel/mode data via the port C parallel I/O port and subsequently sends this data to the TLC2543 via the *MOSI* pin of the SPI. At the same time, the first byte of the result from the previous analog to digital conversion is received at the *MISO* pin of the SPI.

List 6.

```
LINE     LOC   OBJ          SOURCE

     A                      * * * * * * * * * * * * * * * * * * * * *
     A                      *                                          *
     A                      * TLC2543 12-bit Serial Out ADC to MC68HC11 Microcontroller *
     A                      *     Interface Program             *
     A                      *                                          *
     A                      * This program contains subroutines "TLC2543" and "STORE".  *
     A                      * "TLC2543" reads in ADC mode control and channel select    *
     A                      * data via Port C. It then sends this data to the TLC2543   *
     A                      * and at the same time receives the result of the previous  *
     A                      * conversion.                                              *
     A                      * "STORE" puts the results into addresses $30 to $4B with   *
     A                      * MSBytes in even addresses and LSBytes in odd addresses.   *
     A                      * Channel 0 result in addresses $30 and $31       *
     A                      * Channel 1 result in addresses $32 and $33 etc.      *
```

```
15 A                 *                                                          *
16 A                 *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *
17 A
18 A      1000       BASEADD   EQU       $1000                Register block start
19 A      0000       PORTA     EQU       $00                  Port A Data Register
20 A      0003       PORTC     EQU       $03                  Port C Data Register
21 A      0007       DDRC      EQU       $07                  Port C Data Dir Reg
22 A      0008       PORTD     EQU       $08                  Port D Data Register
23 A      0009       DDRD      EQU       $09                  Port D Data Dir Reg
24 A      0028       SPCR      EQU       $28                  SPI Control Register
25 A      0029       SPSR      EQU       $29                  SPI Status Register
26 A      002A       SPDR      EQU       $2A                  SPI Data Register
27 A      00F0       MSBYTE    EQU       $F0                  MSBYTE address
28 A      00F1       LSBYTE    EQU       $F1                  LSBYTE address
29 A      00F2       TEMP      EQU       $F2                  TEMP address
30 A 0000
31 A      F800                 ORG       $F800                Start @ $F800
32 A                 * LDS #$0070 Set Stack Pointer
33 A F800 863E       START     LDAA      #$3E                 Load 3EH in AA
34 A F802 A709                 STAA      DDRD,X               Store 3EH in DDRD
35 A F804 8650                 LDAA      #$50                 Load 50H into AA
36 A F806 A728                 STAA      SPCR,X               Set SPI as master
37 A F808 8600                 LDAA      #$00                 Load 00 into AA
38 A F80A A707                 STAA      DDRC,X               Set PORTC - all I/Ps
39 A F80C 1C0820               BSET      PORTD,X#$20          ;ADC CS high
40 A F80F BDF817               JSR       TLC2543              Do A/D conversion
41 A F812 BDF84A               JSR       STORE                Store results
42 A F815 20E9                 BRA       START                Repeat above
43 A
44 A F817 CE1000     TLC2543   LDX       #BASEADD
45 A F81A 8602                 LDAA      #02
46 A F81C 1C0820     CSHIGH    BSET      PORTD,X#$20
47 A                 *  Set Port A bit 6 (TLC2543 CS) high
48 A F81F 4A                   DECA
49 A F820 26FA                 BNE       CSHIGH
50 A F822 1D0820               BCLR      PORTD,X#$20          ADC CS low
51 A F825 1E030210             BRSET     PORTC,X#$02 LSB      Do LSB first
52 A                 *     if LSBF set.
53 A F829 A603       MSB       LDAA      PORTC,X              Load Chan/mode data
54 A F82B A72A                 STAA      SPDR,X               Send the data to ADC
55 A                 *     and receive MSByte
56 A F82D 1F2980FC   LOOP1     BRCLR     SPSR,X#$80 LOOP1     If SPIF=0,
57 A                 *    repeat check
58 A F831 A62A                 LDAA      SPDR,X
59 A F833 97F0                 STAA      MSBYTE               Store MSByte
60 A F835 1E030210             BRSET     PORTC,X#$02 RETURN
61 A                 * If MSB/LSB-first bit = 1, return
62 A F839 A603       LSB       LDAA      PORTC,X              Load chan/mode data
63 A F83B A72A                 STAA      SPDR,X               Send the data to ADC
64 A                 *     and receive LSByte
65 A F83D 1F2980FC   LOOP2     BRCLR     SPSR,X#$80 LOOP2     If SPIF=0,
66 A F841 A62A                 LDAA      SPDR,X               repeat check
67 A F843 97F1                 STAA      LSBYTE               Store LSByte
68 A F845 1E0302E0             BRSET     PORTC,X#$02 MSB
69 A                 * If MSB/LSB-first bit = 1 go to MSB
70 A F849 39         RETURN    RTS
71 A                 *
72 A                 *  S'routine stores MSByte in even address
73 A                 *                   LSByte in odd address
74 A                 *  Channel 0 result in $30 and $31
75 A                 *  Channel 1 result in $32 and $33 etc.
76 A                 *  (Reserve addresses $30-$4B for results
77 A                 *   of all channels)
78 A F84A A603       STORE     LDAA      PORTC,X
79 A F84C CE0030               LDX       #$30
80 A F84F 97F2                 STAA      TEMP
81 A F851 86F0                 LDAA      #$F0
82 A F853 94F2                 ANDA      TEMP
83 A F855 46                   RORA
84 A F856 46                   RORA
85 A F857 46                   RORA
86 A F858 46                   RORA
```

```
87 A F859 16                TAB
88 A F85A 8602              LDAA        #$02
89 A F85C 3D                MUL
90 A F85D DDF2              STD         TEMP
91 A F85F 96F0              LDAA        MSBYTE
92 A F861 A7F2              STAA        TEMP,X
93 A F863 08                INX
94 A F864 96F1              LDAA        LSBYTE
95 A F866 A7F2              STAA        TEMP,X
96 A F868 39                RTS
97 A                        END
```

2.12 TLC2543 to 80C51 Interface

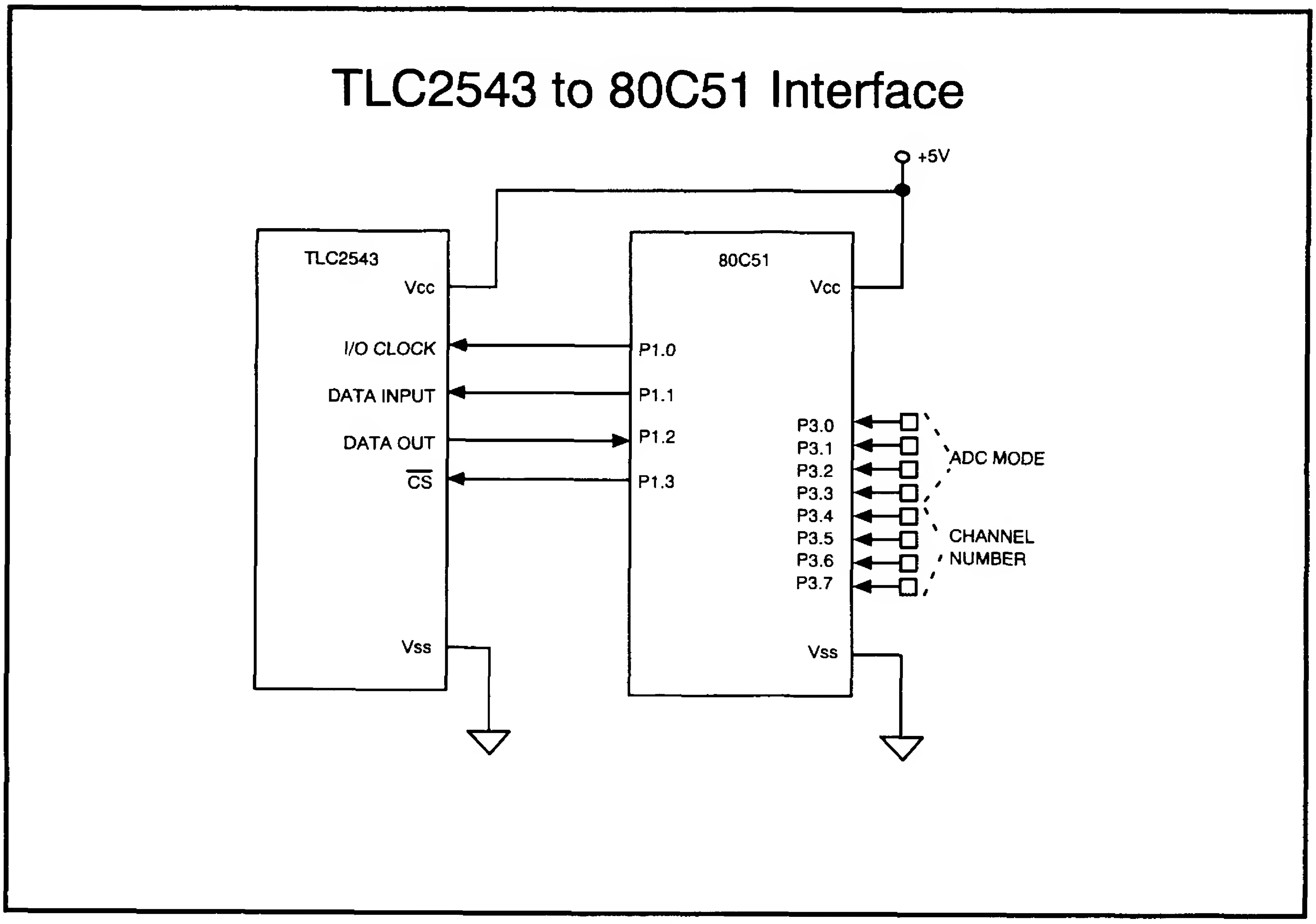

TLC2543 to 80C51 Interface
+5V
TLC2543
Vcc
I/O CLOCK
DATA INPUT
DATA OUT
CS
Vss
80C51
Vcc
P1.0
P1.1
P1.2
P1.3
P3.0
P3.1
P3.2
P3.3
P3.4
P3.5
P3.6
P3.7
ADC MODE
CHANNEL NUMBER
Vss

Figure 3.24 - TLC2543 to 80C51 Microcontroller Interface

2.12.1 Microcontroller Features

The 80C51 microcontroller family does not provide an SPI or equivalent facility. In order to implement the interface with the TLC2543 analog to digital converter it is necessary to use software to synthesise the operation of an SPI. This results in a slower data transfer rate which is governed by the microcontroller's instruction cycle times. These are, in turn, influenced by the clock frequency of the microcontroller. The highest clock frequency possible should therefore be selected for the microcontroller to minimise instruction cycle times and thus optimise the data transfer rate of the interface.

2.12.2 Interface Circuit

Figure 3.24 shows the circuit for the interface of the TLC2543 to the 80C51 microcontroller. The I/O Clock, Data Input and CS inputs to the TLC2543 are provided via the bi-directional parallel Port 1 pins P1.0, P1.1 and P1.3 respectively. Conversion result data from the TLC2543 is received by the 80C51 through the P1.2 pin of Port 1. The channel select/mode data is input to the microcontroller via Port 3.

2.12.3 Software Description

The listing for the program used to control the interface circuit mentioned above is shown in List 7. As for the other microcontroller interface programs, it consists of a main program and two subroutines - "TLC2543" and "STORE".

The main program initialises the directions of the port 1 I/O pins. P1.2 is configured as an input. P1.0, P1.1 and P1.3 are all programmed to perform as outputs. The chip select pin of the TLC2543 is set high by setting P1.3. "TLC2543" is then called. This subroutine contains the instructions which synthesise the SPI function and controls the exchange of data between the microcontroller and the TLC2543. The least significant bit first (LSBF) flag which is bit 1 of the channel select/mode data byte is checked to determine which byte (most significant - MSByte, least significant - LSByte) of the conversion result is to be expected first.

The SPI function is synthesised by using the accumulator in conjunction with the rotate left through carry (RLC) instruction to act as the SPI shift register. The following sequence provides a slow motion version of the SPI function.

The first bit of the first byte of the conversion result is read into the carry (C) bit. The contents of the accumulator is rotated left through carry and the first bit of the channel select/mode data is then output from P1.1. The first pulse of the serial clock is then provided by toggling the P1.0 bit of Port 1 first high and then low. This sequence is repeated a further seven times to complete the transfer of the first byte of data.

The second byte of data is transferred between the TLC2543 and the 80C51 by repeating the entire sequence of eight sets of data transfer and clock pulse. The MSByte is placed in register 2 (R2) and the LSByte is placed in register 3 (R3). The subroutine "STORE" is used to map the MSByte and LSByte conversion results, into even and odd number RAM addresses corresponding to the particular channel number which has been selected.

List 7.

```
LOC   OBJ          SOURCE

                   ;*  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *
                   ;*                                              *
                   ;*  TLC2543 12-bit Serial Out ADC to 80C51      *
                   ;*                                              *
                   ;*  Microcontroller Interface Program           *
                   ;*                                              *
                   ;*  *  *  *  *  *  *  *  *  *  *  *  *  *  *  *
                   ;This program reads mode/channel select data into the
                   ;80C51 via Port 4 and transmits this data to the
                   ;TLC2543 at the same time as reading the result from
                   ;the previous conversion and storing the result in an
                   ;adjacent pair of memory locations from 30H to 4CH.
                   ;MSByte - Even Address  LSByte - Odd Address
                   ;MSByte Channel 0 in 30H, MSByte Channel 1 in 32H etc.
                   ;
0100                       ORG 100H
0100 758150        START:  MOV SP,#50H      ;Initialise Stack Pointer
0103 759004                MOV P1,#04H      ;Initialize port 1 I/O Pins
0106 C290                  CLR P1.0         ;Set I/O clock low
0108 D293                  SETB P1.3        ;Set chip select high
```

```
010A 74FF                   MOV A,#00FFH
010C 3112                   ACALL TLC2543
010E 313F                   ACALL STORE
0110 80EE                   JMP START

0112 ACB0         TLC2543:MOV R4,P3         ;Read mode/channel data into R4
0114 EC                   MOV A,R4          ;and A
0115 C293                 CLR P1.3          ;Set chip select low
0117 20E112               JB ACC.1,LSB      ;If bit 1 of A is 1,
                                            ;do LSByte first
011A 7D08         MSB:    MOV R5,#08        ;Load MS bit counter
011C A292         LOOP1:  MOV C,P1.2        ;Read data bit into carry
011E 33                   RLC A             ;Rotate into accumulator
011F 9291                 MOV P1.1,C        ;Output mode/channel bit
0121 D290                 SETB P1.0         ;Set I/O clock high
0123 C290                 CLR P1.0          ;Set I/O clock low
0125 DDF5                 DJNZ R5,LOOP1     ;Get/send another bit
0127 FA                   MOV R2,A          ;Put MSByte in R2
0128 EC                   MOV A,R4          ;Put mode/channel data in A
0129 20E112               JB ACC.1,RETURN ;
012C 7D08         LSB:    MOV R5,#08        ;Load LS bit counter
012E A292         LOOP2:  MOV C,P1.2        ;Read data bit into carry
0130 33                   RLC A             ;Rotate into accumulator
0131 9291                 MOV P1.1,C        ;Output mode/channel bit
0133 D290                 SETB P1.0         ;Set I/O clock high
0135 C290                 CLR P1.0          ;Set I/O clock low
0137 DDF5                 DJNZ R5,LOOP2     ;Get/send another bit
0139 FB                   MOV R3,A          ;Put LSByte in R3
013A EC                   MOV A,R4          ;Put mode/channel data in A
013B 20E1DC               JB ACC.1,MSB      ;If bit 1 of R4 is 1,
                                            ;do MSbyte next
013E 22           RETURN: RET

013F EC           STORE:  MOV A,R4          ;Put mode/channel data in A
0140 54F0                 ANL A,#0F0H       ;Retain only channel number
0142 C4                   SWAP A            ;Swap high and low nibble of A
0143 75F002               MOV B,#02

0146 A4                   MUL AB
0147 2430                 ADD A,#030H       ;Add 30H to accumulator
0149 F9                   MOV R1,A
014A EA                   MOV A,R2
014B F7                   MOV @R1,A         ;Put MSByte in corresponding
                                            ;even number address :-
                                            ;Channel 0 in address 30H,
                                            ;Channel 1 in address 32H etc.
014C 09                   INC R1
014D EB                   MOV A,R3
014E F7                   MOV @R1,A         ;Put LSByte in corresponding
                                            ;odd number address :-
                                            ;Channel 0 in address 31H,
                                            ;Channel 1 in address 33H etc.
014F 22                   RET
                          END
```

2.13 TLC2543 Analog Considerations

Care should be taken with the design of the printed circuit board lay-out when using 12-bit devices such as the TLC2543. The power supply pin of each analog integrated circuit should be separately decoupled to the analog ground using a 0.1-µF ceramic capacitor. The inclusion of a 10-µF tantalum capacitor in parallel with the ceramic capacitor at each device supply pin is also recommended, particularly in noisy environments.

Separate ground return paths back to the power supply should be used to prevent any noise currents induced by digital components from passing through the analog ground return path.

The important point to remember is that all ground return paths have a finite impedance. This impedance should be kept to a minimum by the use of wide printed circuit board tracks or ground planes where possible. A separate "Star connected" ground topology is recommended for the analog components. This involves connecting each analog component's ground pin to a central "star" point, which can then be connected via a wide printed circuit track to the power supply ground connection.

Digital devices and power switching elements should be kept as far away physically from the analog components as possible. Particular attention should be paid to the use of switching power supplies. The high frequency switching currents which flow in the ground return paths of these space saving power blocks can introduce several LSBs of noise into 12-bit analog circuits. The message here is to either (ideally) use linear regulated power supplies or, if switching regulators must be used, keep them as far as possible from the analog circuitry and carefully decouple their outputs.

Fig 3.25. illustrates a typically grounding scheme for the TLC2543 to TMS370 microcontroller interface.

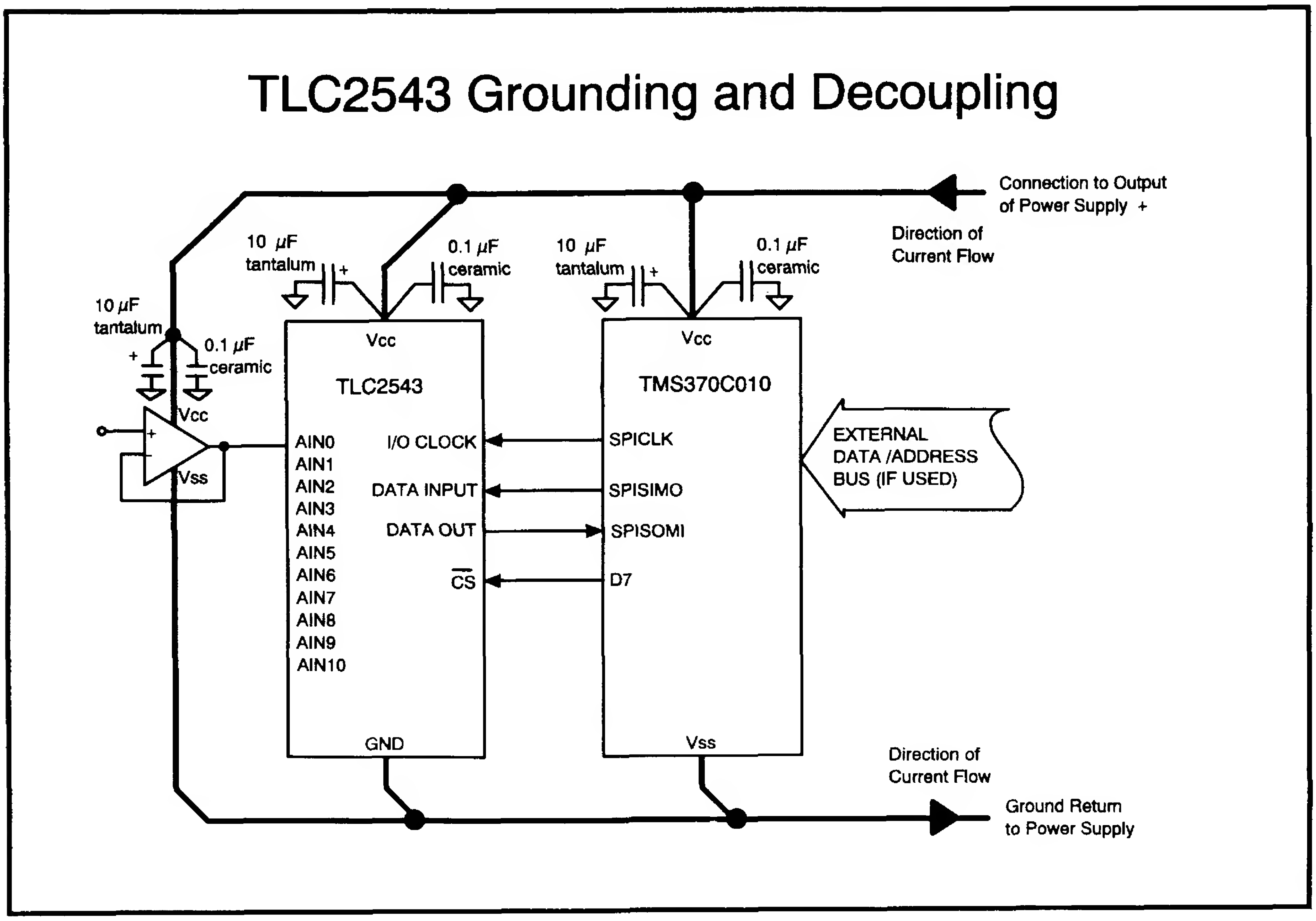

TLC2543 Grounding and Decoupling
Connection to Output of Power Supply +
Direction of Current Flow
10 μF tantalum
+
0.1 μF ceramic
10 μF tantalum
+
0.1 μF ceramic
10 μF tantalum
+
0.1 μF ceramic
Vcc
Vss
+
Vcc
TLC2543
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
AIN8
AIN9
AIN10
I/O CLOCK
DATA INPUT
DATA OUT
CS
GND
Vcc
TMS370C010
SPICLK
SPISIMO
SPISOMI
D7
Vss
EXTERNAL DATA /ADDRESS BUS (IF USED)
Direction of Current Flow
Ground Return to Power Supply

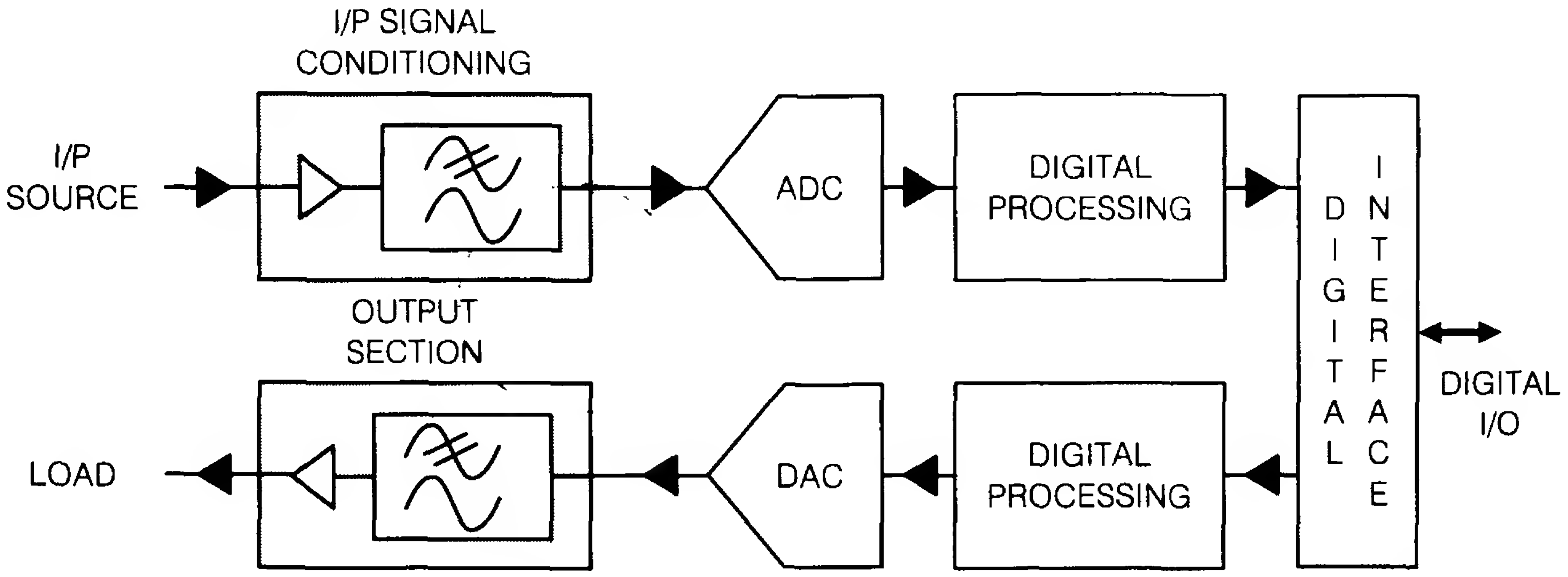
Figure 3.25 - TLC2543 to Microcontroller Interface, Grounding and Decoupling

References

H8/300 User's Manual (1991/2)	Hitachi
Embedded Microcontrollers and Processors Vol 1. (1993)	Intel Corporation
M68HC11 Reference Manual (1991)	Motorola
TMS370 Family Data Manual (1993)	Texas Instruments
TLC2543 Data Sheet (Dec. 1993)	Texas Instruments

3 Analog Interface Circuits for DSP

Analog Interface for DSP


I/P SIGNAL CONDITIONING
I/P SOURCE
ADC
DIGITAL PROCESSING
DIGITAL INTERFACE
DIGITAL I/O
OUTPUT SECTION
LOAD
DAC
DIGITAL PROCESSING

- An Analog Interface Circuit is a complete data-acquisition system on a chip
- It provides an "audio-band" interface from a DSP to the real, analog world

Figure 3.26 - Analog Interface for DSP

3.1 Introduction

Texas Instruments families of Analog Interface Circuits (AIC) for Digital Signal Processors (DSP) are complete data-acquisition systems on a single chip.

The AIC incorporates ADC, DAC, anti-aliasing and anti-imaging filters and input/output amplifiers. They have been developed mainly for "audio-band" (up to 12 kHz bandwidth) system applications which require a high degree of programmability with a simple DSP interface and a highly integrated design that conserves board space.

3.2 Voice-band Audio Processor (VBAP)

TCM320AC3X/4X Voice-Band Audio Processor

Simplified DSP Audio Interface From A Single Supply

- Single supply operation
- Low Power consumption
  40 mW typ
  1.25 mW typ power down
- Low noise (transmit direction)
  10 dBrnC0 max
  70 dBm 0p max
- 13-bit linear or companded mode - Pin selectable
- Direct interface to electret microphone and earpiece

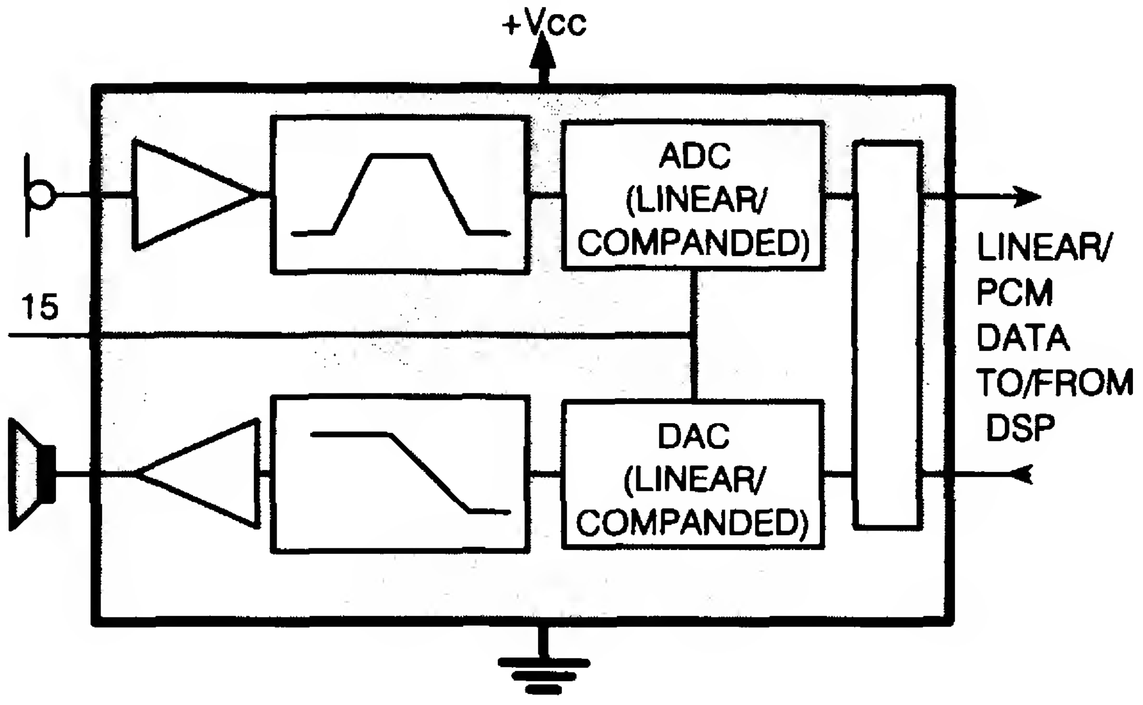


Figure 3.27 - The Voice-band Audio Processor

Many applications using voice-band signals require an efficient interface between analog components and the DSP which operates from a single supply and offers ADC, DAC, pre and post filter stages and on-chip amplifiers. Texas Instruments has developed the TCM320AC3X/4X family of devices to provide the complete voice-band (200 Hz - 3.6 kHz) interface on a single chip. The devices are suitable for a wide range of voice-band data acquisition systems using a DSP including cellular and cordless telephones, answer machines and test equipment.

3.2.1 The Voice-band Audio Processor Building Blocks

The Voice-Band Audio Processor (VBAP) is divided into a transmit and receive section which is controlled from a central timing unit. The input signals from the microphone are amplified via a programmable gain input amplifier to accommodate a range of signal input levels. The amplified signal is passed through an anti-aliasing filter and a high pass filter then converted into digital code. The linear selection pin, when LOW, selects 13-bit linear coding/decoding and, when HIGH, selects companded coding/decoding. Selection of the linear mode of operation reduces the software required in the DSP. The digital data is buffered and clocked out, to the DSP, via the output logic.

The received digital signals are clocked into the device via input logic. The status of the linear selection pin determines if the incoming data is companded and requires decoding or if the data may be transferred directly to the DAC. The analog signal from the DAC is passed through switched capacitor filters, which provide out of band rejection and (sinx)/x correction. Switched capacitor design techniques provide the user with precise audio band pass filtering and low power consumption. The filtered signal is presented to the differential output amplifier which may be connected directly to a piezo speaker.

Both the input and output amplifiers have a mute function which is accessible by the DSP. When the mute function is activated both amplifiers are disabled. In a telephone this function may be used to provide the user with a secrecy function.

The devices offer the user single supply operation and a low power consumption of typical 40 mW (and only 1.25 mW typical in power down mode).

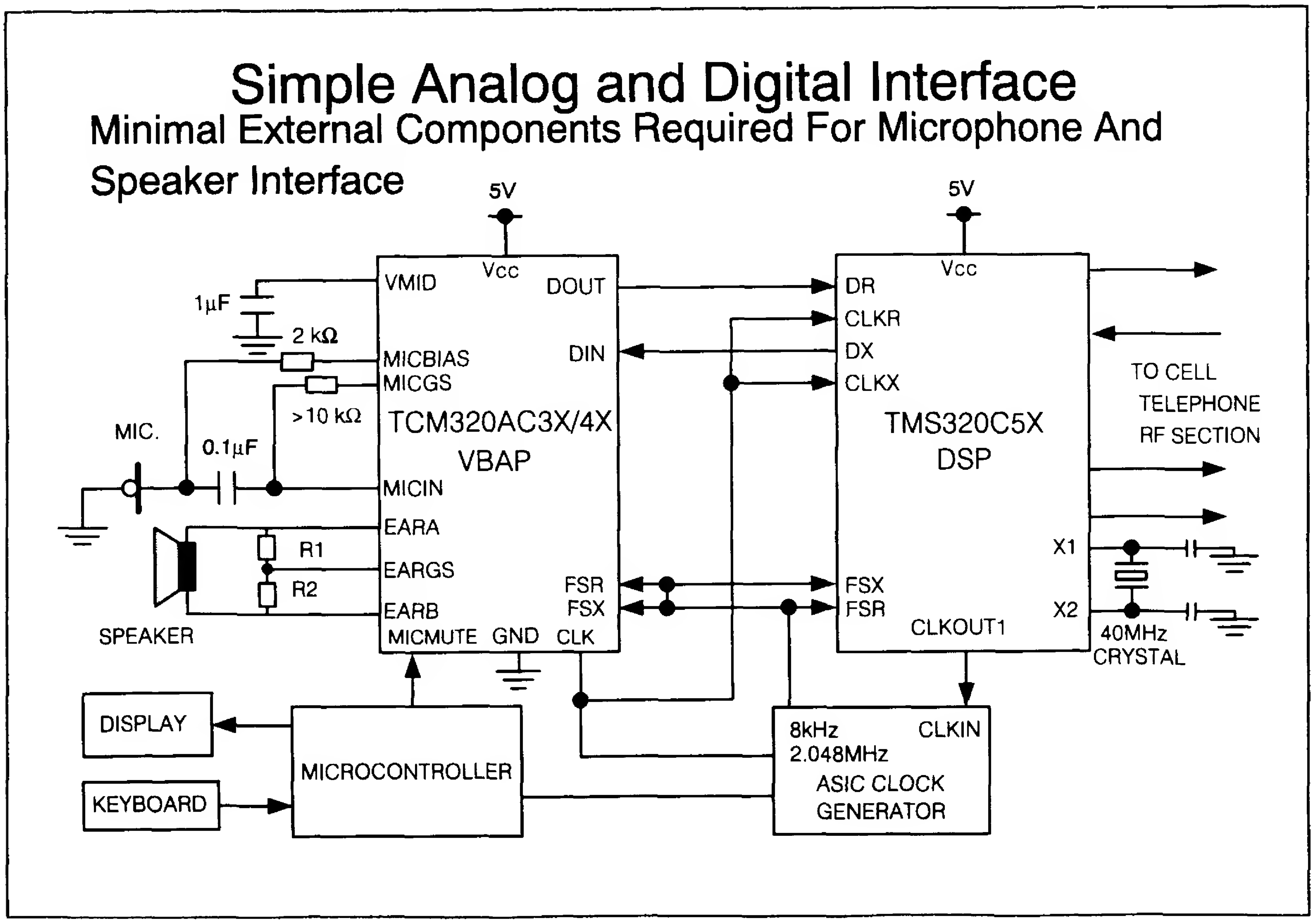

Simple Analog and Digital Interface
Minimal External Components Required For Microphone And Speaker Interface
5V
5V
1µF
2 kΩ
>10 kΩ
MIC.
0.1µF
R1
R2
SPEAKER
VMID
Vcc
DOUT
MICBIAS
DIN
MICGS
TCM320AC3X/4X
VBAP
MICIN
EARA
EARGS
FSR
EARB
FSX
MICMUTE
GND
CLK
DR
Vcc
CLKR
DX
CLKX
TMS320C5X
DSP
FSX
FSR
CLKOUT1
X1
X2
TO CELL
TELEPHONE
RF SECTION
40MHz
CRYSTAL
DISPLAY
KEYBOARD
MICROCONTROLLER
8kHz
CLKIN
2.048MHz
ASIC CLOCK
GENERATOR

Figure 3.28 - Interfacing the VBAP to the load and DSP

The Voice-band Audio Processor is designed to provide a direct interface to the microphone, ear piece and DSP.

The Ear piece Interface.

This interface provides a balanced output from the differential output amplifier which drives a piezo speaker without the need for additional active components.

The output amplifier has adjustable gain-setting via the external resistor network R1 and R2. It is recommended that the value of R1+R2 is set greater than 10 kΩ to reduce loading effects on the amplifier, and less than 100 kΩ to minimise noise and distortion due to the time constant of the parallel resistor combination of R1 and R2 with the capacitance at the gain-set pin *EARGS*.

The output stage may be disabled by using the earphone mute control function. This prevents the audio signal from being sent to the earphone and allows a secrecy function to be incorporated in the system.

The Microphone Interface.

A direct interface is provided to an electret type microphone. The reference voltage for the microphone amplifier and the bias voltage for the electret microphone are generated on-chip. Thus minimising the external circuitry around the device.

When the input amplifier is disabled the device transmits only zero codes.

In the linear mode of operation the microphone interface provides an adjustable volume control, this provides the user with a "soft touch" volume facility. The data word is 16 bits long. The first 13 bits contain the linear data and bits 13-15 allow the volume level to be adjusted in 8 steps between -18 dBm0 and +3 dBm0. In the companded mode of operation the data is transmitted and received in 8-bit words. The mode of operation is pin selectable. Use of the linear mode simplifies software in the DSP.

The DSP Interface.

The Voice-band audio processor provides a standard serial interface to a TMS320 DSP or any other standard DSP. Transmit and receive directions can be operated independently.

The Voice-Band Audio Processor Family

Part Number	Master Clock Frequency (MHz)	Data Conversion	Application
TCM320AC36	2.048	Linear/μ-Law	Low power version
TCM320AC37	2.048	Linear/A-Law	Low power Version
TCM320AC39	2.6	Linear/A-Law	GSM mobile phones
TCM320AC46	2.048	Linear/μ-Law	Standard device for general applications

All devices available in 20 pin dual-in-line and small outline packages, ambient temperature range 0 to 70°C and -40 to +85°C

Figure 3.29 - The VBAP Family

Texas Instruments has released a family of VBAP devices. The distinguishing features between the devices are the frequency of the master clock, the out-of-band rejection characteristics of the filters and the companded format of the digital data. The devices are tailored for use in cordless and cellular telephones in particular AMPS/TACS, CT-2 and GSM systems. Although targeted at these areas the devices are suitable for use in many voice-band data acquisition applications using a DSP; for example, digital encryption, digital voice-band, data storage, instrumentation and ATE.

The VBAP family is available in 20 pin dual-in-line or wide body small-outline packages. The devices are characterised from 0° C to 70° C or -40° C to 85° C.

4 Designing with the TLC320AC01 Analog Interface for DSP

4.1 Introduction

This section was prepared by John Walliker and Julian Daley of University College London. It is based on their experience of using the device as part of a specialised signal processing hearing aid. However the techniques described, for both the analog and digital interfaces, are appropriate for many applications.

Measurements of performance quoted in this application note are those achieved with the particular samples and test set-up. For the full device specification see the TLC320AC01 Data Manual, reference SLAS057A.

Some features of the TLC320AC01 were not used in this design and therefore have not been covered here. They are, phase adjustment and the use of multiple devices.

4.1.1 Overview of device

The TLC320AC01 is a 14-bit resolution, audio frequency (approx. 12-kHz bandwidth) analog interface for DSP with integral anti-aliasing and reconstruction filters. It has a synchronous, serial, digital interface designed for ease of connection to many DSP chips.

The internal circuit configuration and the performance parameters, such as input source, sampling rate, filter bandwidths and gain, are determined by writing in control information to 8 data registers. These registers are used to set-up the device for a given mode of operation and given application. The ADC channel and the DAC channel operate synchronously and data is transferred in 2's complement format.

The anti-aliasing filter is a switched capacitor low-pass filter with a sixth-order elliptic characteristic. The high-pass is a single pole filter which can be switched out if required. There is a 3-pole continuous time filter that precedes the switched capacitor filter to eliminate aliasing caused by sampling in the switched capacitor filter.

The output reconstruction filter is also a switched capacitor low-pass filter with a sixth-order elliptic characteristic and it is followed by a second-order (sinx)/x correction filter. This is followed by a three-pole continuous time filter to eliminate images caused by sampling in the switched capacitor filter.

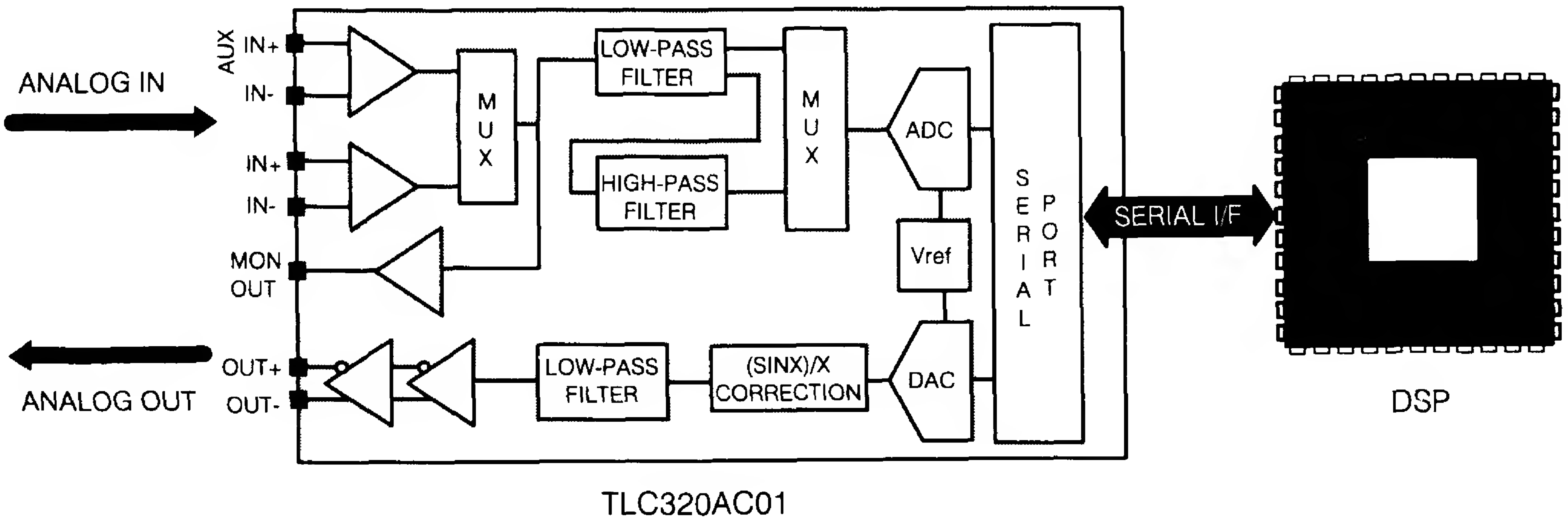
There are three basic modes of operation available:

'Stand-Alone Analog Interface Mode', where the TLC320AC01 generates the shift clock and the frame sync for the data transfers and is the only AIC used.

'Master-Slave Mode', where the master TLC320AC01 generates the shift clock and the frame sync and the rest are slaves to these signals.

'Linear Codec Mode', where the shift clock and the frame sync are generated externally and the timing can be any of the standard codec timing patterns.

TLC320AC01 Analog Interface for DSP



- 14-bit A/D converter
- 14-bit D/A converter
- Anti-aliasing filter
- Anti-imaging filter with
- (sinx)/x correction
- Input and output amplifiers
- Programmable bandwidth, sampling rate, gain, I/P source .
- Single 5V supply
- 70dB typical signal to noise+distortion ratio
- 100mW typical power consumption
- Analog bandwidth up to 10.8kHz

Figure 3.30 - TLC320AC01 Analog Interface for DSP

The TLC320AC01 is available in a standard 28-pin plastic J-lead chip carrier ("FN" suffix) and a 64-pin plastic-quad-flat-pack ("PM" suffix) which is only 1.5 mm thick, making it suitable for use in portable systems.

The device has a maximum power dissipation of 110 mW in the active mode and 10 mW in the Power Down mode. It runs from a single 5-V supply, both for digital and analog circuitry. This is particularly useful for portable equipment, but does require extra care in the design of the analog input and output stages.

4.2 Analog Input

4.2.1 Signal-to-Noise and Signal-to-Distortion Measurements

With the internal gain of the TLC320AC01 set to 0 dB, a full scale signal corresponds to 6 V peak-peak at the analog input (equivalent to $6/(2\sqrt{2}) = 2.12$ V RMS).

The input signal-to-noise ratio of the TLC320AC01 can be expressed in terms of the number of least significant bits (LSB) of noise present in the digital signal, when both its inputs are connected to V_{mid}. The RMS value of the noise was measured on the test boards at 0.5 LSB. This corresponds to a noise voltage of approximately 180 μV RMS at the input (i.e. a signal-to-noise ratio of 81 dB). The intermodulation measurements are shown in Figure 3.31. The stimulus was the sum of a 1 kHz signal at -6 dB referred to full scale plus a 1.2 kHz signal at -12 dB referred to full scale. Distortion products are approx. 80 dB down throughout the pass band. The low frequency peaks that can be seen are multiples of 50 Hz mains interference.

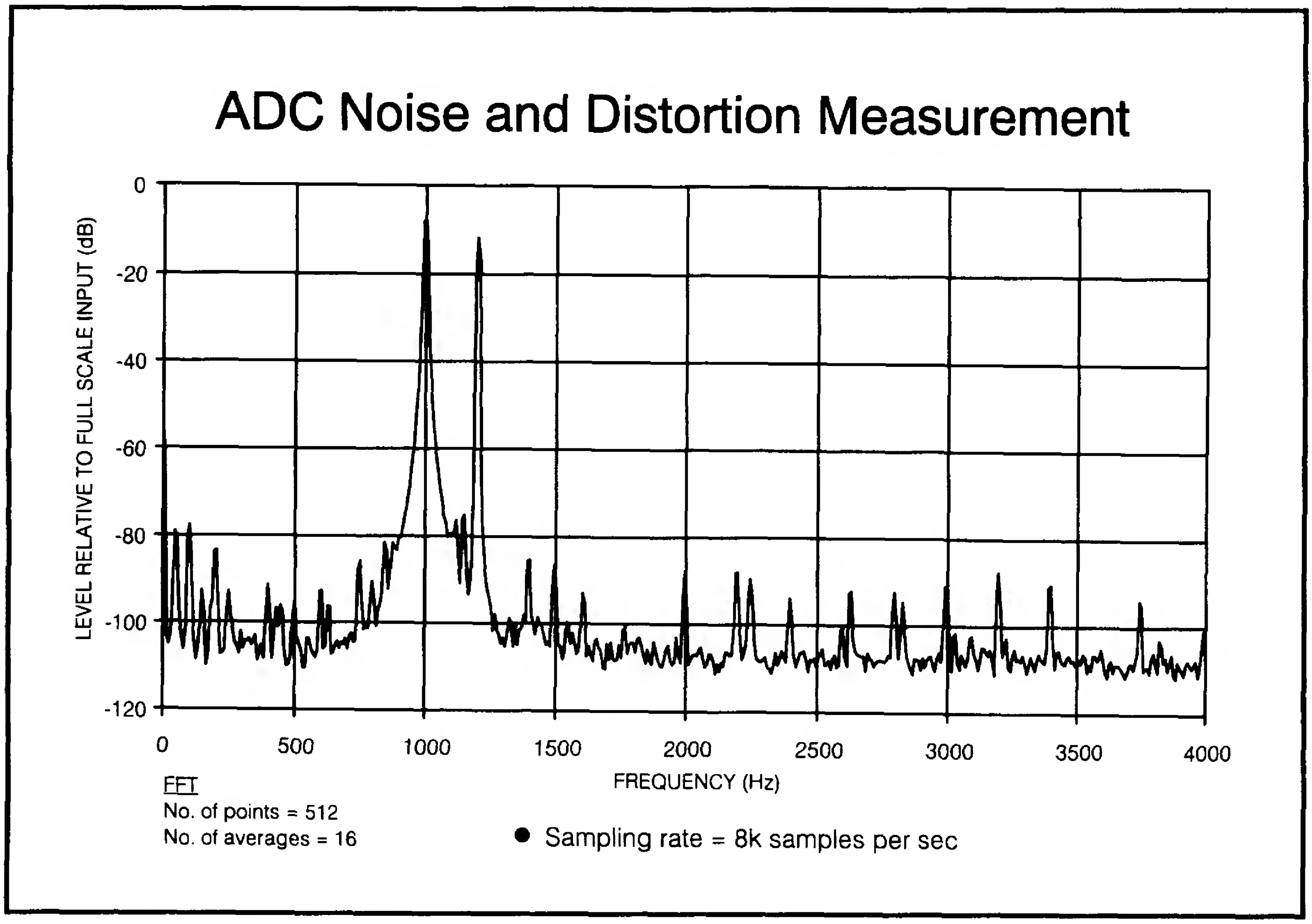


Figure 3.31 - ADC Noise and Distortion Measurement

In the test circuit, the dc accuracy on the samples measured was 14 LSB, equivalent to 5 mV of dc offset.

4.2.2 Input preamp design

Noise Considerations

In order that the input preamp does not significantly affect the noise performance of the system, it should produce a noise level at least 6 dB below the TLC320AC01, (i.e. less than 90 µV RMS) at the TLC320AC01 input.

If we consider the case of a microphone producing 20 mV peak-to-peak at the maximum sound level , we need a preamp with a gain of 6 V / 20 mV = 300 to get a full scale input at the ADC. So the input noise produced by the preamp must be less than 90µV / 300 = 300 nV RMS.

For a preamp with a bandwidth of 10 kHz the input noise voltage should be less than

$$\frac{300nV}{\sqrt{10kHz}} = 3nV / \sqrt{Hz}$$

This noise is made up of the op amp's noise voltage combined with the thermal noise of the equivalent series resistance of the input source. Resistor values need to be carefully chosen, since a 10 kΩ resistor produces thermal noise of 14 nV/$\sqrt{Hz}$ at room temperature. (spectral noise voltage density for a resistor is given by $\sqrt{4KTR}$, where K is Boltzman's constant, T is the absolute temperature and R the resistance). In this case ,a 100-Ω resistor was chosen (producing a thermal noise of 1.4 nV/$\sqrt{Hz}$ at room temperature). A MAX410 op amp was chosen for the first gain stage as this has a noise voltage of 2.4 nV/$\sqrt{Hz}$. Noise voltages combine as the root of the sum of the squares, so the total noise is given by:

$$\sqrt{\left(2.4nV^2 + 1.4nV^2\right)} = 2.8nV / \sqrt{Hz}$$

The gain is split between two op amps. The first, low noise, op amp configured as a non-inverting amplifier with a gain of 100, followed by a second non-inverting stage with a gain of 3. This second op amp does not need such a low noise voltage specification since its input noise is only being amplified by 3. The TLC2272 dual op amp, which has a noise voltage of $9nV / \sqrt{Hz}$, is chosen for its low power consumption, low input offset and well behaved performance under overload. (These op amps do not exhibit the behaviour of Bi FETs which can produce phase reversal of the output when the inputs go out of negative common mode range).

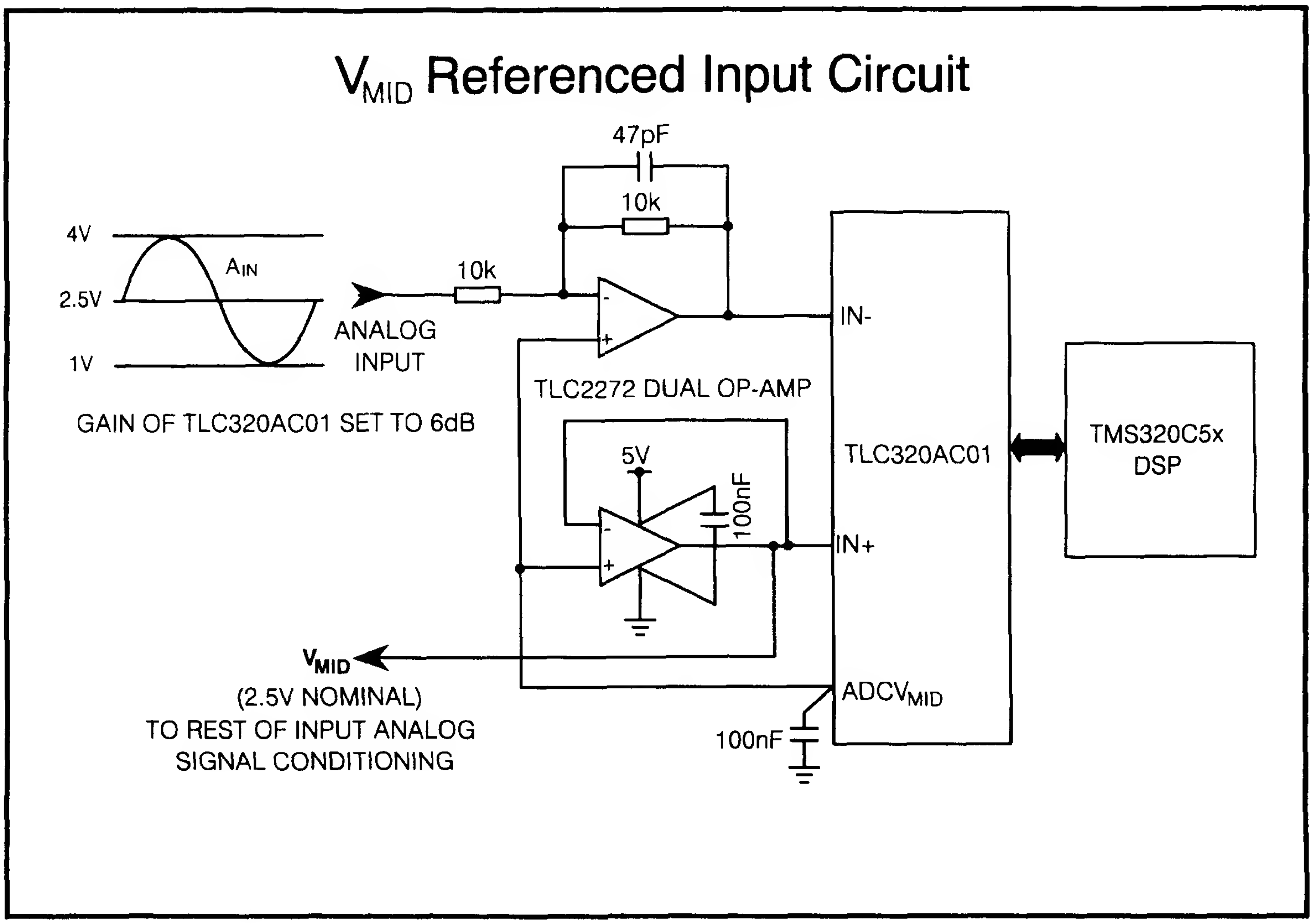

VMID Referenced Input Circuit
47pF
10k
4V
AIN
2.5V
1V
10k
ANALOG
INPUT
IN-
TLC2272 DUAL OP-AMP
GAIN OF TLC320AC01 SET TO 6dB
5V
100nF
TLC320AC01
TMS320C5x
DSP
IN+
VMID
(2.5V NOMINAL)
TO REST OF INPUT ANALOG
SIGNAL CONDITIONING
ADCVMID
100nF

Figure 3.32 - V_{mid} Referenced Input Circuit

V_{mid} Referenced Input Circuit Configuration

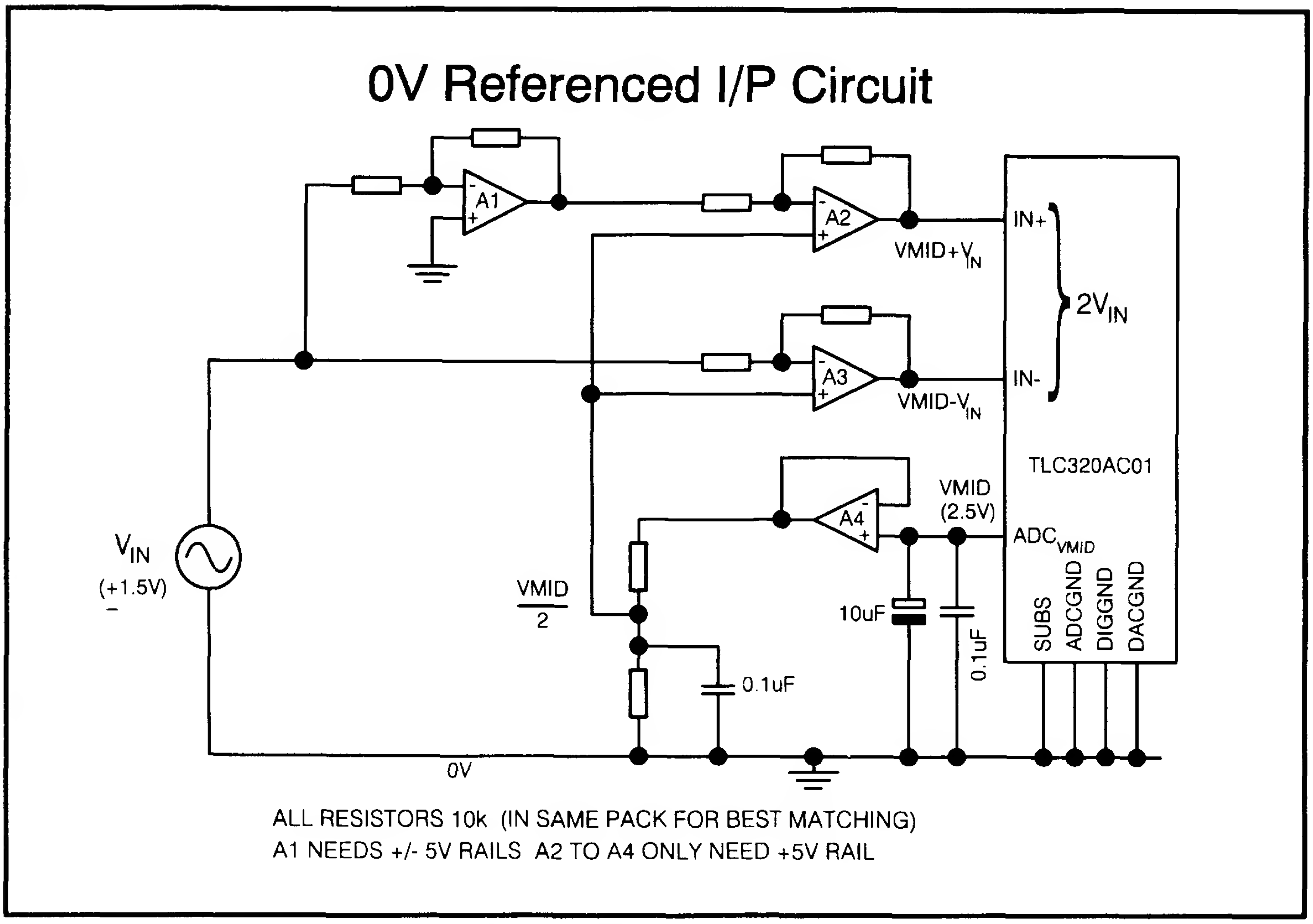
The configuration of the input circuitry requires extra care since all internal signals are referenced to V_{mid} rather than ground, to allow single supply operation. The PSRR at the internally generated V_{mid} point is low, so it is important that both the differential inputs are referenced to V_{mid} with any noise on V_{mid} appearing equally on both inputs.

There are two ways of fulfilling this criterion. The first is to reference the whole input circuit to V_{mid} (using this as a virtual ground) as shown in figure 3.32.

This configuration has the advantage of simplicity although there are some drawbacks. The buffered V_{mid} point has to be capable of driving the 'virtual ground' and since many op amps are unhappy driving large capacitive loads this problem must not be overlooked. The TLC2272 is a good choice for this application. The input needs to be referenced to V_{mid}, which may cause a problem if interfacing to an externally powered, ground referenced signal. In this case the input needs to be ac coupled.

0-V Referenced Input Circuit Configuration

The second method is to level shift the signal just before the ADC inputs as shown in figure 3.33 . In this circuit, the pre-amp input is referenced to 0 V. This circuit allows a full range input swing (V_{mid} ± 1.5 V on each input) for an input signal of ±1.5 V. Any noise on V_{mid} appears equally on both differential inputs and is therefore cancelled. The common mode range of the inputs does not exceed the supply rails, so V_{mid} noise must not take the input signal outside the supply rails. The eight resistors can conveniently be in one thin film resistor package, giving good matching of resistor values and hence good power supply rejection ratio (PSRR) and dc accuracy. Amplifier A1 must have ±5 V or greater power rails but A2 to A4 only need a single 5-V rail.



ALL RESISTORS 10k (IN SAME PACK FOR BEST MATCHING)
A1 NEEDS +/- 5V RAILS A2 TO A4 ONLY NEED +5V RAIL

Figure 3.33 - 0-V Referenced Input Circuit

Gain Control

The internal pre-amp of the TLC320AC01 has software selectable internal gain of 0 dB, 6 dB or 12 dB plus a squelch mode (-60 dB). With 0 dB gain, ± full scale result is given for a differential input of ±3 V. With a single ended input configuration (one input tied to V_{mid}), this would not allow ± full scale before the op amps run out of headroom, so the gain must be set to 6 dB or 12 dB which would give ± full scale with ±1.5 V and ±0.75 V respectively at the TLC320AC01 input.

Most of the input noise is associated with the converter itself, rather than the input amplifiers or multiplexers. Therefore, the signal-to-noise ratio is hardly affected by the chosen input gain. However, it is easier to ensure good rejection of power supply noise coupled through V_{mid} at low gains.

The TLC320AC01 has two sets of differential inputs, IN and AUXIN which can be individually selected (or both selected simultaneously for mixing).

If more gain settings are required, a combination of software switching of input source and input gain coupled with an extra hardware gain stage (see figure 3.34) allows six software selectable gain steps as shown in the table below.

External gain 3 dB		
NORM/AUX Input	Internal gain (dB)	Total gain (dB)
NORM	0	0
AUX	0	3
NORM	6	6
AUX	6	9
NORM	12	12
AUX	12	15

External gain 18 dB		
NORM/AUX Input	Internal gain (dB)	Total gain (dB)
NORM	0	0
NORM	6	6
NORM	12	12
AUX	0	18
AUX	6	24
AUX	12	30

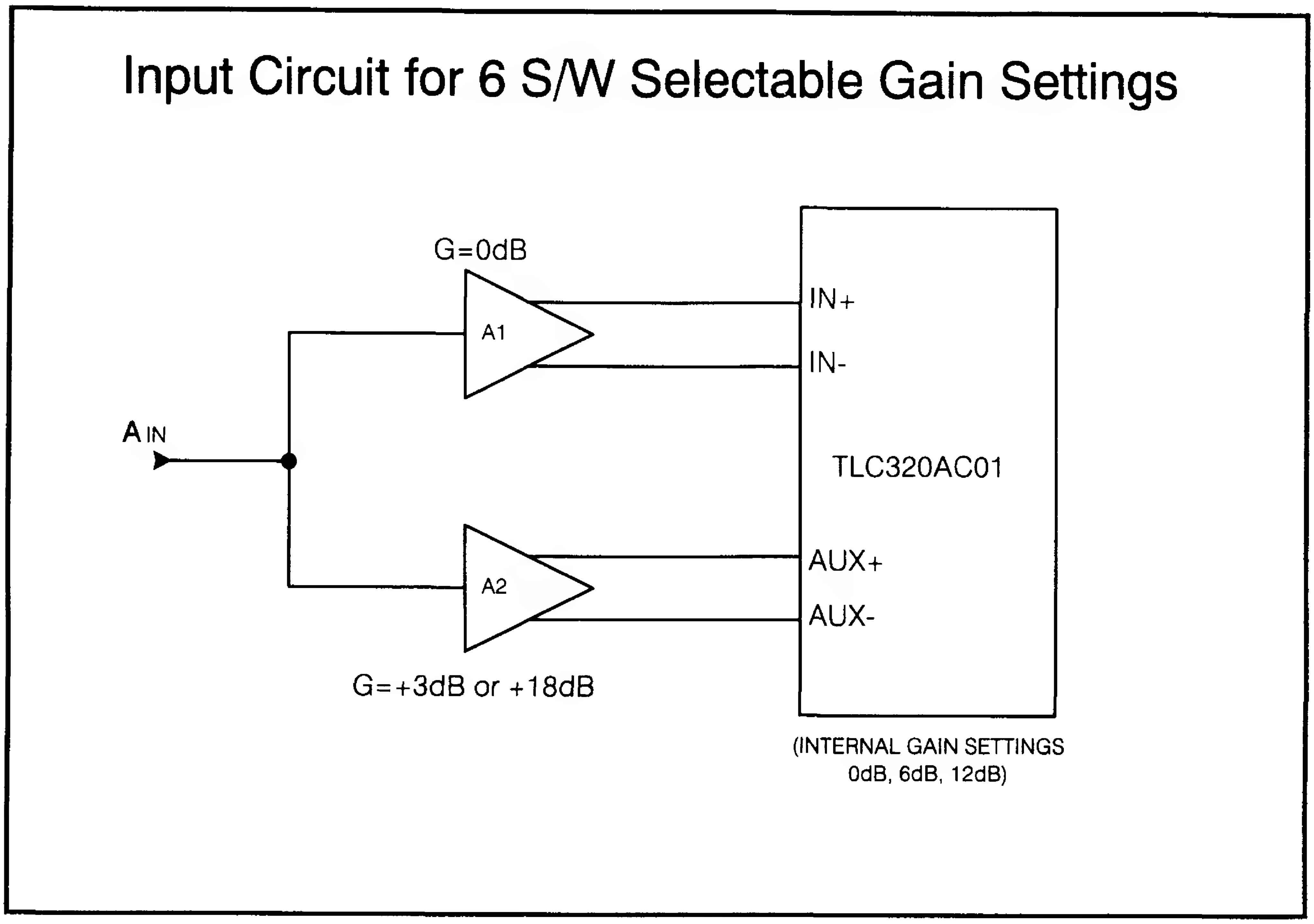


Figure 3.34 - Input Circuit for 6 S / W Selectable Gain Settings

4.2.3 Layout and Grounding

Although earthing and PCB layout do not seem to be too critical for this device, it is good practice to ensure that the ground current from sensitive devices such as the ADC does not flow in the same copper as currents from other devices. This means having a central ground point near the device or using power planes with splits where necessary to isolate return current from other devices.

The substrate (SUBS) should be connected to ADC ground. Failure to do so can result in noisy and unstable operation. The circuit should be well decoupled for low and high frequencies to minimise noise injection from the supplies.

4.2.4 Power supply

With a master clock frequency of 10 MHz, our TLC320AC01 samples typically drew about 10 mA at 5.0 V with default register values. The supply current depends principally on the filter clock frequency. If a negative supply is needed for op amps etc., it may be convenient to generate it using a negative voltage converter. Since the negative supply generally draws little current this is a feasible solution and avoids the need for a second battery in portable systems. The ICL7660 needs no external inductors and is available in an 8-pin small outline package. As the internal oscillator of the ICL7660 free runs at about 10 kHz, noise generated from this oscillator can find its way into the ADC input, often beating with the sampling clock creating a "whirring" type noise. It is however possible to lock this oscillator to the ADC clock by linking the conversion complete signal to the oscillator input on the ICL7660. Coupling via a 100-pF capacitor allows the converter to free-run if the ADC is not operative (e.g. during start-up). Any noise that now gets coupled into the ADC will be the same for each sample, creating a dc result that is much easier to deal with. Alternatively the TLE2682 provides a negative rail generator supplying up to 100 mA (which can be phase locked) plus a dual op amp in one 16-pin wide body SO package) .

4.2.5 Sampling Rate and Filters

Within limits, the sampling rate of the device (both ADC and DAC are inherently synchronous) can be set under software control. If the DAC is not used then the ADC can run at up to 43.2k samples/sec. However, if the DAC is to be used the sampling rate must be limited to 25k samples/sec.

The anti-aliasing filters (switched capacitor type) track the sampling rate by setting the corner frequency of the filter to some fraction of the sampling rate. This allows for the possibility of sub-Nyquist sampling, which should be avoided in most cases. The ratio of sampling rate to anti-aliasing filter corner frequency is set by the B register value ($\mathrm{Reg_B}$). The anti-aliasing corner frequency is set by the A register value ($\mathrm{Reg_A}$) within the TLC320AC01.

Conversion rate is given by:

$$f_{sample} = \frac{f_{MCLK}}{(2 * \mathrm{Re}\,g_A * \mathrm{Re}\,g_B)}$$

The anti-aliasing corner frequency is given by:

$$f_{lp} = \frac{f_{MCLK}}{80 * \mathrm{Re}\,g_A}$$

$$\frac{f_{sample}}{f_{lp}} = \frac{40}{\mathrm{Re}\,g_B}$$

To satisfy Nyquist's sampling theorem:

$$\frac{f_{sample}}{f_{lp}} \geq 2$$

$$\therefore \mathrm{Re}\,g_B \leq 20$$

The default of 18 for the B register gives $f_{sample}/f_{lp} = 2.2$. This ensures that energy above the Nyquist frequency is well into the filter's stop band.

The product of the A and B registers must be greater than 65 to allow for 17 serial clock cycles between conversions (16 data bits plus one extra cycle for frame sync in master or standalone mode). The B register must not be less than 10, since the ADC conversion takes 10 B register counts to complete. The A and B registers have a maximum value of 255.

High Pass Filter

The TLC320AC01 also has a high-pass filter which can be used to attenuate subsonic noise and remove dc offsets. The importance of subsonic noise filtering should not be underestimated. For example: Air conditioning systems are a notorious source of low frequency noise and a slamming door can produce extremely high levels of subsonic energy. The filter in the TLC320AC01 has a corner frequency of $f_S/200$ and a slope of 6 dB per octave. The corner frequency cannot be changed independently of the sampling frequency.

4.3 Analog output

As previously mentioned, the maximum sample rate for the DAC, at 25 kHz, is lower than for the ADC. This limits the bandwidth of the output signal to less than 12.5 kHz.

4.3.1 Signal-to-Noise and Signal-to Distortion Ratio

Figure 3.35 shows the result of intermodulation distortion measurements for the DAC made on the test boards. The noise floor can be seen at approximately -90 dB in the pass band, falling to approximately -108 dB at frequencies above $f_S/2$. There are some distortion products in the pass band at approximately -85 dB. The double peaks at approx. 7 and 9 kHz are images of the signal that have been only partially attenuated by the reconstruction filter. Images are the digital to analog equivalents of aliases in analog to digital conversion. They occur at frequencies given by:

$f_{image} = N f_S \pm f_{in}$ N = 1, 2, 3 ...

f_S = sampling frequency

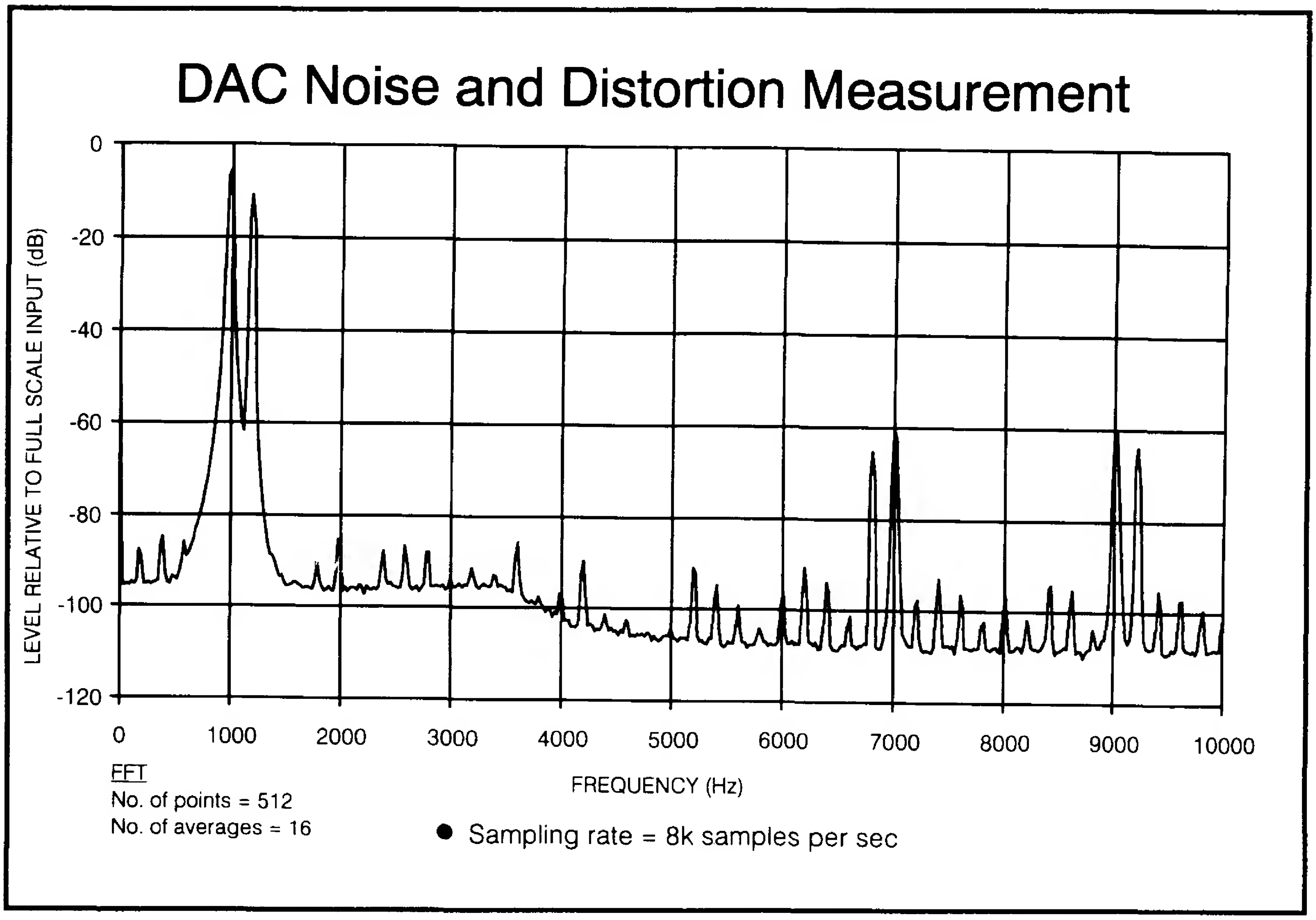


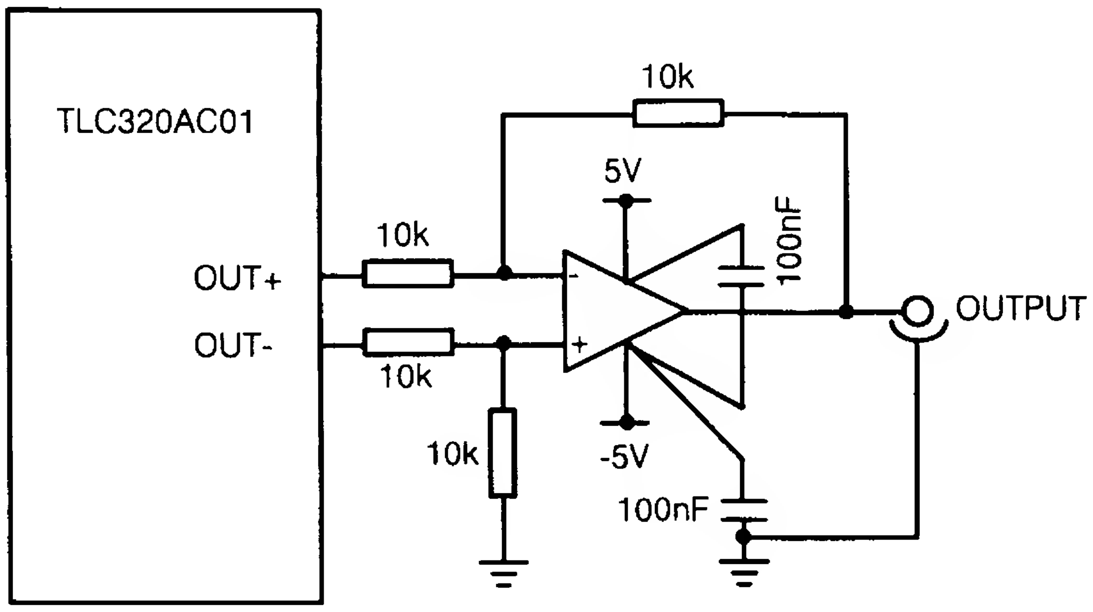
Figure 3.35 - DAC Noise and Distortion Measurements

If the images are too large for a given application they can be removed by continuous-time low-pass filtering at the output of the DAC. The size of the images reflects the 45 dB stop-band attenuation of the reconstruction filter.

4.3.2 Voltage Swing and PSRR

The voltage swing at the differential output is ±6 V for a full scale output. There are software selectable attenuators giving outputs of 0 dB, -6 dB, -12 dB and a squelch mode of -60 dB. Although there is not a large improvement in SNR ratio by using a differential output stage, it has the added advantage of increasing the PSRR and allowing level shifting to a ground referenced output without having to ac couple the signal. Using a thin film resistor pack for the differential amplifier gives the well matched resistors needed for good common mode rejection and accurate gain. Using a differential amplifier in this way the PSRR was improved from 49 dB to 52 dB. See figure 3.36

Differential to Single-ended Output Amplifier



- The TLE2061 op amp will drive +/- 3V into a 600 ohm load

Figure 3.36 - Differential to Single Ended Output Circuit

4.3.3 (Sinx)/x Correction

Sin(x)/x error arises because the output from a digital-to-analog converter is held constant between samples rather than smoothly joining them up. The TLC320AC01 has a sin(x)/x correction filter. It gives a correct response for a B register value of 15, which gives a ratio of sample rate to ADC anti-aliasing filter of 2.67. But as it does not track the B Register, other values for the B register will produce an error in the magnitude of a given output frequency. Figure 3.37 shows a graph of calculated error versus frequency for various values of B register with a master clock of 10 MHz and a sample rate of approximately 8 kHz. Other values can be calculated using the equation given in section 2.15.7 of the TLC320AC01 data manual.

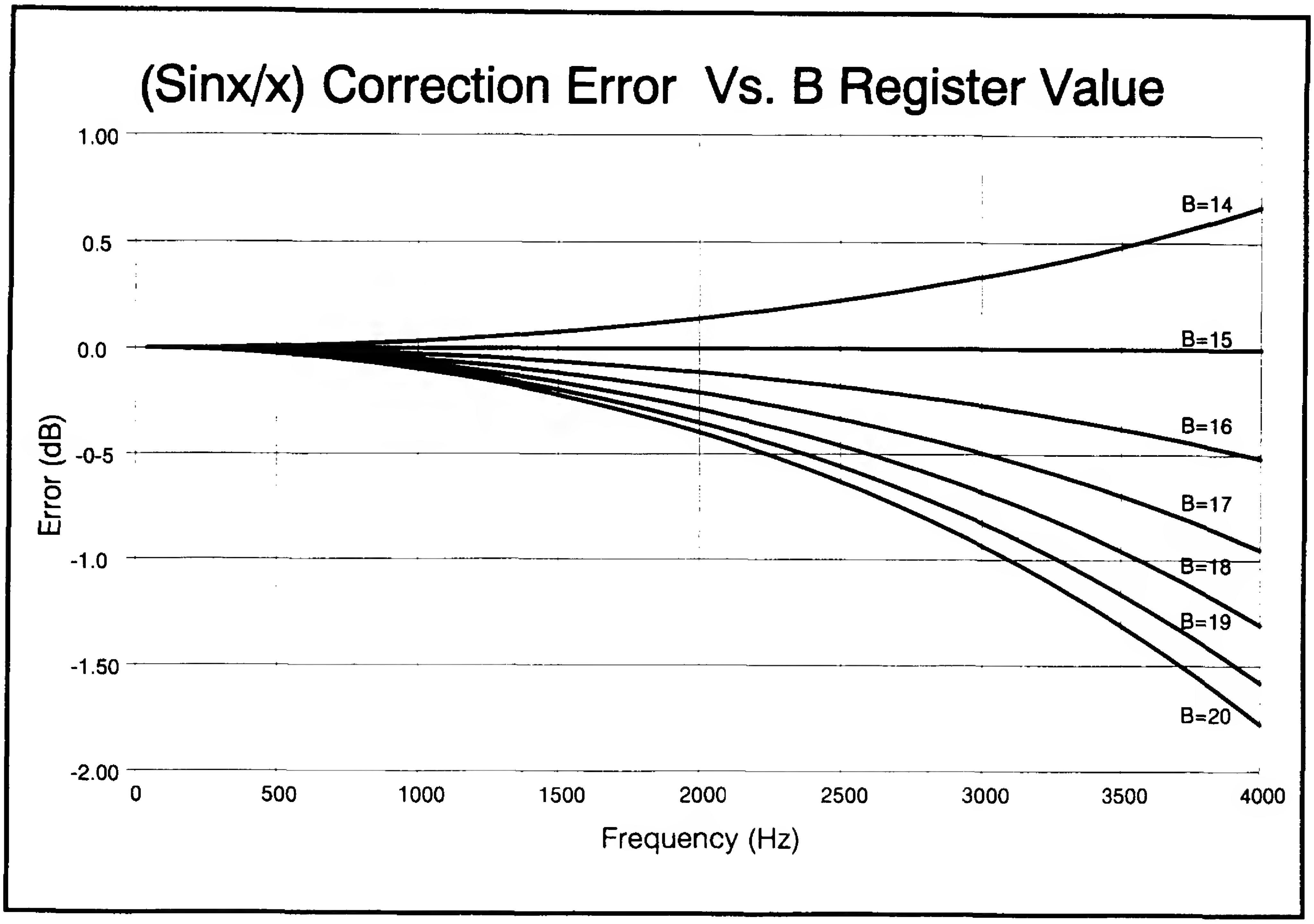


Figure 3.37 - (Sinx)/x Error

4.4 Digital Design Considerations

4.4.1 DSP Serial Interface

The TLC320AC01 can be connected directly to the synchronous serial port of a TMS320C25 as shown in figures 6-1 and 6-3 of the TLC320AC01 data manual. Interfacing to the TMS320C50 family requires some caution because the CLKOUT signal will usually exceed the maximum 15 MHz MCLK frequency of the TLC320AC01. So a divider is required. Most makes of DSP chip support the synchronous serial interface and should connect directly to the TLC320AC01.

Maximum clock rate

It is highly desirable that the DSP chip and TLC320AC01 are clocked from a common master oscillator. This ensures that the digital noise which is often coupled into the ADC and DAC of the TLC320AC01 in miniature systems is aliased to a stable frequency, preferably dc. We have found that the signal-to-noise ratio can be degraded by as much as 6 dB in a breadboard system when independent clocks are used compared with a fully synchronous system.

A very convenient way of phase locking the TLC320AC01 to the processor is to drive the MCLK input of the TLC320AC01 from the CLKOUT of a TMS320C25 or TMS320C50 or from the H1 or H3 output of a TMS320C30. However, because of the higher speed of the TMS320C50 an external one or two stage divider must be used to lower the CLKOUT frequency (which can be between 20 MHz and 40 MHz depending on which speed grade of processor is used) to 15 MHz or less. A '74ACT74 was chosen for its high maximum clock frequency, relatively low power consumption and availability in surface mount package. The divider power supply current was measured at 6.5 mA at 5 V and 3.17 mA at 3 V when dividing by 2 at 20 MHz; and 20.3 mA at 5 V and 9.6 mA at 3 V when dividing by 4 at 40 MHz.

Synchronisation of Negative Rail Generator

If switching power supplies are used in the system, for example to generate a negative supply rail, it is advantageous to phase lock the switching frequency to the sampling frequency. The EOC output from the TLC320AC01 is fairly close to a square wave for reasonable sampling frequencies and can be connected to the OSC pin of a ICL7660 negative supply generator through a small (100 pF) capacitor to force the normally free running oscillator. The small capacitor allows the ICL7660 to free run in the absence of an EOC signal. The ICL7660 divides this signal by two internally, so that power supply ripple is at exactly the Nyquist frequency and hence appears as a small dc offset rather than as an unstable whistle.

Edge timing

It is important to ensure that the rise and fall times of the serial clock signal between the codec and DSP chip are within specification, particularly if level shifting circuits are used for mixed 5 V and 3 V operation. Failure to do so can result in data or frame sync signals being sampled on the wrong clock edge, causing erratic errors. The maximum shift clock output rise and fall times for the TLC320AC01 in master mode are 18 ns, typically 13 ns. The maximum serial clock input rise and fall times for the TMS320C25 are 25 ns, and for the TMS320C30 and TMS320C50 are 8 ns. While it might seem from these specifications that the TLC320AC01 cannot satisfactorily drive the TMS320C30 or TMS320C50 without buffering, in our experience, these devices do work reliably together so long as very short connections are used.

4.4.2 Hardware Design of TMS320C50 Based DSP system

A relatively simple yet powerful DSP system can be built using a TMS320C50 family digital signal processor and a TLC320AC01 codec, as shown in figure 3.38. The circuit shown is a simplified version of one that we have used extensively. It can readily be expanded to include parallel input and output ports. The TMS320C50 has 10K words of on-chip RAM, allowing quite complex algorithms to be implemented without the need to use external RAM. Some means of program storage is needed. We used a pair of 8-bit wide 1-Mbit flash EPROMs (N28F001BX-B120 from Intel) which completely fill the program and data address spaces, allowing the use of very large data tables. They have the advantages of reasonably low power consumption, especially when idle, the ability to be reprogrammed in-circuit or in a standard programmer (if socketed) and have a hardware protected boot block. The boot block is an 8K byte segment starting at address zero which can be protected against erasure by opening a switch. This allows the EPROM programming algorithm to be safely stored within the EPROM itself, downloaded to on-chip memory and executed from there to reprogram the rest of the flash EPROM with data transmitted through one of the serial ports. This is very convenient when portable equipment is to be reprogrammed in the field, especially when surface mounted devices are permanently soldered into the circuit. The initial bootstrap code can either be loaded using a standard programmer before assembly, or afterwards using the XDS510 in-circuit emulator interface which is brought out to a 14-pin header. These flash EPROMs have an internal state machine to control the erasure and programming algorithms. This is very important, not only because it simplifies programming, but it ensures that the essential pre-charge step before erasure is applied to all locations. This cannot easily be done with earlier generations of flash memory because those addresses that overlap internal registers and memory cannot easily be accessed. 100 kΩ pull-up resistor packs were used on the data bus and serial port signals to minimise power consumption when the bus is in a high impedance condition, which is the normal condition when executing from on-chip RAM.

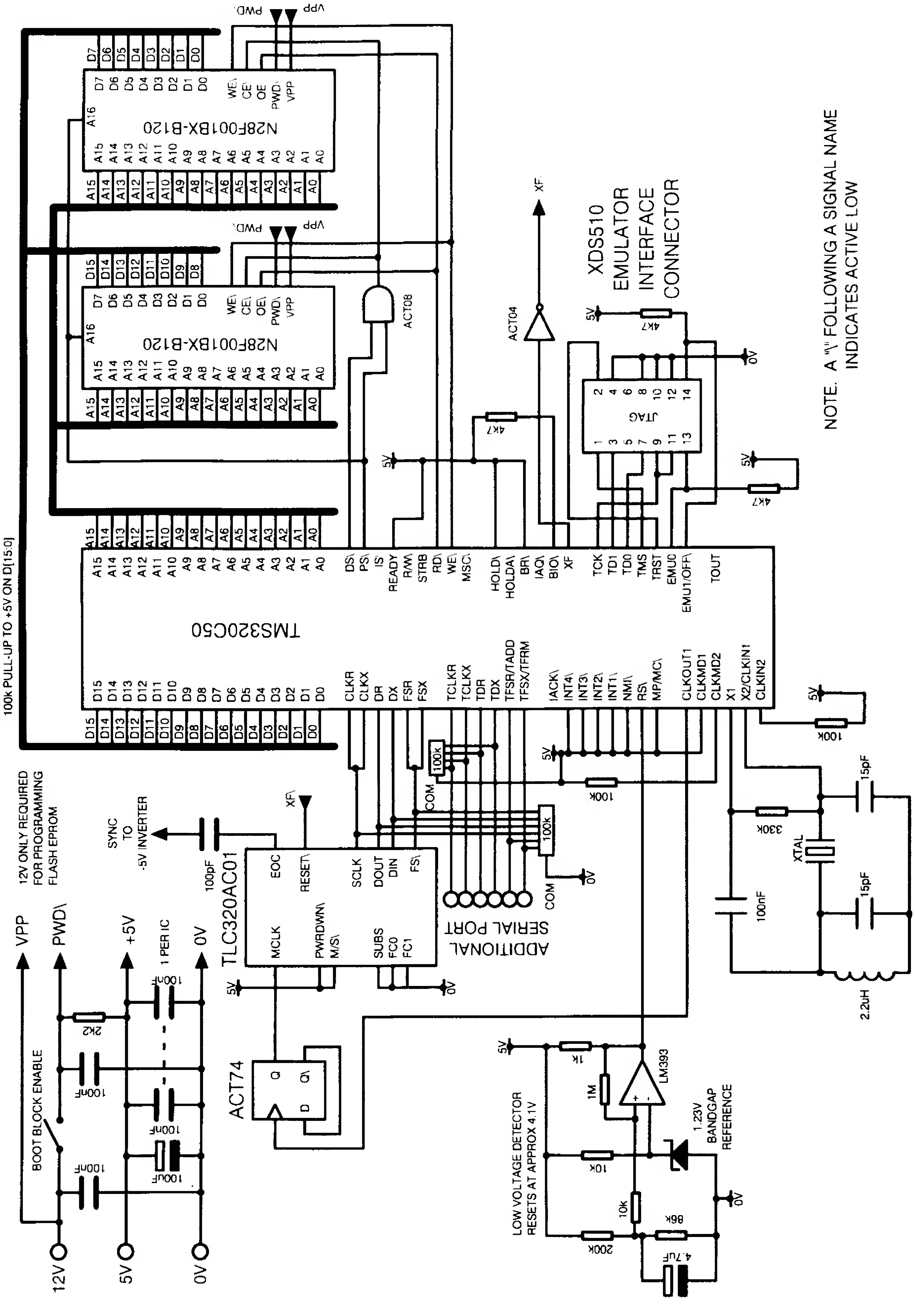

TMS320C50
N28F001BX-B120
N28F001BX-B120
TLC320AC01
ACT74
ACT08
ACT04
LM393
JTAG
XDS510 EMULATOR INTERFACE CONNECTOR
NOTE. A "\" FOLLOWING A SIGNAL NAME INDICATES ACTIVE LOW
100k PULL-UP TO +5V ON D[15:0]
12V ONLY REQUIRED FOR PROGRAMMING FLASH EPROM
SYNC TO -5V INVERTER
ADDITIONAL SERIAL PORT
LOW VOLTAGE DETECTOR RESETS AT APPROX 4.1V
1.23V BANDGAP REFERENCE
BOOT BLOCK ENABLE
1 PER IC
VPP
PWD\
+5V
0V
12V
5V
0V
XTAL
2.2uH
15pF
15pF
330K
100nF
100pF
100uF
4.7uF
200K
86K
10K
10k
1M
1k
2K2
4K7
100K
100k
COM
XF

Figure 3.38 - TLC320AC01 to TMS320C50 Hardware Schematic

A standard, 40 MHz, third overtone crystal oscillator was used to clock the TMS320C50. Exactly 8 kHz or 16 kHz sampling frequencies cannot be obtained with a 40 MHz *MCLK*. If this is a requirement, an *MCLK* of 41.472 MHz should be used. A 2.2 µH surface mount inductor blocks oscillation at the fundamental frequency of the crystal. The 330 kΩ resistor biases the on-chip oscillator inverter. Some care is needed in the choice of this value to ensure stable operation and reliable start-up. With the component values shown, the oscillator starts at a supply voltage of approximately 2 V and is stable up to the absolute maximum of 7 V. Alternatively, *CLKMD2* of the TMS320C50 can be grounded and an external 20 MHz clock fed into *CLKIN2*. This provides a divide by 1 option whereby the CPU clock operates at the same 20-MHz frequency. The 20 MHz, CLKOUT1 signal from the TMS320C50 is divided by two using half a 74ACT74 D-type flip-flop to provide a 10 MHz *MCLK* to the TLC320AC01.

The TMS320C50 needs a reset signal with a fast rise-time, so a comparator or Shmidt trigger must follow any resistor-capacitor reset delay circuit. At 20 MHz internal clock, the TMS320C50 requires 35 ns memory (including logic delays) for zero wait-state reads. It is therefore necessary, in the start-up software, to specify two extra wait-states of 50 ns each when accessing the 120 ns flash EPROM. (The TMS320C50 will automatically reset with 7 wait-states programmed for external access). The AND gate (which must have a delay of less than 15 ns) selects the EPROM when either the program or data memory spaces are to be accessed, and the $\overline{PS}$ drives the most significant address bit of the EPROM. In this way, program memory accesses select the lower 64K words of memory, and data memory accesses are mapped into the upper 64K words. This arrangement is very convenient, because code can be executed directly out of the EPROM when speed is not important. Very large data tables can speed up many algorithms and, because they are not usually accessed very often, the extra wait-states are not significant. Where there is a conflict between internal memory or other resources and the external flash EPROM, the internal access always takes priority.

Parallel input and output ports can readily be controlled by decoding the $\overline{IS}$ signal with $\overline{RD}$ or $\overline{WE}$ and, perhaps, some low address lines.

The power supplies should be generously decoupled with a combination of 0.1 µF ceramic capacitors placed close to each chip and one large tantalum electrolytic capacitor. Multi-layer printed circuit boards with ground and power planes dramatically reduce radiated noise and interference susceptibility. In our system, it was possible to place the antenna of an active PCN mobile telephone, transmitting a pulsed carrier at 1.8 GHz directly over the DSP chip without affecting its operation.

The TLC320AC01 is interfaced to one of the two serial ports of the TMS320C50. The reset input of the TLC320AC01 is connected to the external flag (*XF*) output of the TMS320C50 via an inverter and the *MCLK* is derived from *CLKOUT1* of the TMS320C50. The $M/\overline{S}$ control input is wired high to make the TLC320AC01 operate in master mode, and the *FC0* and *FC1* inputs are also held low because phase control is not used in this application.

4.4.3 Battery Operation

Reset considerations

The TLC320AC01 undergoes a power-on reset when V_{dd} falls below about 4 V with the samples we have tested. In battery powered systems it is important to ensure that the supply never dips this low, otherwise all the programmed registers will return to their default values. To guard against undetected resetting, the system supply should be monitored, using a comparator as shown in Figure 3.40 or a supply voltage supervisor such as the TL7702B. Also, one of the registers that has been changed from its default should periodically be read back and checked.

Interfacing to a 3-V DSP processor

There is a strong incentive to operate DSPs at 3 V or 3.3 V to save power. As the TLC320AC01 resets at a V_{dd} of about 4 V, separate power supplies and level shifting circuits must be used. The signals from a true CMOS DSP such as the TMS320C50 swing from 0 to V_{dd}, that is from 0 V to 3 V. As this is greater than the 2.2-V logic high threshold of the TLC320AC01, all signals from the DSP to the TLC320AC01 can be directly connected, provided that the 5-V supply rises and falls faster than the logic supply at switch on and off respectively. If the power sequence cannot be guaranteed, the TLC320AC01 inputs should be protected with a series resistor of about 3.3 kΩ compensated with a parallel capacitor of about 1 nF. There will be a small increase in I_{dd} of the TLC320AC01 compared with driving from 0 V to 5 V due to simultaneous conduction by both FETs in the input circuits. Signals from the TLC320AC01 to the DSP cannot be directly connected, however. The simplest interface circuit is a series resistor, to limit the current flowing through the upper protection diode, with parallel compensating capacitor to preserve the rise and fall times, as shown in figure 3.39.

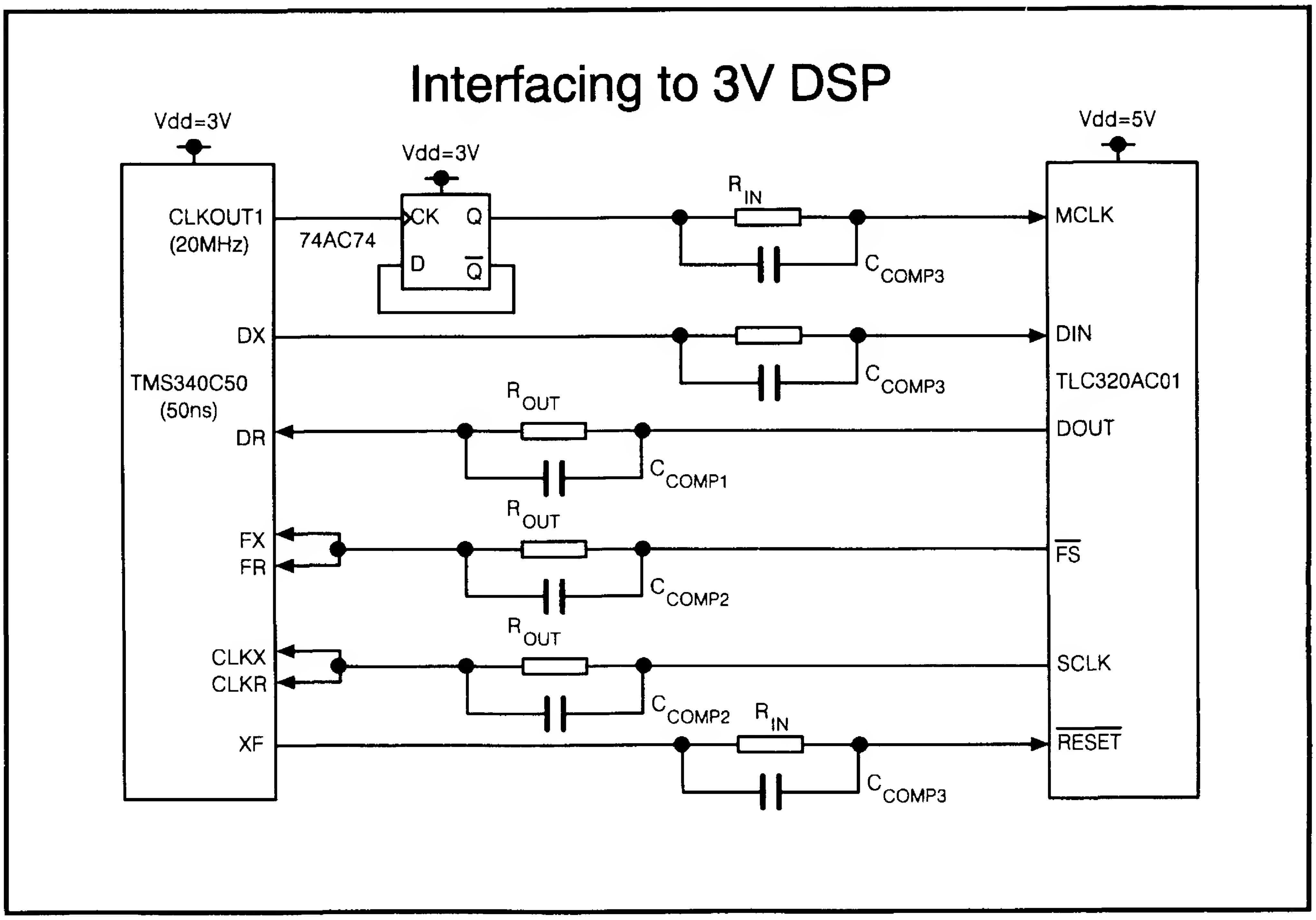

Interfacing to 3V DSP
Vdd=3V
Vdd=3V
Vdd=5V
CLKOUT1 (20MHz)
74AC74
CK
Q
D
Q̄
R_IN
MCLK
C_COMP3
DX
DIN
TMS340C50 (50ns)
C_COMP3
TLC320AC01
R_OUT
DR
DOUT
C_COMP1
R_OUT
FX
FR
FS
C_COMP2
R_OUT
CLKX
CLKR
SCLK
C_COMP2
R_IN
XF
RESET
C_COMP3

Figure 3.39 - Interfacing to 3-V DSP

Calculation of interface component values

Assuming that a transient input current through the protection diodes of 1 mA at power-up is safe for both devices and that the order of rise and fall is unknown. Then, 3.3 kΩ in series with the TLC320AC01 inputs (R_{in}) and 5.6 kΩ in series with the outputs (R_{out}) will provide full protection.

To calculate the appropriate compensation capacitor for signals from the TLC320AC01 to the TMS320C50, treat the parallel combination of C_{in} and C_{stray} in conjunction with C_{comp} as a capacitive divider where:

$$V_{OUT} = \frac{V_{IN}C_{COMP}}{C_{COMP} + C_{IN+STRAY}}$$

rearranging:

$$C_{COMP} = \frac{C_{IN+STRAY}V_{OUT}}{V_{IN} - V_{OUT}}$$

Substituting for worst case power supplies of 3.3 V and 4.5 V with one TMS320C50 input load of 15 pF and 10 pF stray capacitance:

For one input;

$$C_{COMP1} = \frac{(15+10)x3.3}{4.5-3.3} \approx 68pF$$

For two inputs:

$$C_{COMP2} = \frac{(15=15+10)x3.3}{4.5-3.3} \approx 120pF$$

These capacitor values should not be greatly increased because the input protection diodes of the TMS320C50 would then be driven into transient conduction on each rising logic edge.

The same method is applied to calculate the compensation capacitor for signals going to the TLC320AC01 (e.g. $\overline{RESET}$, *MCLK* and *DIN*). Assume a TLC320AC01 input capacitance of 5 pF and 10 pF stray capacitance, a worst case V_{dd} for the TMS320C50 of 2.7 V and TLC320AC01 input threshold of 2.2 V.

$$C_{comp3} = 68 \text{ pF}$$

This is a minimum value. C_{comp} should be as large as possible for lowest power consumption and best noise margin. The maximum value of C_{comp} depends upon the DSP chip power supply rise time. Switching three series connected 1.2 Ah NiCd cells with a total internal resistance of 30 mΩ into 200 µF of decoupling capacitance gives a maximum dV/dt of approximately 1 V/µs. In practice, wiring inductance and the resistance of protective fuses limit dV/dt to < 0.1 V/µs.

$$C_{IN}\big|_{MAX} = I_{IN}\big|_{MAX} * \frac{dV_{dd}}{dt}\Big|_{MAX}$$

Therefore, C_{in} should not greatly exceed 1 nF.

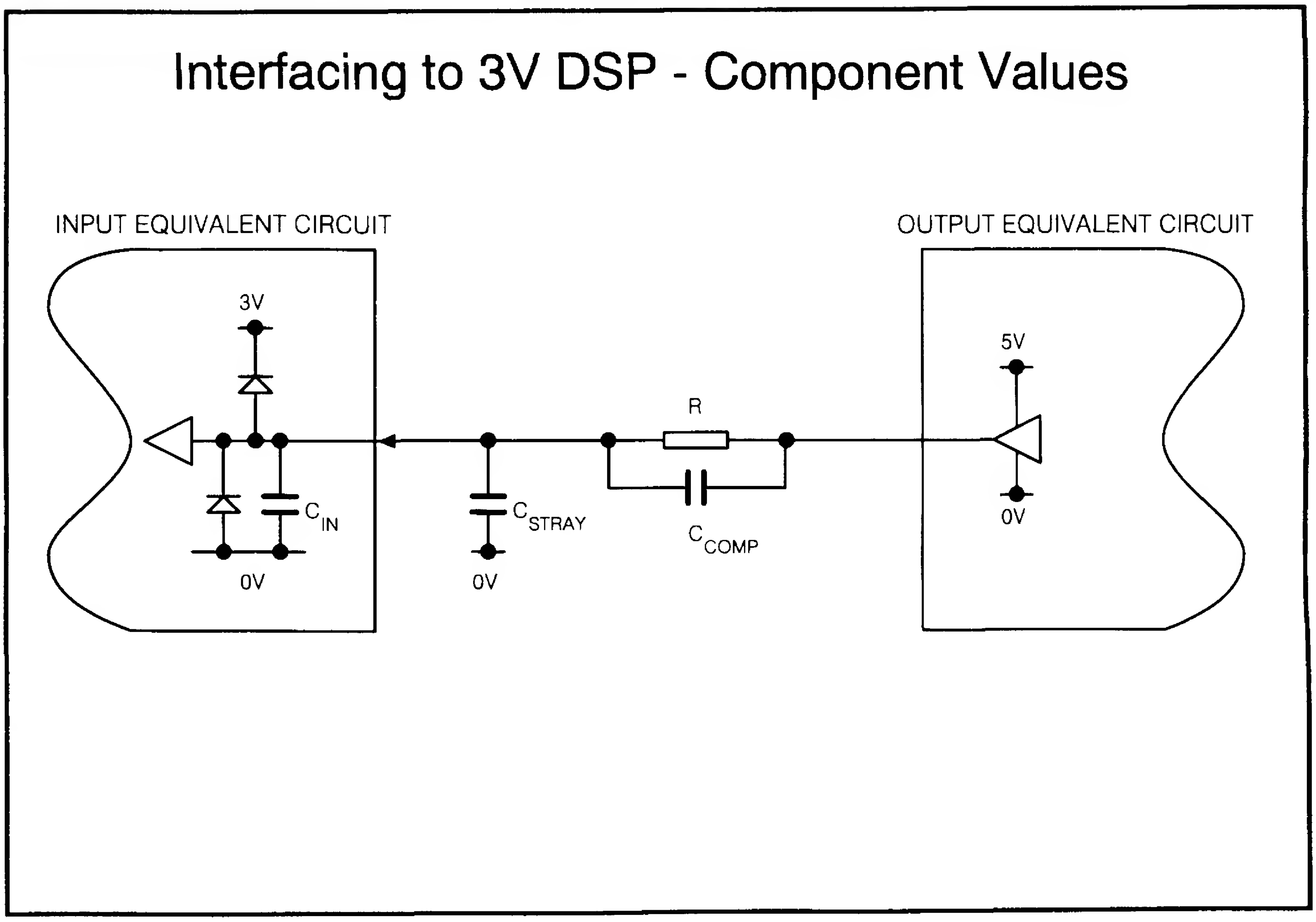

Interfacing to 3V DSP - Component Values
INPUT EQUIVALENT CIRCUIT
OUTPUT EQUIVALENT CIRCUIT
3V
5V
R
C_IN
C_STRAY
C_COMP
0V
0V
0V

Figure 3.40 - Interfacing to 3V DSP - Component Values

4.4.4 Programming

Many parameters, including the sampling frequency, low-pass filter cut-off frequency and input and output gains can be modified under software control. This can be done either just after resetting the TLC320AC01 or at any later time. For those applications where the default values are satisfactory the TLC320AC01 can be used without any initialisation. If any parameters need to be changed, it is best to do so immediately after a reset to avoid generation of clicks. For this reason it is convenient to control the reset input to the TLC320AC01 from an output bit of the DSP chip rather than the system reset signal. For TMS320C25 or TMS320C50 devices this can conveniently be the external flag (*XF*) output signal. If *XF* is directly connected to the TLC320AC01 without an inverter, it should be reset to zero immediately after the DSP comes out of reset, as it defaults high. *XF* is set to start the TLC320AC01 when all other initialisation is complete and serial port interrupts can be serviced. If possible, the *XF* output should be inverted with a spare gate. Then the TLC320AC01 will remain reset until *XF* is cleared to 0 with a CLRC XF or RXF instruction.

Initialisation

Only those registers that have to be changed from their defaults need to be reprogrammed. The initialisation process consists of sending pairs of data values from the 16-bit synchronous serial interface of the DSP chip to the TLC320AC01. In most cases the first word of the pair will be 0000 0000 0000 0011B. The 14 most significant bits of this value (bits 15 to 2) specify that an output sample of zero be sent and the two least significant bits (bits 1 and 0) specify that the next word transmitted will be interpreted as a secondary communication.

The secondary data value is used to reprogram one of the nine registers. Bits 15 and 14, which control phase shifting in modem applications will usually be zero, bit 13 = 0 specifies that data is to be written to a register, bits 12 to 8 define the address of the register that is to be changed. Bits 7 to 0 contain the data to be stored in the register.

4.4.5 Register descriptions

Pseudo Register 0 (no-op)

The main purpose of R0 is to allow phase shift commands to be sent as secondary communications without reprogramming any other register. It is not needed for most applications.

Register 1 (A register)

The A register sets half the number by which the master clock input (MCLK) is divided to provide the switched capacitor filter clock (FCLK). This is also the principal method for setting the sampling frequency.

Register 2 (B register)

The B register sets the ratio between the low-pass filter corner frequency and the sampling frequency. For most purposes the default, or a value close to it will be appropriate.

Register 3 (A' register)

The A' register is used for phase shift control and can be ignored for most purposes.

Register 4 (Amplifier gain select register)

This allows the gains of the analog input and output to be varied by -6 dB or -12 dB or disabled. The monitor output can be varied by -8 dB or -18 dB or disabled.

Register 5 (Analog configuration register)

This selects whether the high-pass filter is to be disabled, thus allowing the codec to respond to dc, and controls the input multiplexer.

Register 6 (Digital configuration register)

Controls operating modes and power-down options. The defaults will be suitable for many applications.

Register 7 (Frame-sync delay register)

This controls the timing of the serial data transmission of a slave converter in multi-channel multiplexed systems.

Register 8 (Frame-sync number register)

This controls the number of frame-sync pulses generated, corresponding to the number of channels being multiplexed on to the bussed serial interface. The default of 1 is suitable for single channel operation.

4.4.6 TLC320AC01 / TMS320C50 Demonstration Program

The demonstration program AC01DEMO.ASM carries out the simplest possible operation - reading in a sample from the ADC in the TLC320AC01 and then writing it to the DAC. It is assembled and linked using the commands in the batch file MAKE.BAT. This is called as follows: "MAKE AC01DEMO".

The program begins with the definition of some variables and allocation of their memory locations. The COFF assembler used here does not assign absolute addresses, but instead relative positions within named blocks of memory. The linker then resolves these references in conjunction with information stored in the linker command file AC01DEMO.CMD.

The next section of the program is the definition of macros that will be used later. Using macros makes the main program listing easier to understand by hiding some of the frequently repeated details.

The section called "vectors" is loaded into flash EPROM at address zero, which is where the TMS320C50 starts executing after reset. The ".text" section is the main body of the program, and would typically be loaded into the memory section "flashp" defined in the command file. In this example, however, it has been placed immediately after the "vectors" section in the protected bootstrap area for convenience of testing.

The main program starts by initialising certain processor registers that are undefined or have unsuitable defaults at start-up, then clearing the memory variables. The code which is to run in real-time is copied from flash EPROM to the on-chip single-access RAM block for maximum speed of execution. The serial port is initialised to use external clock and frame synchronisation pulses, and to transfer 16-bit data words. The initial behaviour of the serial port is unpredictable when it is reset with the frame sync input high, as is the case when the TLC320AC01 is inactive. Therefore, a dummy value of zero is sent, and afterwards the TLC320AC01 is again reset briefly. Now the interface is properly initialised, the program branches to the real-time processing loop.

The processor waits in a low power idle mode until an interrupt is received. It then wakes up and determines whether the interrupt was from the serial port, in which case it executes the processing loop. The processed results from the previous sample are written to the serial port data transmit register, then the fresh ADC data is read in from the data receive register and processed. The results are stored ready to be sent to the DAC on the next interrupt. This double buffering method maximises the processing time available because processing can take place while serial data is being transmitted and received. The two least significant bits of the output data are masked out to ensure that a secondary communication request is not inadvertently sent.

The serial port receive interrupt routine simply sets a flag to indicate that data is available. There is no need to have a separate transmit interrupt because the transmit and receive operations are inherently synchronous with each other.

List 8 - TMS320C50 Assembler Listing

```
        .title "'AC01 demonstration program"
        .width 200
        .version 50     ; Makes assembler generate C50 code
        .mmregs         ; Predefine names for memory mapped registers

; This program initialises the 'C50 processor and serial port,
; then initialises the 'AC01 codec and starts the main signal
; processing loop.  In this example, a data sample is read from the
; adc and written back to the dac unchanged.

; Using rev 6.40 or higher assembler tools, use the following make file

; @echo off
; if "%1" == "" goto :nofile
; dspa %1.asm -x -w -s -v50 -l
; if not errorlevel 1 dsplnk %1.obj -o %1.out -m %1.map %1.cmd
; goto :done
; :nofile
; echo no source file!
; :done
;   -s option makes all symbols global, and thus accessible to the
;      emulator and simulator.
;   -w option warns about pipeline conflicts.
;   -x option makes a cross reference table.
;   -l option generates listing file

; If an eprom programmer is used it may also be necessary to use the
; DSPHEX conversion program to split the linker output file which is in
; COFF format into a pair of high and low byte files in HEX format.

FSAMP     .set 16        ; 8 selects 8 kHz, 16 selects 16 kHz

; The following 2 variables must be in memory block b2 and dp set to 0
; because they are accessed by direct addressing

gotdataflag     .usect  "b2", 1 ; used to signal that an interrupt came
                       ; from the serial input port
outputbuffer    .usect  "b2", 1 ; temporarily store output sample

; Macro definitions

waitint .macro
waitint?
      lacc   gotdataflag
      bz     waitint?          ; wait for semaphore to be changed
      splk   #0, gotdataflag   ; set it again
      .endm

progreg .macro progval
      splk    #11b, dxr        ; request secondary comms
      waitint                  ; wait for transmission
      splk    #:progval:, dxr  ; send value
      waitint                  ; wait ....
      .endm

      .sect "vectors"     ; vectors is the starting point of a block of
                          ; program memory starting at address zero

; Interrupt vectors - these start at address zero
; unused interrupts branch to themselves so that if they are inadvertently
; activated they can be identified using the xds510 emulator
rs      b       mainentry
int1    b       int1
int2    b       int2
int3    b       int3
tint    b       tint
rint    b       getdata
xint    b       xint
trnt    b       trnt
txnt    b       txnt
int4    b       int4
rsvd14  b       rsvd14
rsvd16  b       rsvd16
rsvd18  b       rsvd18
rsvd1A  b       rsvd1A
rsvd1C  b       rsvd1C
rsvd1E  b       rsvd1E
rsvd20  b       rsvd20
trap    b       trap
nmi     b       nmi
rsvd26  b       rsvd26
rsvd28  b       rsvd28

      .text       ; .text indicates start of main program storage
                  ; block in flash eprom

mainentry               ; This is the startup entry point
      ldp     #0      ; data page pointer to page zero
      setc    INTM    ; globally disable interrupts
      setc    SXM     ; set sign extension mode
      setc    OVM     ; set saturation on arithmetic overflow
```

```
; Disable address visibility (to save power by not driving address bus)
; set up on-chip single access ram and B0 to be in data space
; for initialisation.
    splk    #0000000010101000b, PMST
    clrc    CNF     ; B0 is in data space

; Set up wait state control registers for 2 wait states
; when accessing flash eprom
    splk    #00000b, CWSR
    splk    #1010101010101010b, PDWSR

    splk    #0, gotdataflag         ; zero data received flag
    splk    #0, outputbuffer        ; zero output storage buffer

; relocate speed critical part of program to on chip ram
    lrlk    AR1, 800h       ; address in data memory of start of ram block
    larp    AR1
    lacc    #ocramstart     ; address in flash memory of start of code
    rpt     #ocramend-ocramstart-1
    tblr    *+

    apl    #1111111111011111b, PMST ; remove ram from data space
    opl    #0000000000010000b, PMST ; put it in program space

; set all interrupt masks except serial receive
    splk    #000010000b, IMR

; set up serial port
    splk    #0, dxr         ; zero the data transmit register
    splk    #0001000b, SPC  ; use ext clock & frame sync
    opl     #0c0h, SPC      ; take it out of reset

; clear all interrupt flag bits
    splk    #0ffffh, IFR
    clrc    intm            ; enable interrupts

    clrc    xf      ; release codec from reset
    waitint         ; wait for interrupt from serial port

; this code assumes that XF is inverted in hardware
; reset the codec and release it again to make it ignore first garbage word
; generated by serial port in revision 1 'C50 silicon
    setc    xf
    rpt     #10     ; hold 'AC01 reset low for at least 1 MCLK period
    nop             ; ie > 100ns for MCLK = 10MHz
    clrc    xf

; serial interface and 'AC01 are now in a stable state

; setup codec - only need to reprogram those registers that need
;              to be changed from their defaults
                                        ; reg 0 = no op

                                        ; reg 1 = A register (18=default)

    .if FSAMP = 8
     progreg 0000000101000101b          ; 36->8kHz @10.368 MHz clockin
    .endif                              ; 35->7.937kHz @10.0 MHz

    .if FSAMP = 16
     progreg 0000000100100010b          ; 18->16kHz @10.368 MHz clockin
    .endif                              ; 17->16.34kHz @ 10.0 MHz

     progreg 0000001000010010b          ; reg 2 = B register (18=default)
;            ||||||||||||||||
;            ||||||||++++++++---- data
;            |||+++++------------ address
;            ||+----------------- 0 = write
;            ++------------------ Phase shift

                                        ; reg 3 = A' register
```

```
        progreg 0000010000011001b       ; reg 4 = amplifier gain select
;               ||||||||||||||||
;               ||||||||||||||++---- output  0=sq, 1=0dB, 2=-6dB, 3=-12dB
;               ||||||||||||++------ input   0=sq, 1=0dB, 2=+6dB, 3=+12dB
;               ||||||||||++-------- monitor 0=sq, 1=0dB, 2=-8dB, 3=-18dB
;               ||||||||++---------- not used
;               |||+++++------------ address
;               ||+----------------- 0 = write
;               ++------------------ Phase shift

        progreg 0000010100000101b       ; reg 5 = analog configuration
;               ||||||||||||||++---- 0=loopback,1=norm i/p,2=aux i/p,3=both
;               |||||||||||||+------ 0=hp filter on, 1=hp filter off
;               ||||||||||||+------- 0=echo off, 1=echo on
;               ||||||||++++-------- not used
;               |||+++++------------ address
;               ||+----------------- 0=write
;               ++------------------ phase shift

                                       ; reg 6 = digital configuration
                                       ; reg 7 = frame sync delay
                                       ; reg 8 = frame sync number

      b       passthrough     ; branch to real-time code in on-chip ram

; This section is relocated to on-chip single access ram block
; for faster operation

      .sect "ocram"
      .label ocramstart ; this label refers to the address where the
                        ; following code is stored in eprom, not the
                        ; address from which it is executed

passthrough             ; this label refers to the execution address
                        ; in on-chip ram

; Main signal processing loop

      clrc    intm            ; Wait for any interrupt, determine whether
      nop                     ; it is caused by serial data input and branch
      idle                    ; back to idle if not.
      setc    intm            ; WARNING - The manipulation of INTM and the
      lacc    gotdataflag     ; nop, idle sequence are necessary to prevent
      bz      passthrough     ; serial interrupts from being missed if they
      clrc    intm            ; occur just after another interrupt!

      splk    #0, gotdataflag ; clear the data received flag

      out     outputbuffer, dxr     ; write the data derived from the
                                    ; previous input sample to the serial
                                    ; port data transmit register


      lacc    drr ; read a codec input sample from the serial port
                  ; data receive register. Data is in low accumulator


      ; do the signal processing here, leaving result in accumulator
      ; ...
      ; ...
      ; ...

      and     #1111111111111100b    ; mask out bottom two bits to ensure
                                    ; that secondary communications are
                                    ; not accidentally requested

      sacl outputbuffer           ; save the result of the processing until
                        ;the next interrupt, and only then write it
                        ; to the serial port.  This maximises the
                        ; processing time available.

      b       passthrough
```

```
; Interrupt handlers
; Because the transmit and receive operations of the 'AC01 are synchronous
; only one serial port interrupt handler is needed

getdata  splk    #1, gotdataflag  ; set a flag to indicate data available
      rete        ; return from interrupt, restoring context
                  ; and re-enabling interrupts

      .label ocramend ; end of block transferred to on-chip ram
   .end
```

List 9 - Linker command file: AC01DEMO.CMD

```
MEMORY   /* memory map for C50 */
{
page 0 : /* program memory */
   reset : origin = 0,      length = 800h  /* boot block up to start of on chip ram */
 onchipp : origin =  800h, length = 2400h /* on chip program memory */

flashp : origin = 8000h,  length = 7e00h /* top half flash prog except b0 */
param2 : origin = 3000h, length = 1000h  /* second parameter block in eprom */
                                   /* first par. block is overlaid by on-chip ram */

page 1 : /* data memory */
     b2   : origin = 60h,    length = 20h
     b0b1 : origin = 100h, length = 400h  /* combined blocks 0 and 1 */
onchipd : origin = 800h,  length = 2400h  /* ocram is on-chip data if OVLY=1 */
                                    /* external flash eprom if OVLY=0  */
}

SECTIONS
{        vectors : load = reset  page 0
       .text    : load = flashp page 0
       param2   : load = param2 page 0
       ocram    : load = flashp page 0 run = onchipp page 0

       b2       : load = b2     page 1 /* data page 0 on-chip ram */
       .bss     : load = b0b1   page 1
}
```

4.4.7 Measuring the DAC Filter Response with a White Noise Generator

A convenient way of measuring the frequency response of a linear system is to excite it with white noise and measure the response with a spectrum analyser. This example shows how white noise can be generated by a very short random bit generator program and used to measure the response of the TLC320AC01AC01's DAC reconstruction filter.

The random bit generator implements a recurrence relation in a primitive polynomial modulo 2 of order 31 (Reference 1). This gives a maximal length sequence of pseudo-random bits which only repeats after 2^{31}- 1 iterations. The polynomial used is $x^{31}+x^3+x^0$, although there are many others to choose from. A 32 bit variable "noise_sr", which is initially seeded with any non zero value, stores the state between iterations. On each iteration, the accumulator is loaded from "noise_sr" and shifted left one bit. The most significant bit (now in the carry bit) is then exclusive ORed with the remaining non zero terms. Each bit that has been XORed is stored back into the same location in the accumulator and the result is saved. This is implemented by testing the carry bit after the shift with the XC (execute conditional) instruction. If C was 0, do nothing because anything XORed with 0 is 0 and bit zero of the accumulator is filled with 0 after a shift. If C was 1, XOR the low accumulator with the constant 10010b which achieves the desired result.

There are three main limitations to this technique. Because the XOR is only carried out on the 16 least significant bits there must not be any non zero terms in the polynomial above x15 apart from x31. The contents of the accumulator should not be used directly as a random number because successive values are correlated as the bits work their way to the left. This is overcome in the example by iterating the code 14 times for each sample. Although the noise has a white long-term spectrum (that is equal power per unit frequency) it is non gaussian. This does not matter for frequency response measurements.

Figure 3.41 shows the response of the TLC320AC01 reconstruction filter measured at a sampling rate of 7.937 kHz. The A register value was 42, the B register value was 15 and the MCLK frequency was 10MHz.

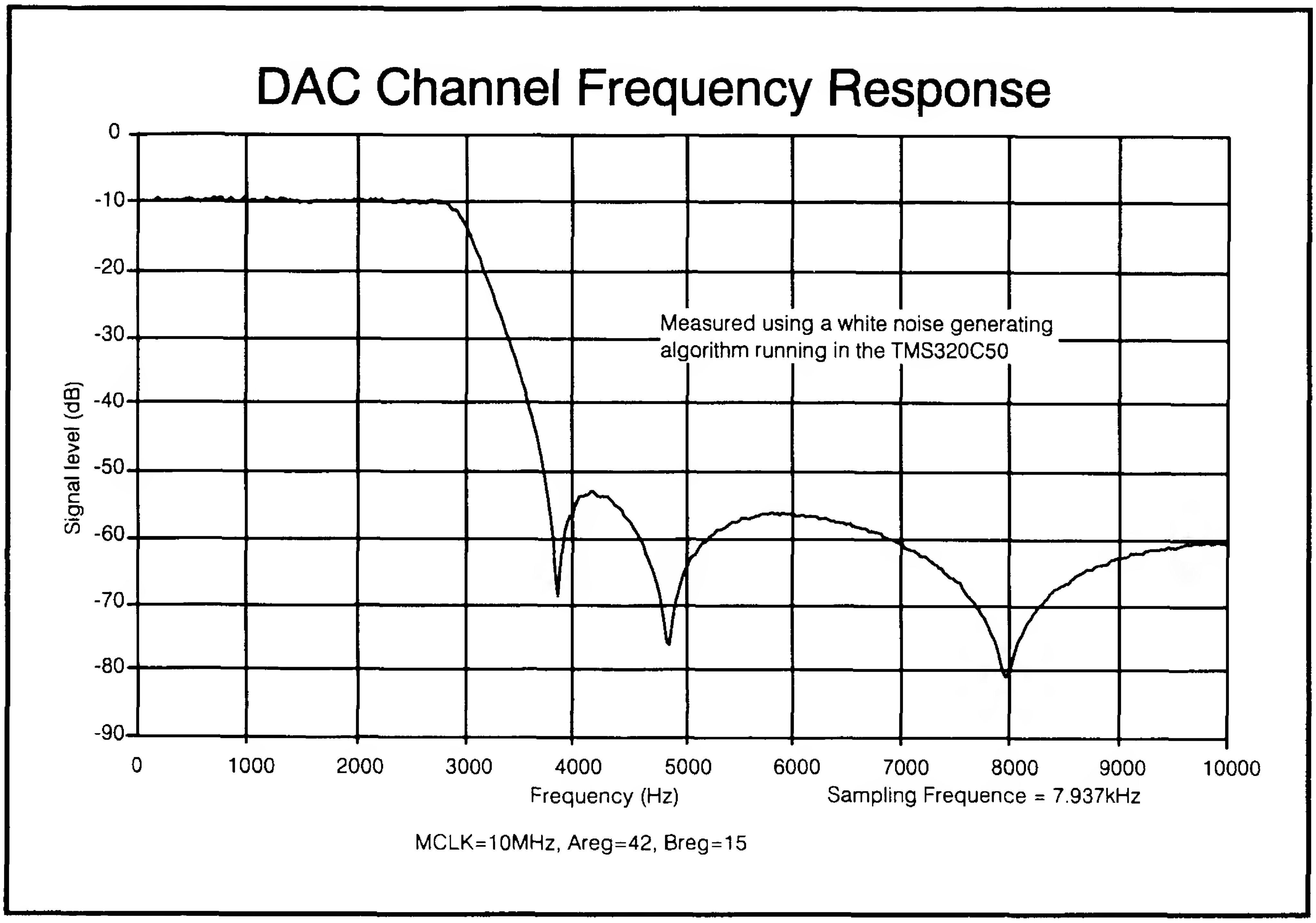


Figure 3.41 - DAC Channel Frequency Response

List 10 - Example Noise Generator Code

```
noise_sr    .usect "b2", 2    ; allocate 32 bits of data memory

; ...

       larp    AR1      ; seed random bit generator with 2
       lrlk    AR1, noise_sr
       lac     #2
       sacl    *+
       zac
       sacl    *

; ...

; execute this section once per dac output sample
       larp    AR1
```

```
      lrlk    AR1, noise_sr
      lacl    *+             ; load low accumulator from data memory
      add     *, 16          ; load high accumulator
      splk    #13, brcr      ; repeat block 14 times to decorrelate
                       ; sequential bits
        rptb    end_noise - 1
        sfl                  ; need a 1 cycle gap between sfl and xc to
        nop                  ; allow for pipeline delay
        xc      1, C         ; execute next instruction if carry set
        xor     #10010b       ; xor bit 3 with bit 31, copy bit 31 to bit 0
end_noise

        sach  *-             ; save high accumulator to data memory
        sacl  *              ; save low accumulator

; Write low accumulator to transmit data register
; (after masking out bottom 2 bits)
```

4.4.8 Sampling and Quantisation - Tutorial

Nyquist - Ideal Sampling

In converting a continuous time signal into a discrete digital representation, the process of sampling is a fundamental requirement. In an ideal case, the sampling signal is a train of impulses (infinitessimally narrow with unit area). The frequency of these impulses is the sampling rate (f_s). The input signal can also be idealised, by considering it to be truly band limited, containing no components in its spectrum above a certain frequency.

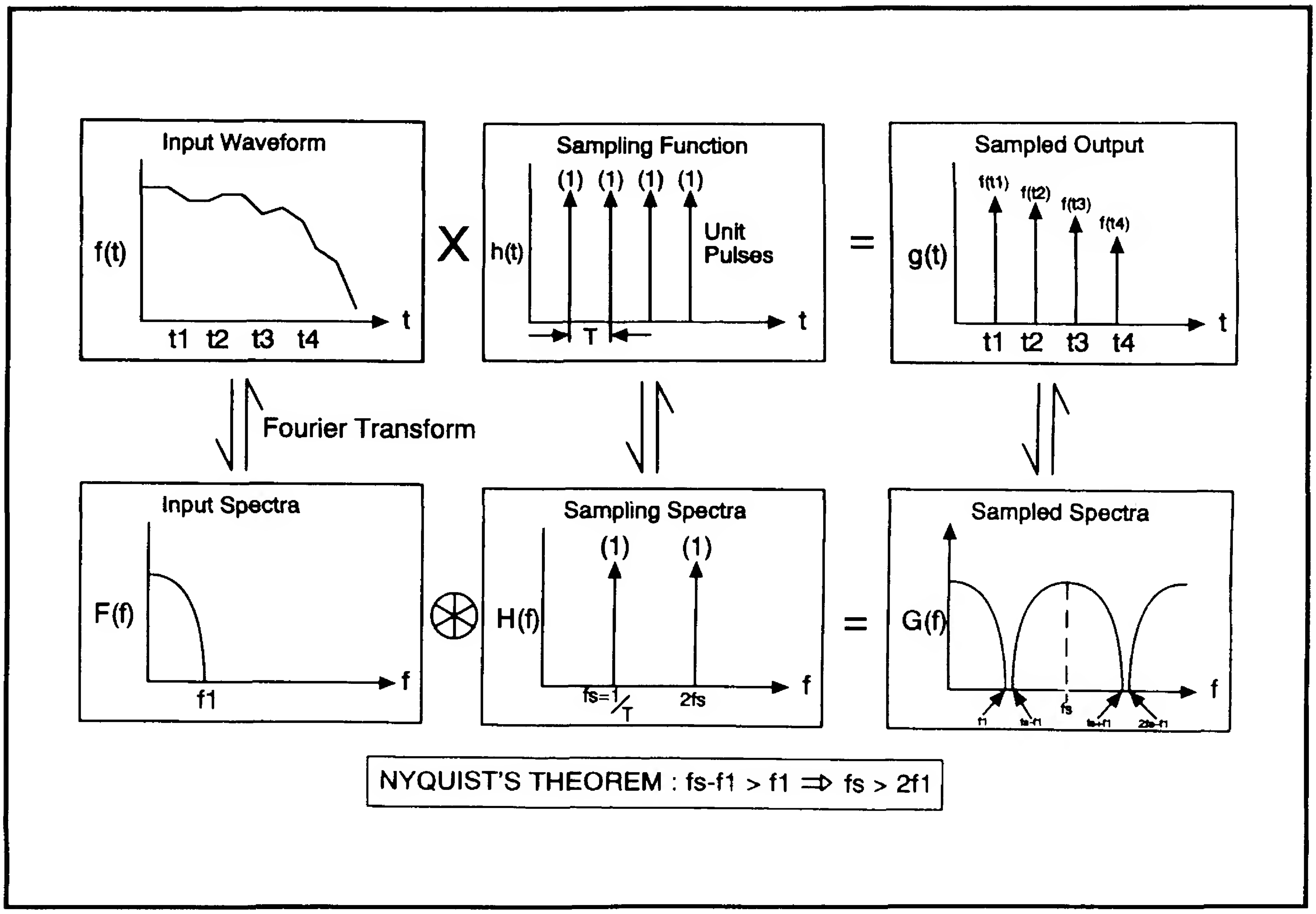

Input Waveform
f(t)
t1 t2 t3 t4
t
X
Sampling Function
h(t)
(1) (1) (1) (1)
Unit Pulses
T
t
=
Sampled Output
g(t)
f(t1) f(t2) f(t3) f(t4)
t1 t2 t3 t4
t
Fourier Transform
Input Spectra
F(f)
f1
f
Sampling Spectra
H(f)
(1) (1)
fs=1/T
2fs
f
=
Sampled Spectra
G(f)
f1
fs-f1
fs
fs+f1
2fs-f1
f
NYQUIST'S THEOREM : fs-f1 > f1 ⇒ fs > 2f1

Figure 3.42 - Ideal sampling

The ideal sampling condition is shown in figure 3.42, represented in both the frequency and time domains. The effect of sampling in the time domain is to produce an amplitude modulated train of impulses representing the value of the input signal at the instant of sampling. In the frequency domain, the spectrum of the pulse train is a series of discrete frequencies at multiples of the sampling rate. Sampling convolves the spectrum of the input signal with that of the pulse train to produce the combined spectrum shown , with double sidebands around each discrete frequency which are produced by the amplitude modulation. In effect, some of the higher frequencies are "folded back" so that they produce interference at lower ones. This interference causes distortion which is called Aliasing. Aliases cannot be removed by subsequent processing.

If we assume the input signal is band limited to a frequency f_1 , and is sampled at frequency f_S it is clear from the diagram that the overlap (and hence aliasing) will not occur if

$$f_1 < f_S - f_1 \qquad \text{ie.} \quad 2f_1 < f_S$$

Therefore if sampling is done at a frequency at least twice as great as the maximum frequency of input signal, no aliasing will occur and all the signal information can be extracted. This is ***Nyquist's Sampling Theorem***, and it provides a basic criterion for the selection of the sampling rate required by the converter to process an input signal of a given bandwidth.

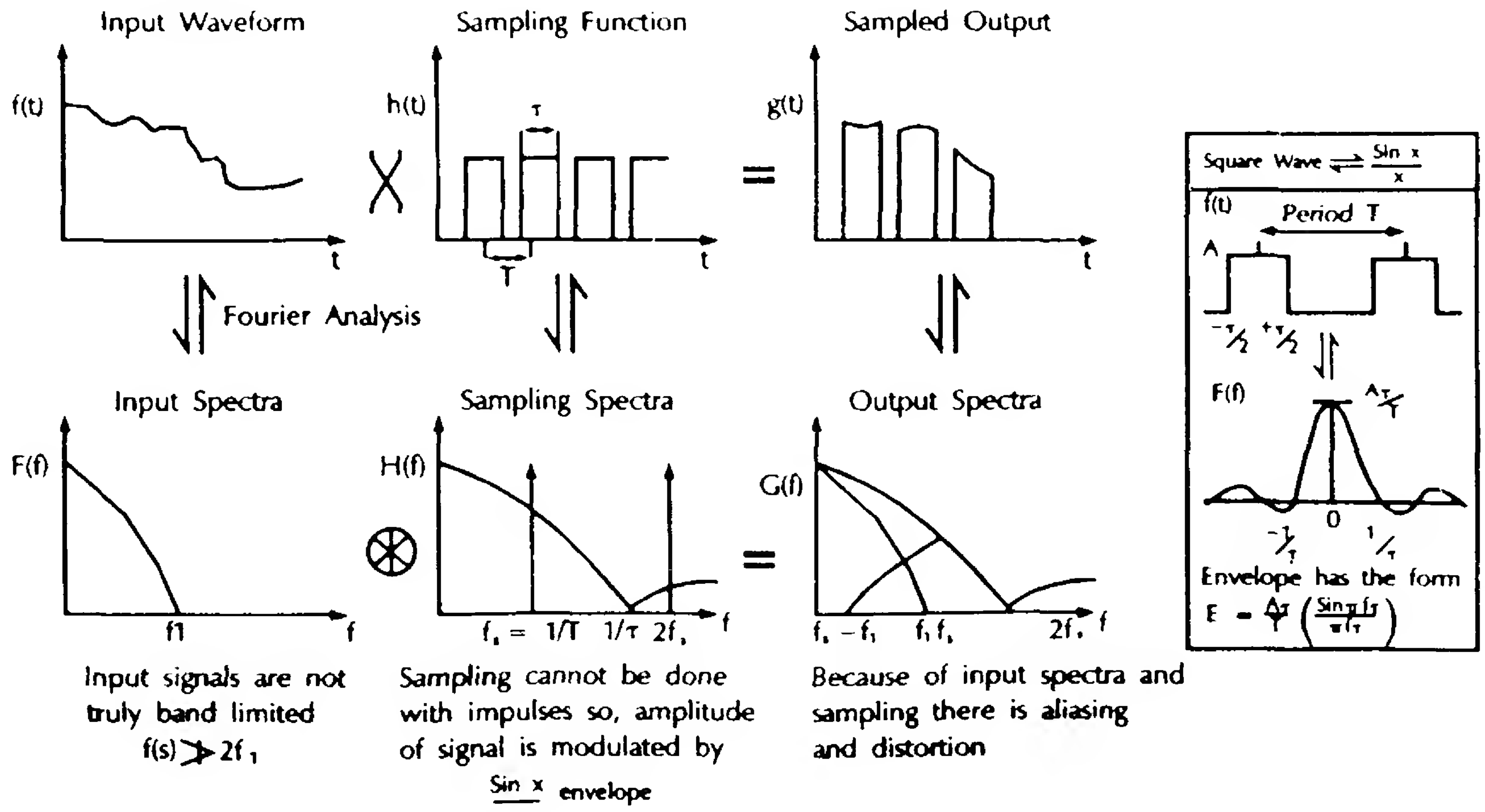

Input Waveform
Sampling Function
Sampled Output
f(t)
h(t)
g(t)
T
t
X
=
Fourier Analysis
Input Spectra
Sampling Spectra
Output Spectra
F(f)
H(f)
G(f)
⊛
f1
f
f₁ = 1/T 1/τ 2f₁
f₁ - f₁ f₁ f₁ 2f₁
Input signals are not truly band limited f(s) ≯ 2f₁
Sampling cannot be done with impulses so, amplitude of signal is modulated by Sin x / x envelope
Because of input spectra and sampling there is aliasing and distortion
Square Wave ⇌ Sin x / x
Period T
A
-τ/2 +τ/2
Aτ/T
0
-1/τ 1/τ
Envelope has the form
E = Aτ/T (Sin πfτ / πfτ)

Figure 3.43 -Real sampling

Real sampling

The concept of an impulse is a useful one to simplify the analysis of sampling. However, it is a theoretical ideal which can be approached but never reached in practice. Instead the real signal will be a series of pulses of period equalling the reciprocal of the sampling frequency. The result of sampling with this pulse train is a series of amplitude modulated pulses.

Examining the spectrum of a square wave pulse train shows a series of discrete frequencies, as with the impulse train, but the amplitude of these frequencies is modified by an envelope which is defined by sinx/x (sometimes written sinc(x)) where x in this case is πf_S. For a square wave of amplitude A, the envelope of the spectrum is defined as

$$Envelope = A\left(\tau/_T\right)\left[\sin(\pi f_S \tau)\right] / \pi f_S \tau$$

The error resulting from this can be controlled with a filter which compensates for the sinc envelope. This can be implemented as a digital filter, in a DSP or using conventional analog techniques. (The TLC320AC01 Analog Interface Circuit has an on-chip (sinx)/x correction filter after its DAC output for this purpose).

Aliasing effects and considerations

In practice, any real signal has infinite bandwidth. However, the energy of the higher frequency components gets increasingly smaller so that at a certain value they can be considered to be irrelevant. This value is a choice that must be made by the system designer.

As we have seen, the amount of aliasing will be affected by the sampling frequency and by the relevant bandwidth of the input signal, filtered as required. The factor that determines how much aliasing can be tolerated is ultimately the resolution of the system. If the system has low resolution, the noise floor is already relatively high and aliasing may not have a significant effect. However, with a high resolution system , aliasing may increase the noise floor considerably and therefore needs to be controlled more completely.

Increasing the sampling rate is one way to prevent aliasing, as we have seen. However, there will be a limit on what frequency this can be, determined by the type of converter used and also by the maximum clock rate of the digital processor receiving and transmitting the data. Therefore, to reduce the effects of aliasing to within acceptable levels, analog filters must be used to alter the input signal's spectrum.

Theoretical SNR for a 14-bit device

The real world analog input to an ADC is a continuous signal with an infinite number of possible states, whereas the digital output is by its nature a discrete function with a number of different states determined by the resolution of the device. It follows from this therefore, that in converting from one form to the other, certain parts of the analog signal that were represented by a different voltage on the input, are represented by the same digital code at the output. Some information has been lost and distortion has been introduced into the signal. This is *Quantisation noise.*

If we take an ideal staircase transfer function of the ADC, the error between the actual input and its digital form will have a uniform probability density function if the input signal is assumed to be random. It can vary in the range ± 1/2 Least Significant Bit (LSB) or ± q/2 where q is the width of one step.

$$p(\varepsilon) = \frac{1}{q} \quad for \ (-\frac{q}{2} \le \varepsilon \le +\frac{q}{2})$$

$$p(\varepsilon) = 0 \ \text{otherwise}$$

The average noise power (mean square) of the error over a step is given by

$$E^2(\varepsilon) = \frac{1}{q}\int_{-q/2}^{+q/2} p(\varepsilon)^2 \, d\varepsilon$$

$$\text{which gives } E^2(\varepsilon) = \frac{q^2}{12}$$

The total mean square error, N^2, over the whole conversion area will be the sum of each quantisation level's mean square multiplied by its associated probability. Assuming the converter is ideal, the width of each code step is identical and therefore has an equal probability. Hence for the ideal case

$$N^2 = \frac{q^2}{12}$$

Considering a sinewave input F(t) of amplitude A so that

$$F(t) = A\sin\omega t$$

which has a mean square value of $F^2(t)$, where

$$F^2(t) = \frac{1}{2\pi}\int_0^{2\Pi} A^2 \sin^2(\omega t)dt$$

which is the signal power. Therefore the signal to noise ratio SNR is given by

$$SNR(dB) = 10Log\left[\left(\frac{A^2}{2}\right)\Big/\left(\frac{q^2}{12}\right)\right]$$

$$\text{But} \quad q = 1LSB = \frac{2A}{2^n} = \frac{A}{2^{n-1}}$$

Substituting for q gives

$$SNR = 10Log\left[\left(\frac{A^2}{2}\right)\Big/\left(\frac{A^2}{3x2^{2n}}\right)\right] = 10Log\left(\frac{3x2^{2n}}{2}\right)$$

$$\Rightarrow \underline{\underline{6.02n + 1.76dB}}$$

This gives the ideal value for a perfect n-bit converter and shows that each extra bit of resolution provides approximately 6 dB improvement in the SNR. In practice, errors in the ADC introduce non-linearities that lead to a reduction of this value.

For a perfect 14-bit converter, the SNR is:

$$6.02x14 + 1.76 \approx 86dB$$

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2. TLC320AC01 Analog Interface Circuit Data Manual; SLAS057A
3. TMS320C2x User's Guide; SPRU014C
4. TMS320C5x User's Guide; SPRU056B
5. TMS320 Fixed-Point DSP Assembly Language Tools; SPRU018C

5 Video Interface Palettes Overview

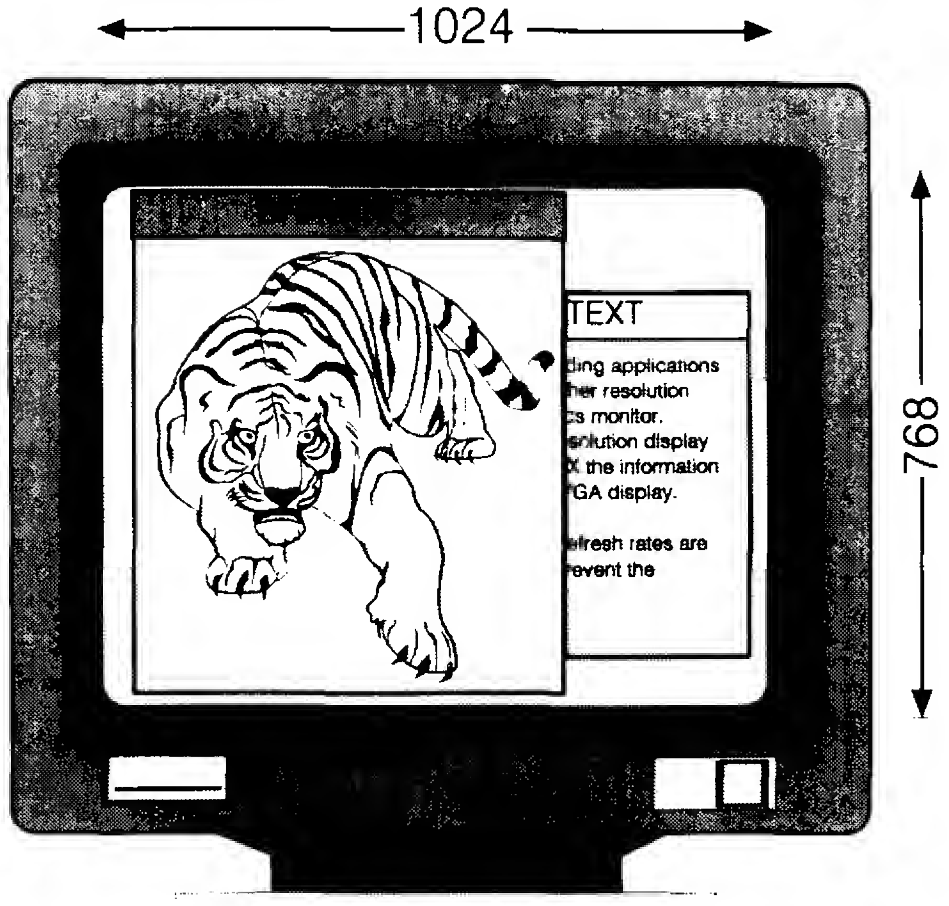
5.1 Introduction

Today's computer systems make extensive use of graphics, both in the user interface such as Windows™ and in the applications S/W such as desktop publications, CAD, etc.

In order to service these applications, high resolution monitors are required together with the circuits that drive them.

Introduction - Resolution and Refresh Rate

- Today's demanding applications require ever higher resolution from the graphics monitor.
- A 1024 x 768 resolution, XGA display has approx 2.5 x the information of a 640 x 480 VGA display.
- Higher screen refresh rates are demanded to prevent the annoying flicker. 72 Hz is the normal standard.



- Blanking ratio is typically 25%
- Dot clock = (No. of pixels per line) x (No. of lines per frame) x (refresh rate) x (blanking ratio)
- EG. Dot clock = 75MHz = 1024 x 768 x 72 x 1.33 or approx 129MHz at 1280 x 1024

Figure 3.44 - Video Interface Palettes - Introduction

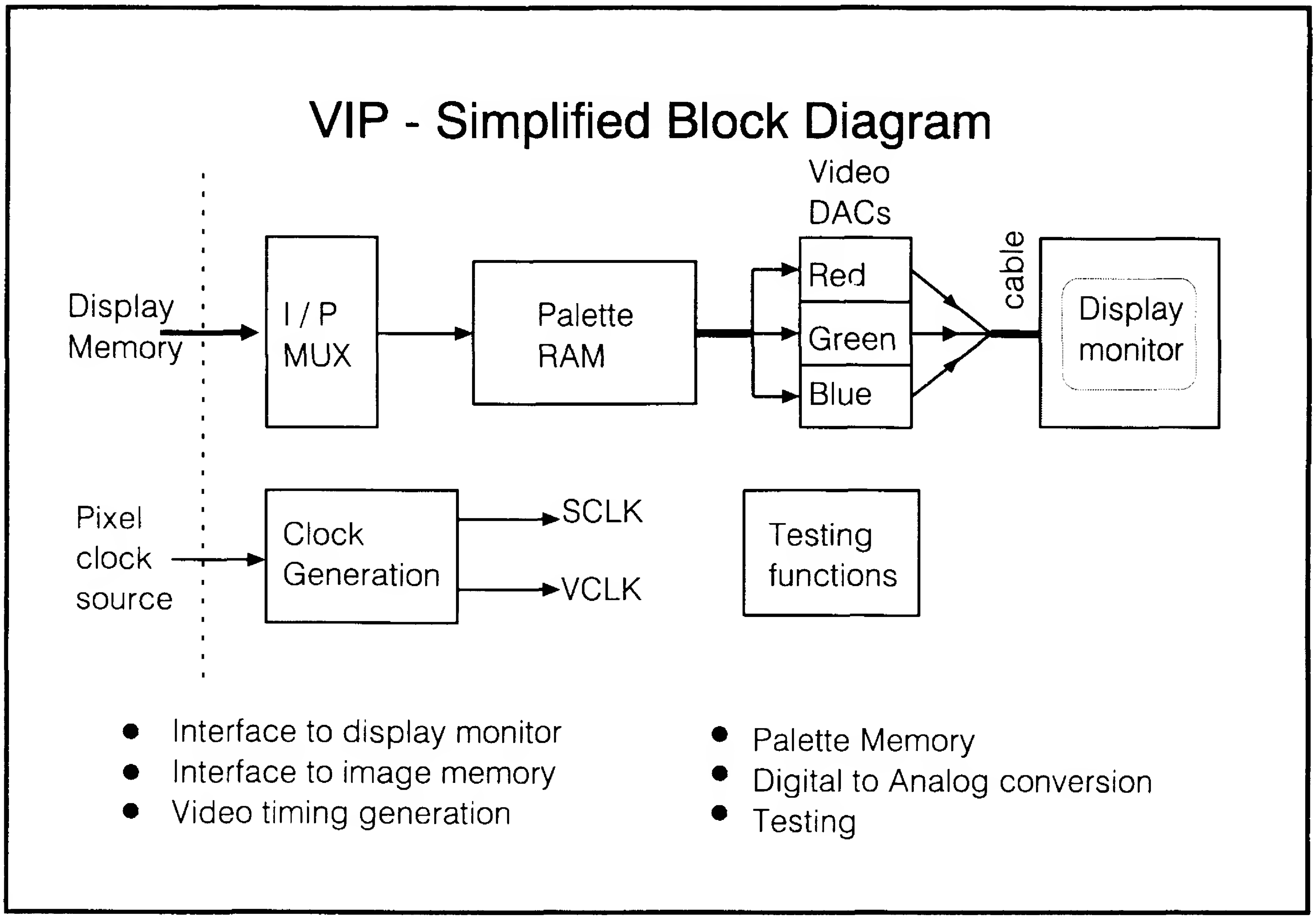
5.1.1 Resolution and Refresh Rate

Over the years IBM VGA (Video Graphics Array), which has a resolution of 640 x 480, has dominated the overall graphics board design. However, as the technology advances, resolutions of 1024 x 768 and higher (such as 1280x1024 and 1600x1280) become the general design target.

There is also a requirement for high refresh rates, to eliminate the annoying flicker effect. The current standard is 72 Hz non-interlaced, but more designers are now considering 76 Hz, 85 Hz and even higher. This combination of high resolution and high refresh rate demands a very fast pixel clock (dot clock).

5.2 A Video Interface Palette

A Video Interface Palette (VIP) is a complete graphics back-end on a chip. It interfaces the Video RAM of a PC or workstation with the graphics monitor. It contains a combination of fast logic functions and video DACs to transform the stored image into an analog signal for input to the monitor.



- Interface to display monitor
- Interface to image memory
- Video timing generation
- Palette Memory
- Digital to Analog conversion
- Testing

Figure 3.45 - VIP Simplified Block Diagram

The input multiplexer on the VIP will allow different numbers of bits-per-pixel and different numbers of pixels-per-transfer under S/W control. This, together with a programmable dot clock source, allows the computer display to be set-up with different screen resolutions and numbers of colors.

In the 1, 2, 4 or 8 bits-per-pixel modes the pixel data, from the Frame Buffer goes, not to the DACs, but addresses a 256 location x 24 bit palette RAM within the VIP. This allows up to 256 colors to be resident at any one time with the 24 bits being composed of 8 bits each of red, green and blue data. The 256 colors chosen are downloaded by the host depending on the application.

The VIP also supports 16-bit and 24-bit true color modes, where the data from the Frame Buffer goes directly to the video DACs. This is usually used to present "real" images to the screen, the 24-bit mode providing "photo-realistic" images.

Because the VRAM serial port speed is limited to approximately 50 MHz, then for dot clock speeds above 50 MHz, more than 1 set of pixel data has to be transferred in each read cycle. As more colors are demanded at higher and higher resolution then wider pixel busses are required to effect the transfer and, effectively, increase the bandwidth of the pixel bus.

With the advent of Windows™ 3.1 which supports 24-bit true color applications, there is an increasing demand for graphics systems which support 24-bit true color at 1024x768 resolution. As the dot-clock is approximately 80 MHz at 1024x768 resolution, then 2 pixels need to be read into the VIP in each transfer. For 24-bit true color the pixel bus width would have to be 48-bits wide. In fact a 64-bit wide pixel bus is traditionally used, allowing an 8-bit overlay function.

Resolution, Colors and Frame Store Size

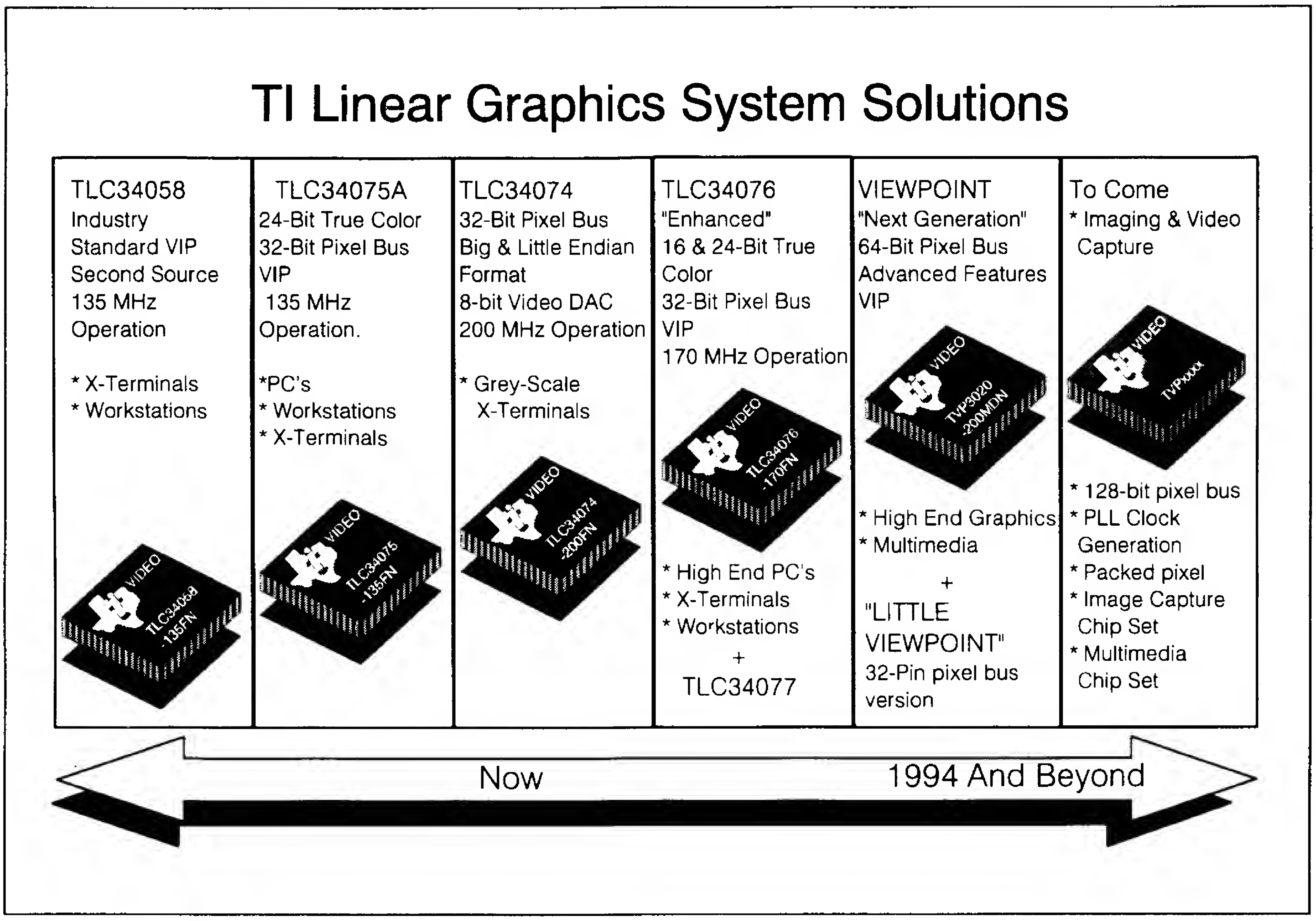
MIN. NUMBER OF PIXELS PER TRANSFER *	FRAME RATE	APPROX DOT CLOCK	SCREEN RESOLUTION	FRAME STORE SIZE FOR NUMBER OF COLORS (MBytes)						
1	60Hz	38MHz	800 600	0.25	0.5	0.5	1	1	2	2
	72Hz	46MHz								
2	60Hz	63MHz	1024 768	0.25	0.5	1	2	2	3 **	4 **
	72Hz	76MHz								
4	60Hz	105MHz	1280 1024	0.5	1	2	3 **	3 **	4 ***	6 ***
	72Hz	126MHz								
4	60Hz	164MHz	1600 1280	0.5	1	2	4 **	4 **	6 ***	8 ***
	72Hz	197MHz								
NUMBER OF COLORS				4	16	256	32K	64K	16M	16M + 256 OVERLAY
NUMBER OF BITS PER PIXEL				2	4	8	15 (16)	16	24	32

* AT APPROX 45MHz VRAM SERIAL PORT SPEED
** NEEDS PALETTE WITH 64-BIT PIXEL PORT OR EXTERNAL MUX
*** NEEDS PALETTE WITH MORE THAN 64-BIT PIXEL PORT AT PRESENT VRAM SPEED OR EXTERNAL MUX

Figure 3.46 - Resolution, Colors and Frame Store Size

5.3 Video Interface Palettes Roadmap

TI produces a substantial range of Video Interface Palettes with new devices constantly under development to keep pace with the rapidly developing PC market.



TI Linear Graphics System Solutions

TLC34058	TLC34075A	TLC34074	TLC34076	VIEWPOINT	To Come
Industry Standard VIP Second Source 135 MHz Operation * X-Terminals * Workstations	24-Bit True Color 32-Bit Pixel Bus VIP 135 MHz Operation. *PC's * Workstations * X-Terminals	32-Bit Pixel Bus Big & Little Endian Format 8-bit Video DAC 200 MHz Operation * Grey-Scale X-Terminals	"Enhanced" 16 & 24-Bit True Color 32-Bit Pixel Bus VIP 170 MHz Operation * High End PC's * X-Terminals * Workstations + TLC34077	"Next Generation" 64-Bit Pixel Bus Advanced Features VIP * High End Graphics * Multimedia + "LITTLE VIEWPOINT" 32-Pin pixel bus version	* Imaging & Video Capture * 128-bit pixel bus * PLL Clock Generation * Packed pixel * Image Capture Chip Set * Multimedia Chip Set

VIDEO
TLC34058
-135FN
VIDEO
TLC34075
-135FN
VIDEO
TLC34074
-200FN
VIDEO
TLC34076
-170FN
VIDEO
TVP3020
-200MDN
VIDEO
TVPxxxx
Now
1994 And Beyond

Figure 3.47 - Video Interface Palettes Roadmap

Section 4
Data Transmission

Section Contributions by:

Bridget Barrett
Ralf Asmussen
Alun Webber
Geoffrey Arnold

TEXAS INSTRUMENTS

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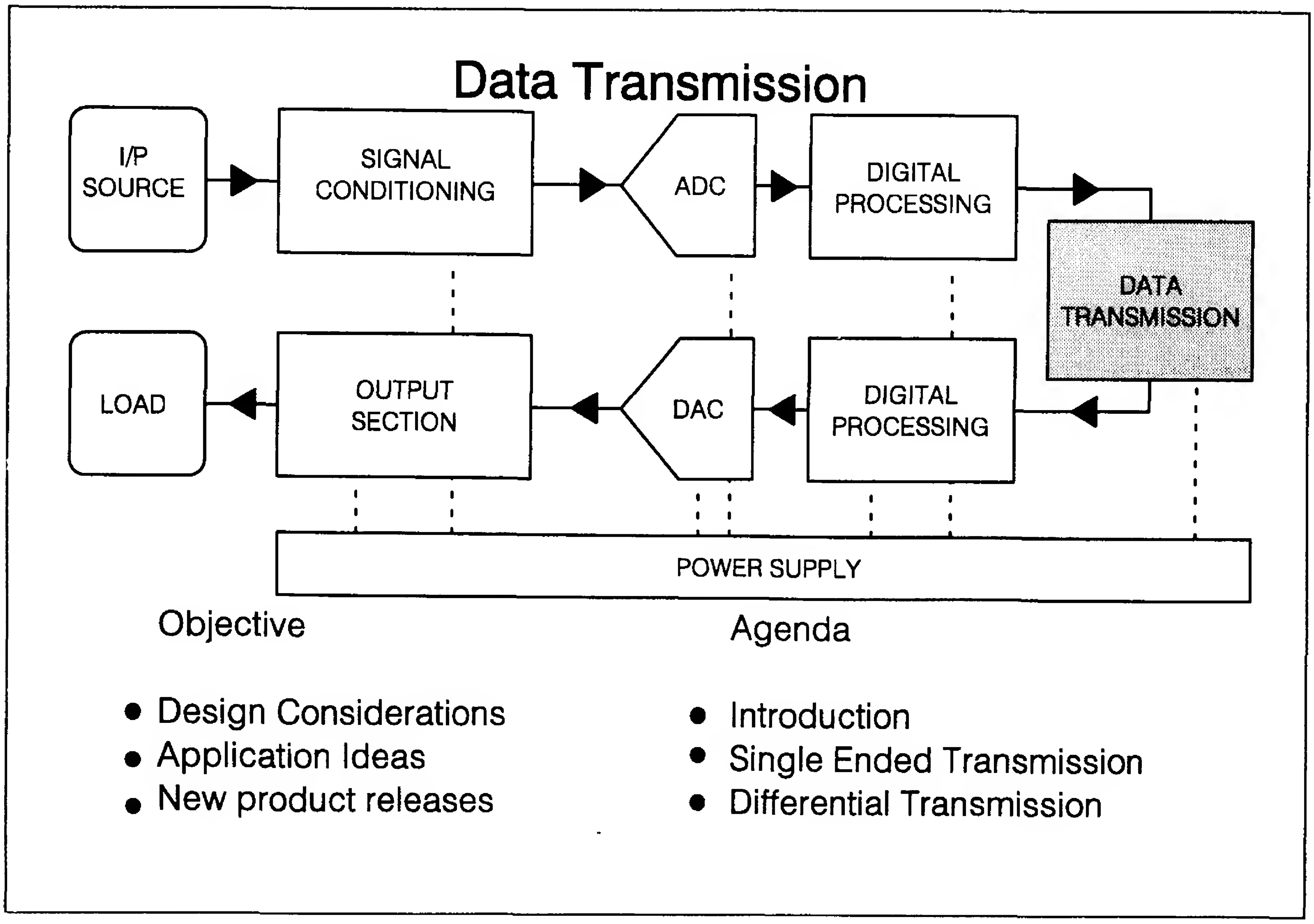
1 Introduction

1.1 Data Transmission

It may seem strange that Texas Instruments' 'Data transmission' products are included within the Linear seminar. Data Transmission as part of Texas Instruments' Linear Products portfolio is concerned with the standards involving transmitting data at relatively high speeds down long line lengths, the considerations for which are primarily of an analog more than a digital nature. Likewise the design of data transmission ICs requires experienced analog engineers to implement functions such as slew rate limiting, receiver filtering and common-mode protection.



Data Transmission

I/P SOURCE
SIGNAL CONDITIONING
ADC
DIGITAL PROCESSING
DATA TRANSMISSION
LOAD
OUTPUT SECTION
DAC
DIGITAL PROCESSING
POWER SUPPLY

Objective

- Design Considerations
- Application Ideas
- New product releases

Agenda

- Introduction
- Single Ended Transmission
- Differential Transmission

Figure 4.1 - Data Transmission

In this year's seminar we will review single ended transmission standards and differential transmission standards. We will explore the circumstances under which to select a given standard and review design considerations when implementing the standard.

1.1.1 The Need for Transmission Standards

Data transmission standards evolved for two main reasons: From the need to transmit data reliably over long distances, and to provide a standard interface to facilitate communication between equipment from different suppliers. Although TTL/Logic signal levels and products can be used, they generally lack the power handling capabilities, robustness and noise margins required for reliable transmission. Indeed for backplane equipment, TTL is no longer specified for the newer high speed standards, such as Futurebus+ which uses BTL transceivers. In general the standards concerned with transmitting data over long distances incorporate wider voltage swings, increased robustness and higher power outputs than can be delivered using conventional 'Logic' products. Similarly the sub-micron technologies used in the fabrication of today's logic devices cannot provide the power handling and robustness necessary for successful long distance transmission.

1.1.2 Specialist Technologies

This leads to the need for specialist ICs, and technologies, to meet the exacting requirements of these transmission standards. The traditional technological answer has been to utilise the inherent robustness afforded by bipolar technologies, however the additional need for low power consumption and high levels of integration no longer makes this attractive. SC manufacturers are now having to develop their technologies to accommodate these requirements. TI has introduced its proprietary LinBiCMOS™ technology combining the robustness of bipolar together with the power consumption and integration afforded by CMOS. Other manufacturers are using pure CMOS and integrating Schottky diodes to the same end. The result is very specialised and reliable products that are able to withstand the harsh environment unique to data transmission products.

Texas Instruments has been a leading supplier of data transmission products for many years, and is continually innovating new fields. Although the following sections are limited to the more common interface standards, TI is actively involved in many new emerging standards and markets, for example Futurebus+, a backplane standard with virtually no ceiling on data rate, the high speed serial data link evolving from the P1394 committee and multiplex wiring systems such as ABUS, CAN and VAN. The reader is advised to contact a TI representative for information on these product areas.

With the considerable expertise in design, product definition and range of technologies Texas Instruments is the ideal choice for supplying your data transmission product requirements.

1.1.3 About This Section

This Section is split into distinct sections each of which provides a practical rather than theoretical approach to in an attempt to give the reader an insight into popular data transmission techniques and standards. The Section is split as follows:

Interface Standards

Single Ended

- Low data Rates
- Restricted Line Length <20 metres
- Common mode restrictions

Differential

- Long Line Length >1.2Km
- Common mode cancellation
- High Data Rate >10MBPS

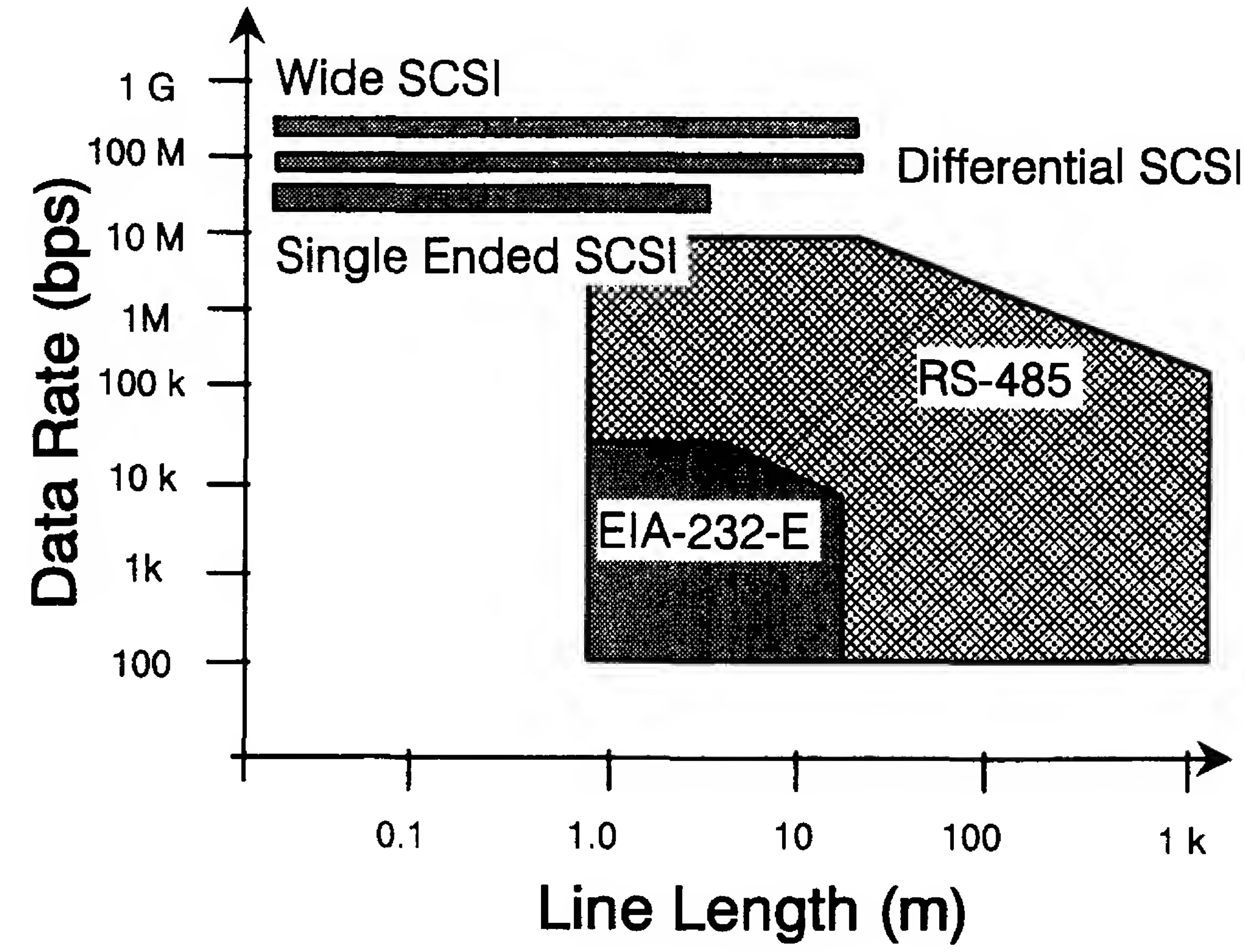


Figure 4.2 - Interface Standards

1. Introduction: An overview of the various factors that affect any data transmission system. Under discussion are the line length versus data rate trade-off, sources of distortion and their effect, and an explanation of the use of eye patterns as a tool to measure transmission quality.

2. Single Ended Transmission: A discussion on the pros and cons of single ended transmission together with the various techniques and standards which use this configuration. The majority of the section is concerned with EIA-232, by far the most popular single ended transmission standard. The standard is discussed in detail with particular attention paid to the changes made in the 'E' revision. Also covered is the use of '232' at higher data rates, up to 116 kbps (kilo bits per second) and an application focus on the popular DB9 PC interface. Towards the end of this section multi-point transmission is discussed. Attention is paid to Texas Instruments' new products throughout the section. (The generic '232' standard will be referred to in this book as EIA-232, where a parameter is unique to a specific revision the EIA-232 reference will be used.)

3. Differential Transmission: A discussion on pros and cons of differential (balanced) transmission together with various techniques and standards which use this configuration. The majority of the section is concerned with the design considerations when using a differential transmission standard making reference to RS-485. The section concludes by looking at implementing differential SCSI for line lengths up to 25m using RS-485 and Meter Bus as a standard for line lengths up to 4km using differential data transmission.

1.2 Types of Transmission

Most commonly transmission of data occurs directly from one logic gate to another. Low power Schottky TTL and HCMOS can operate at clock frequencies of up to 40MHz. Interconnects must be short (a few 100s of millimetres) and special care taken to assure adequate noise margin and minimum line reflections. The higher speeds of Advanced Schottky TTL and ECL gates place even more emphasis on properly terminated, well defined lines.

There are limiting factors to directly driving over longer distances using standard logic devices. The most important of these is the environmental noise level, whether this is directly radiated or by ground shift potentials. The guaranteed noise margin of standard TTL is +/- 0.4V and is insufficient in most applications.

Many specialised data transmission devices have been developed to overcome this problem, they work by increasing the signal level on a line and thereby improving the noise margin. The techniques involved use single ended or differential (balanced) operation with either voltage mode or current mode drive to the line.

Twisted pair and coax lines are used for single ended drive over longer distances but single and multi wire can be used where the data rate is low and line lengths are short. For differential data transmission a twisted pair is normally used.

Single-Ended Transmission

Numerous integrated circuit devices are available for driving single ended data transmission lines. Some are general purpose and others have been designed to meet specific industrial standards.

Advantages and disadvantages of single ended drivers :

Advantages

- Simplicity : minimum connections
- Low cost

Disadvantages

- Radiates RFI easily
- Poor noise immunity
- Coax improves noise but is expensive
- Limited line lengths and data rates due to susceptibility to interference signals

Differential (balanced) Transmission

The ability to transmit data from one location to another without errors requires immunity to noise. At high data rates, on long lines or under noisy conditions, differential data transmission has an advantage because it is more immune to noise interference than single-ended transmission.

Voltages induced onto the data lines by ground noise or switching transients appear as common-mode signals at the receiver input. Since the receiver has a differential input it corresponds only to the differential data signal. Differential drivers and receivers can operate safely within specified common-mode voltage ranges. Differential line drivers and receivers are designed for general purpose applications as well as specific standards.

Advantages and disadvantages of differential (balanced) data transmission relative to single ended transmission are :

Advantages

- High common mode noise voltage rejection
- Reduced line radiation - less RFI
- Improved speed capabilities
- Drive longer line lengths

Disadvantages

- Slightly higher costs (sometimes)
- Must be used with twisted pair or other types of balanced transmission lines

Referring to Figure 4.2 we can see the relationship of each transmission standard when comparing data rate and line length.

1.2.1 Single Ended Transmission : EIA/TIA-232

EIA-232 or 'Recommended Standard' 232 is defined in the ANSI (American National Standard Institution) specification as "The Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange". The standard employs a single ended serial transmission scheme and outlines the set of rules for exchanging data between computer equipment, originally this being a Computer Terminal (DTE) and a modem (DCE). The standard has evolved over the years with the latest 'E' revision released in July 1991. The standard is now known as EIA/TIA-232-E, with EIA standing for the Electronic Industries Association and TIA for the Telecommunications Industry Association.

As with previous revisions of the standard the maximum data rate is defined as 20 k bits per second (kbps) although there are now a number of software applications that now push this data rate up to 116 kbps, well outside the standard. The 'C' revision defined the maximum line length as 15 metres however this failed to comprehend the type of cable used and consequently the load capacitance on the line driver. Both the 'D' and 'E' revisions addressed this by more correctly defining the line length in terms of load capacitance. The maximum load capacitance is specified as 2500 pF that translates using standard cables to between 15 and 20 metres. Line length and data rate are limited as the standard employs single ended communication which is prone to external factors. For longer line lengths and higher data rates a differential balanced line communication link is essential.

1.2.2 Differential Transmission : RS422-A

The balanced transmission line standard EIA RS-422 was developed in 1975 to interface a host computer's data, timing or control lines to its peripherals. The standard was revised (RS-422A) in December 1978 bringing it in line with its present specification.

A RS-422 line allows for only one way communication (simplex) mode. By using a differential twisted pair transmission media (not specified in the standard) and a RS-422 receiver with its minimum 7V common mode voltage capacity it is less susceptible to noise picked up in hostile environments via the long cables allowed by the standard. Each driver can drive up to 10 receivers. The specification in the standard places no restrictions on minimum or maximum operating data rates but rather on the relationship of transition speed to a unit interval. However, data rates up to 10Mbps are supported and a line length up to 1200 metres is given as a guide-line , but not at the maximum data rate.

When operating at low data rates (below 200kps) or at any speed where the ratio of the driver's output rise time to the one way propagation delay time of the cable exceeds ten, the cable will not act as a true transmission line and therefore termination is not absolutely necessary. Under all other conditions, the cable loading can no longer be considered as a lumped parameter but must be considered as a transmission line.

The characteristic impedance of twisted pair cable is a function of frequency and cable type, however typical twisted pair cable impedance's lie in the range 100Ω to 120Ω.A termination resistor with an impedance similar to the cable's characteristics impedance should only be connected at the furthest end of the cable.

1.2.3 Differential Transmission : RS-485

RS-485 was primarily an upgrade to the EIA RS-422-A standard utilising the same signal levels but facilitating half duplex multi-point communication. The standard is less complex than the EIA-232 standard as it only specifies the physical layer of the transmission scheme. Hardware such as the connector is left to the user to define. The standard specifies a balanced transmission line whose maximum line length is undefined but is nominally 1.2 km for 24 AWG cable based on 6 dB signal attenuation. The maximum data rate is also undefined but is specified by the relationship of signal rise time to bit time which is influenced both by the line driver and the line length and the line loading. In the majority of applications it is the line length that is the limiting factor on data rate due to signal dispersion. This is discussed in later sections.

1.2.4 Single and Differential Transmission : Small Computer Systems Interface (SCSI)

SCSI is an industry-standard interface, defined by the ANSI, for the interchange of data between computer and computer peripherals. Standard SCSI is a byte wide parallel interface for high speed data transfer over relatively short distances. The SCSI bus is bi-directional and is terminated at both ends of the cable to reduce reflections. For the single ended interface the standard specifies a maximum line length of 6 metres. The maximum data rate is not specified but at present 5 Million Transfers per second (MTps) is achievable using active termination. This can be increased up to 10 MTps using innovative termination as we will discuss later. For longer line length applications, up to 25 metres, the SCSI standard defines the interface using the RS-485 standard as the physical layer. This pushes the data rate to 10 MTps over the full 25 metres which equates to 80 Mbps. A further development of SCSI is 'Wide' SCSI which increases the data bus to 16 bits wide. Using the 10 MTps differential interface this increases the bit rate to 160 Mbps.

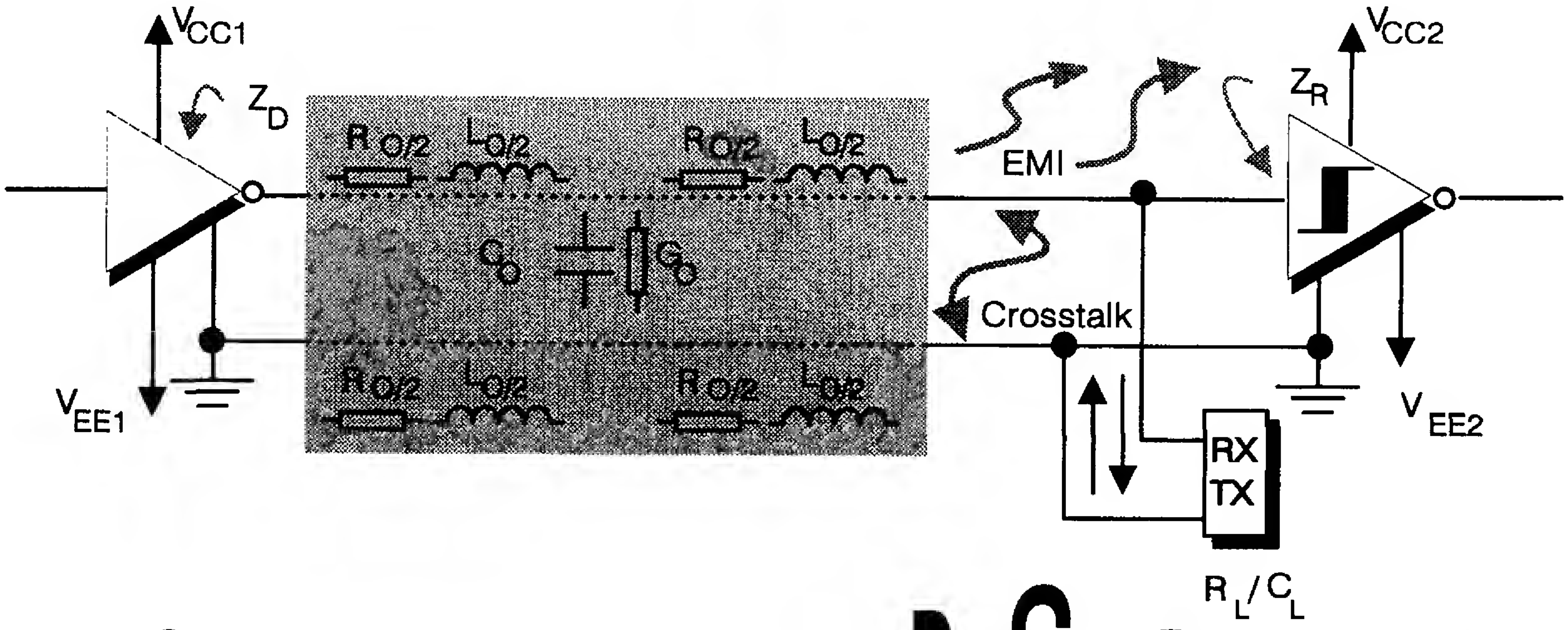
1.2.5 Summary of EIA Interface Standards

Parameter		EIA-232	RS-423-A	RS-422-A	RS-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
Maximum Cable Length (m)		15	1200	1200	1200
Maximum Data Rate (bps)		20 k	100 k	10 M	10 M
Maximum Common-Mode Voltage (V)		±25	±6	6 to –0.25	12 to –7
Driver Output	Unloaded	±5	±3.6	±2	±1.5
Levels (V)	Loaded	±15	±6	±5	±5
Driver Load (Ω)		3 k to 7 k	450 (Min)	100 (Min)	60 (Min)
Driver Slew Rate		30 V/μs (Max.)	External Control	NA	NA
Driver Output Short Circuit Current Limit (mA)		500 to V_{CC}	150 to GND	150 to GND	150 to GND 250 to –7 or 12 V
Driver Output Resistance -	Power on	NA	NA	NA	12 k
High Z state (Ω)	Power off	300	60 k	60 k	12 k
Receiver Input Resistance (Ω)		3 to 7	4	4	12
Receiver Sensitivity		±3 V	±200 mV	±200 mV	±200 mV

1.3 System Influences

Signal dispersion, attenuation and noise are always present in data transmission systems and strictly limit performance by distorting the signal. We will consider each one of these in turn.

System Influences



- Signal Attenuation
- Signal Dispersion
- Noise

= Distortion

Figure 4.3 - System Influences

1.3.1 Signal Attenuation

Any data transmission over wire experiences losses and distortion due to distributed constants present along the cable: distributed series inductance, distributed shunt capacitance, distributed series resistance and distributed shunt conductance. Attenuation of the signal in a cable is affected by each of the these components. The series resistance, **R**, is frequency dependent and is a result of the DC resistance of the cable and the skin effect. Skin effect is a term which refers to the tendency of electrons to travel to the surface of a conductor at higher frequencies, thereby reducing the overall cross sectional area and increasing the resistance. The series inductance, **L**, represents the opposition to change in current levels caused by the collapsing and expanding magnetic fields created due to fluctuating current levels. The shunt capacitance, **C** ,is created by the two conductors in close proximity and separated by a dielectric. As the signal frequency increases the capacitive reactance decreases, consequently reducing the opposition to current flow. The final component, shunt transconductance or **G**, is a function of the dielectric loss of the insulation around each conductor which allows some leakage current to pass between conductors. In modern dielectrics this is often assumed to be negligible.

The overall effect of these distributed constants is called the characteristic impedance of the line, $\mathbf{Z_O}$, and is expressed as:

$$Z_O = \sqrt{\frac{\mathbf{R} + \mathbf{j2\pi fL}}{\mathbf{G} + \mathbf{j2\pi fC}}}$$

Where:

L is in henries/unit length
R is in ohms/unit length

C is in farads/unit length
G is on siemens/unit length

The current/voltage relationship of an incident wave travelling down a transmission line in the direction of the load will be determined by this equation. Equally a reflected wave travelling from the direction of the load will also be dependent on this relationship. We will revisit this equation when we discuss transmission line termination in section 1.5. The signal velocity along the transmission line and the attenuation depends upon the propagation constant γ of the line. The propagation constant, when separated into its real and imaginary parts, is symbolised by $\alpha + j\beta$ where α is known as the attenuation constant and β as the phase constant. α determines the rate of attenuation and has units of nepers per unit length, and β determines the phase velocity, where:

Phase velocity,

$$\mathbf{Vp} = \frac{\omega}{\beta}$$

Where ω is the angular velocity.

Additionally, the propagation constant,

$$\gamma = \alpha + j\beta = \sqrt{(\mathbf{R} + j\omega\mathbf{L})(\mathbf{G} + j\omega\mathbf{C})}$$

In practice the attenuation of a particular cable can be determined from manufacturers data where usually a curve of bit rate or frequency is plotted against dB, usually quoted per 100 ft or 30 metres. The attenuation constant, β, can be converted to dBs by multiplying by 8.686.

The maximum attenuation allowable will be dependent on the system configuration but a figure of 6 dBV maximum is a good guide. Actual curves are discussed later in the differential transmission section.

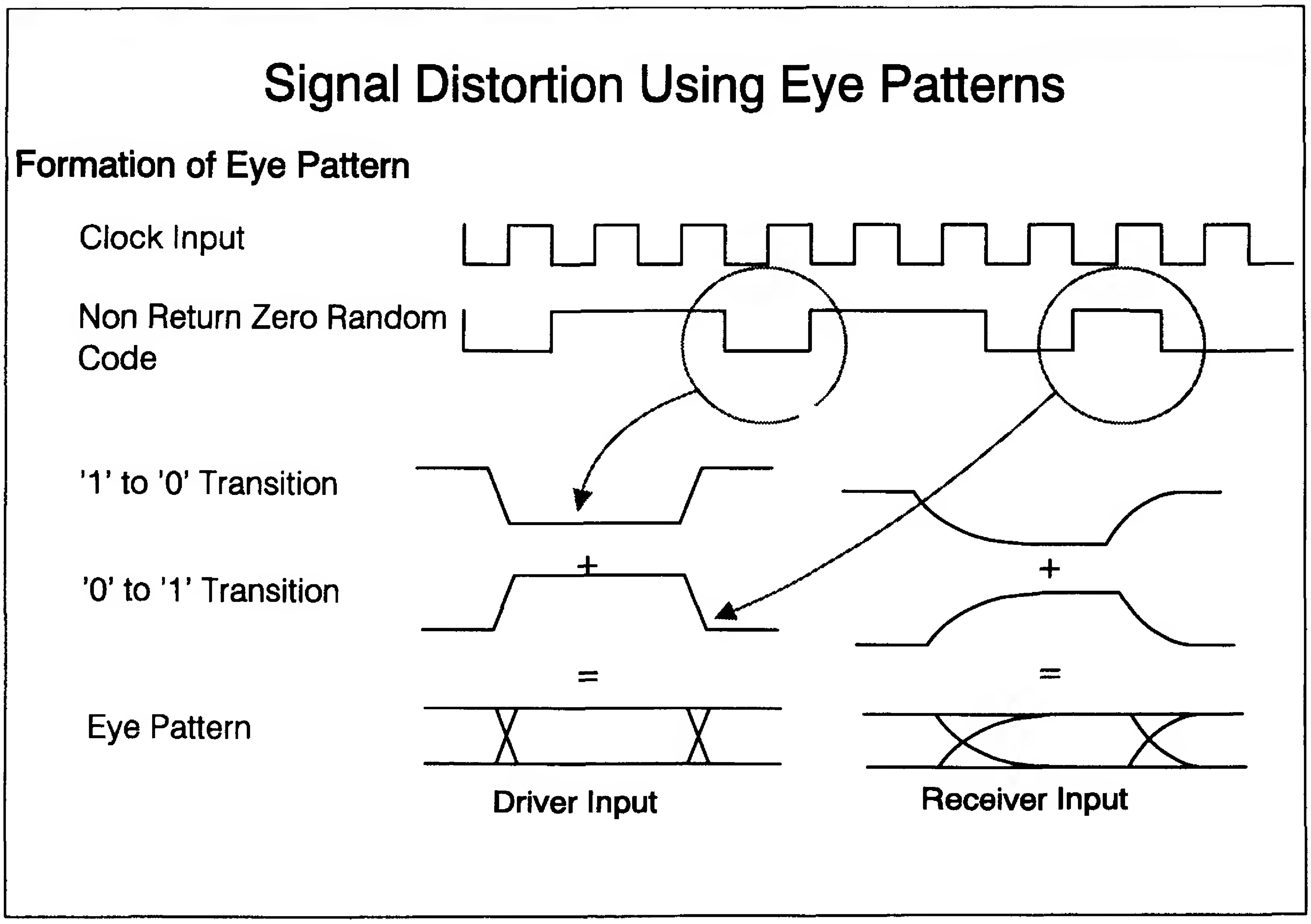


Figure 4.4 - Signal Distortion Using Eye Patterns

1.3.2 Signal Dispersion

One of the primary causes of signal distortion is the effect known as frequency dispersion. As discussed in 1.3.1. phase velocity and attenuation are both frequency dependent and whose effect is to distort and delay the signal pulse. The high frequency components contained in the leading and lagging edges of a pulse experience minimum delay but experience maximum attenuation. The pulse top and low frequency components are subjected to increased delays. The result is that various parts of the pulse arrive at the receiving end at different times and at differing levels causing distortion of the original signal. It follows the longer the line length the more the bit rate must be reduced. In many transmission systems it is this factor alone which determines the maximum signalling rate.

Once again cable manufacturers sometimes specify a bit rate versus line length curve but a better way to check signal distortion of your system is by the use of eye patterns or eye diagrams. Indeed cable manufacturers generate their bit rate/distance curves using eye pattern measurements. Eye patterns allow you to visibly see and measure signal distortion as a function of data rate. See later sections on how to implement Eye Patterns.

1.3.3 Noise Considerations

Noise is generated from a variety of sources and can strongly influence how you implement your data transmission system. All extraneous signals appearing at the receiving end of the transmission circuit that are not due to the input signal are considered as noise. The two most likely sources of noise that will affecting data transmission systems in the context of this section are common-mode voltages and cross talk. We will discuss both these types of noise in later sections.

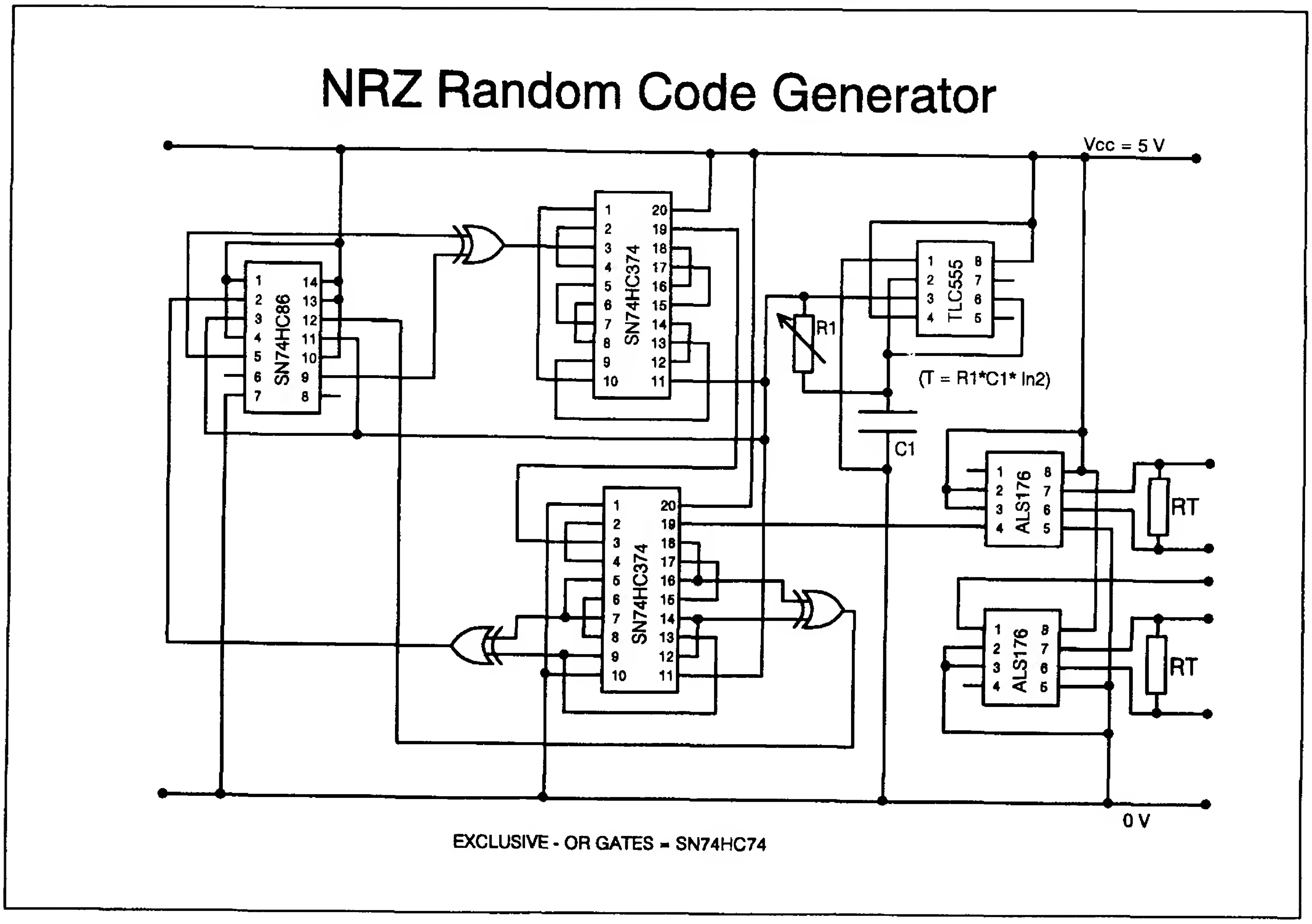


Figure 4.5 - NRZ Random Code Generator

1.4 Eye patterns

To determine the effects of signal distortion, noise etc. on Intersymbol interference (ISI) in a data transmission system the eye pattern is used. ISI is the effect of neighbouring pulses in a pulse train spilling over into adjacent pulses and forces a reduction in the allowable permitted pulse rate for a given line length in order to maintain adequate distinction between adjacent pulses. The eye pattern is displayed on an oscilloscope with the term 'Eye' coming from the appearance of the trace on the CRT.

1.4.1 Setting up the eye pattern

The eye pattern is obtained by applying a random non return zero (NRZ) code down the transmission line under test. This represents all possible pulse combinations. The signal at the receiving end of the line is connected to the vertical amplifier of an oscilloscope, with the 'scope triggered using the synchronisation clock to the NRZ code generator on a separate trace. See figure 4.6 Over any one unit interval the random code generator should produce a combination of signals. The resulting signals can then be viewed on the oscilloscope over one unit interval, each unit interval should resemble an eye, similar to figure 4.7. For differential transmission both signals at the end of the transmission line should be applied to separate amplifiers on the oscilloscope and then summed using the summation facility on the oscilloscope.

Figure 4.5 shows a circuit to generate the NRZ code. In this case we have used it to test the RS-485 SN75176 type transceiver.

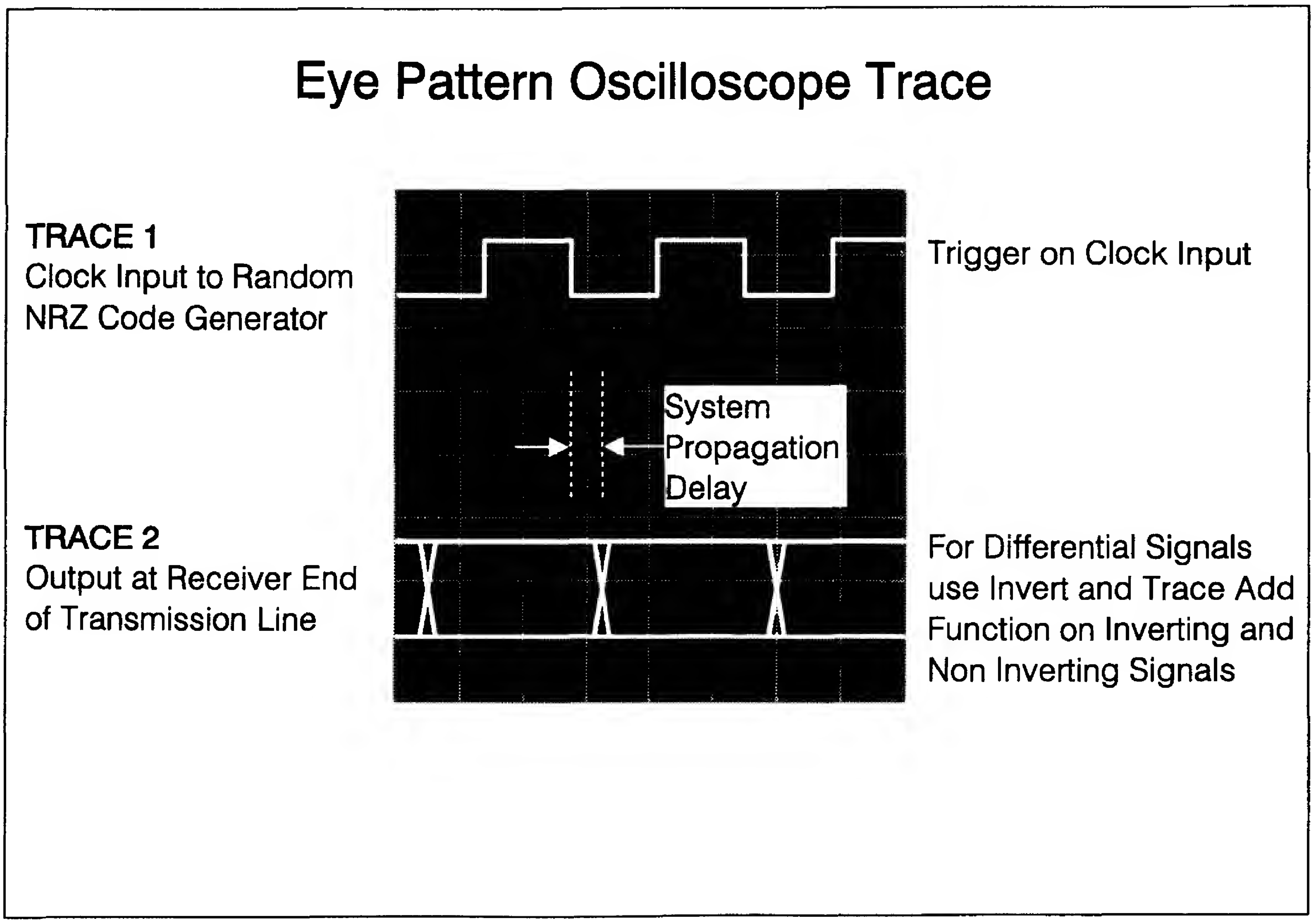

Eye Pattern Oscilloscope Trace
TRACE 1
Clock Input to Random NRZ Code Generator
Trigger on Clock Input
System Propagation Delay
TRACE 2
Output at Receiver End of Transmission Line
For Differential Signals use Invert and Trace Add Function on Inverting and Non Inverting Signals

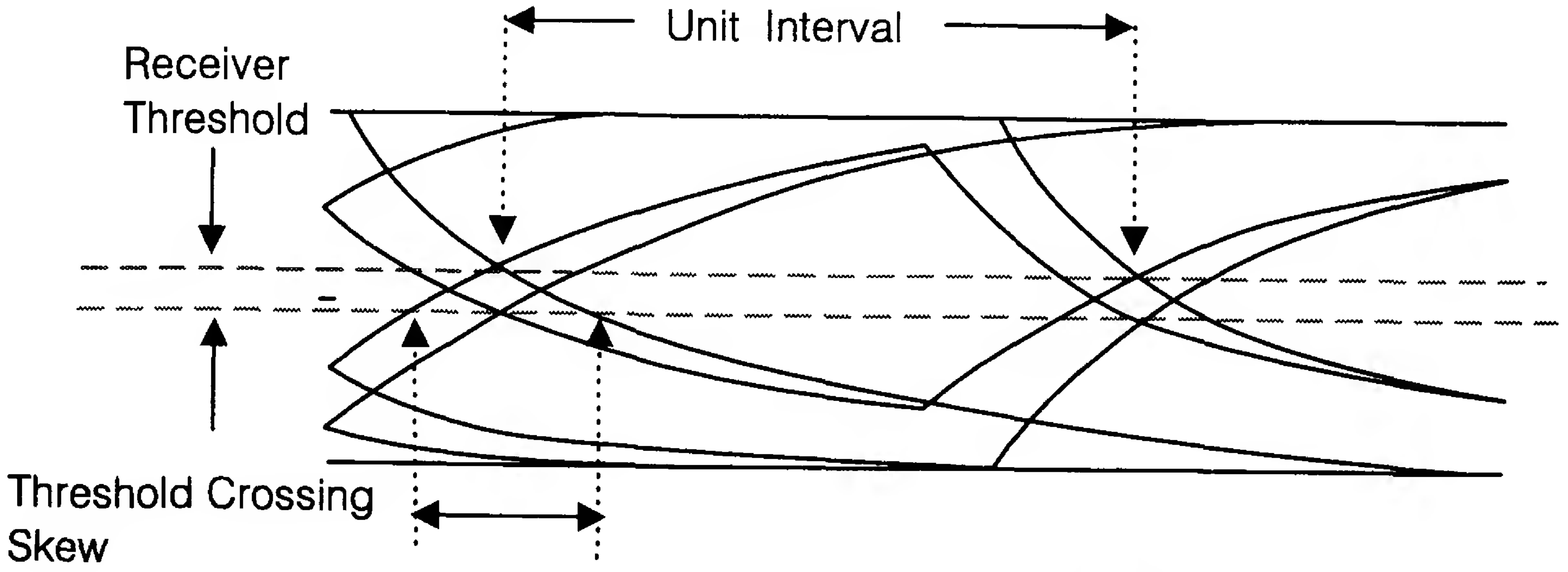
Figure 4.6 - Eye Pattern Oscilloscope Trace

1.4.2 Taking Measurements from Eye Patterns

Before considering actual measurements the first key indicator on the performance of the transmission system can be seen by simply looking at the eye pattern. The 'openness' of the eye is an indication of the 'quality' of the transmitted signal and is an indication of the noise and distortion tolerance of the system.

For actual measurements the decision points of the transceiver should be superimposed upon the eye pattern. The vertical distance between the decision points and the signal trace is an approximate indication of the noise margin of the system. The horizontal appearance of the eye can be used to determine the maximum jitter tolerance of the system. A good guide, and one that is used by cable manufacturers to determine data rate versus line length curves, is to design with no more than 5% jitter. Where % jitter is defined as the ratio of Threshold crossing Skew to unit interval as shown in Figure 4.7. Jitter is caused by a number of factors including , signal frequency, noise and cross talk. (Noise frequency can modulate the transmitted signal, for example 50 Hz hum or from other low frequency sources). It should also be noted at this point the effect of threshold misalignment which can cause severe problems with the received signal, reducing the detected pulse width considerably.

Measuring Signal Transmission Quality


Unit Interval
Receiver Threshold
Threshold Crossing Skew

$$\% \text{ Jitter} = \frac{\text{Threshold Crossing Skew}}{\text{Unit Interval}} \times 100\%$$

Design With No More than 5% Jitter

Figure 4.7 - Measuring Signal Transmission Quality

2 Single Ended Transmission

2.1 General Information

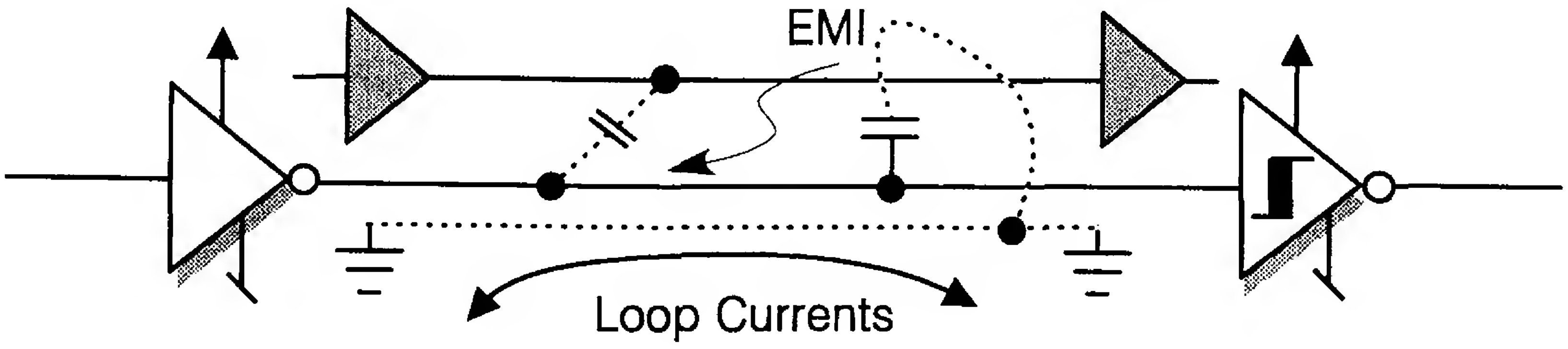
This section is concerned with the transmission topology know as single ended transmission where data is transmitted through a single wire with reference to ground. A single ended transmission line is often referred to as an unbalanced line where one of the signal lines is kept at ground. This form of transmission is by far the most common however the trend is towards the more reliable differential or balanced line transmission where much of the drawbacks of single ended systems are addressed.

The first part in section 2 covers the popular EIA-232 transmission standard used in many applications, particularly those associated with communicating with personal computers e.g. data loggers, PC mouse.

The second part of this section will review the problems associated with mutli-point single ended transmission and particularly address ways of increasing the transmission line bandwidth.

However, before we move on it is useful to understand the pros and cons of single ended transmission.

Single Ended Transmission



Advantages

- Low system cost
- Simple to implement

Disadvantages

- Noise and crosstalk
- Ground shifts
- Low data rates
- Low line lengths

Figure 4.8 - Single Ended Transmission

2.1.1 Advantages of single ended transmission

The advantages of single ended transmission relate to simplicity and cost of implementation. Obviously a single ended system requires one line per signal and is therefore ideal for parallel communication where many lines are required e.g. PC parallel printer port or serial communication with many handshaking lines e.g. EIA-232. Cabling costs can be kept to an absolute minimum with short distance communication requiring no more than a low cost ribbon cable. For longer distances or/and noisy environments, shielding is essential and cabling costs begin to increase.

The limitation on transmission distance has been partly overcome with RS-423-A which still uses an unbalanced line however only one end of the transmission system is grounded preventing low frequency ground loops. Each signal also has its own ground return line and prevents the accumulation of large ground currents in the return path as in the case of the EIA-232 standard. Cabling proves to be important particularly in reducing DC attenuation, normally for RS-423-A 24 AWG cable is specified. Crosstalk is kept to below 1 volt peak by limiting the slew rates, the maximum allowable rise time between the 10% and 90% points of the DC line condition can be no faster than 15 µs. This slower rise time than say for EIA-232, which at 20 kbps would be 2 µs, reduces the crosstalk and therefore longer distances can be achieved before the same level of crosstalk is experienced.

2.1.2 Disadvantages of single ended transmission

The main disadvantage of the single ended solution is its poor noise immunity. Because the ground wire forms part of the system, any transient voltage or shifts in voltage potential may be induced (from nearby high frequency logic or high current power circuits), leading to signal degradation ultimately leading to false receiver triggering. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the input switching threshold of the receiver device, thus increasing susceptibility to noise.

Cross talk is also a major concern especially at high frequencies. Cross talk is generated from both capacitive and inductive coupling. Capacitive coupling tends to be more severe at higher signal frequencies as capacitive reactance decreases. The impedance and termination of the coupled line determines whether the electric or the magnetic coupling is dominant. If the impedance of the line is high the capacitive pickup is large. Alternatively, if the line impedance is low, the series impedance as seen by the induced voltage is low, allowing large induced currents to flow.

These problems will normally limit the distance and speed of reliable operation for a single ended link.

Cross talk can be reduced by;

i. **Limiting the slew-rate of signals so that they do not cause cross talk to be induced onto other lines**

ii. **Limiting the line length.**

iii. **Shielding the signal conductor.**

While the common-mode noise could be reduced by:-

i. **Isolating the signal ground from power conductors (e.g. keep signal grounds separated as far as possible from power grounds).**

ii. **Ground wires should be as low as impedance as possible.**

iii. **Using star ground system configurations.**

2.2 EIA-232/TIA-232-E Industry Standard for Data Transmission

This sub-section on EIA/TIA-232, or RS-232 as it has been known in the past, will discuss the electrical aspects of the standard, i.e. the physical layer. Initially we will discuss the latest developments of the 'E' revision upgrade and then cover Texas Instruments' latest products conforming to this standard. However the reader should note the products under discussion in this section are application specific to the 9-pin DB9 Personal Computer DTE serial interface which is effectively a sub-set of the full EIA-232 standard. As a semiconductor manufacturer we find the majority of EIA-232 applications are moving to this interface. Due to the nature of the signals i.e. 5 receive and 3 transmit lines the older established EIA-232 products no longer provide an optimum solution. This interface is now driving the need for single chip EIA-232 solutions. Additional features such as single supply operation, increased ESD protection, power down modes have moved from the desirable features to the essential features of today's interface. In the later half of this section we will discuss the DB9 interface and Texas Instruments' products designed specifically for this application.

Looking at the DB9 interface one step back into the digital system, there is in most cases a UART or ACE (asynchronous communication element). The ACE provides the parallel to serial conversion and the necessary start/stop bits, parity bit generation and checking for error free data transmission. TI manufactures a number of ACEs, the most advanced being the TL16C552. This integrates two serial ports with FIFO buffers together with a PC parallel port. Although not specifically covered in this section a selection guide on ACEs is included towards the rear of this section.

2.2.1 Reliability Data

System designers have long been aware the mean-time-between-failure (MTBF) for most systems is limited by the reliability of the line interface circuitry. This is mainly due to the shear power dissipation of such line circuits. The older devices such as the SN75188 quad driver ran at quite high temperatures with obvious degradation on reliability. For today's products the use of low power bipolar and more recently BiCMOS technologies significantly reduces operating temperatures while maintaining the robustness associated with bipolar designs providing for a more reliable interface. This is show by reliability data collected on Texas Instruments' products.

Life test data collected on a range of EIA-232 devices yielded a failure rate of 1.65 FITS (failures per 10^9 device hours). This was at an ambient temperature of 55°C (to an upper confidence level of 60% and assumes an activation energy of 0.96 eV).

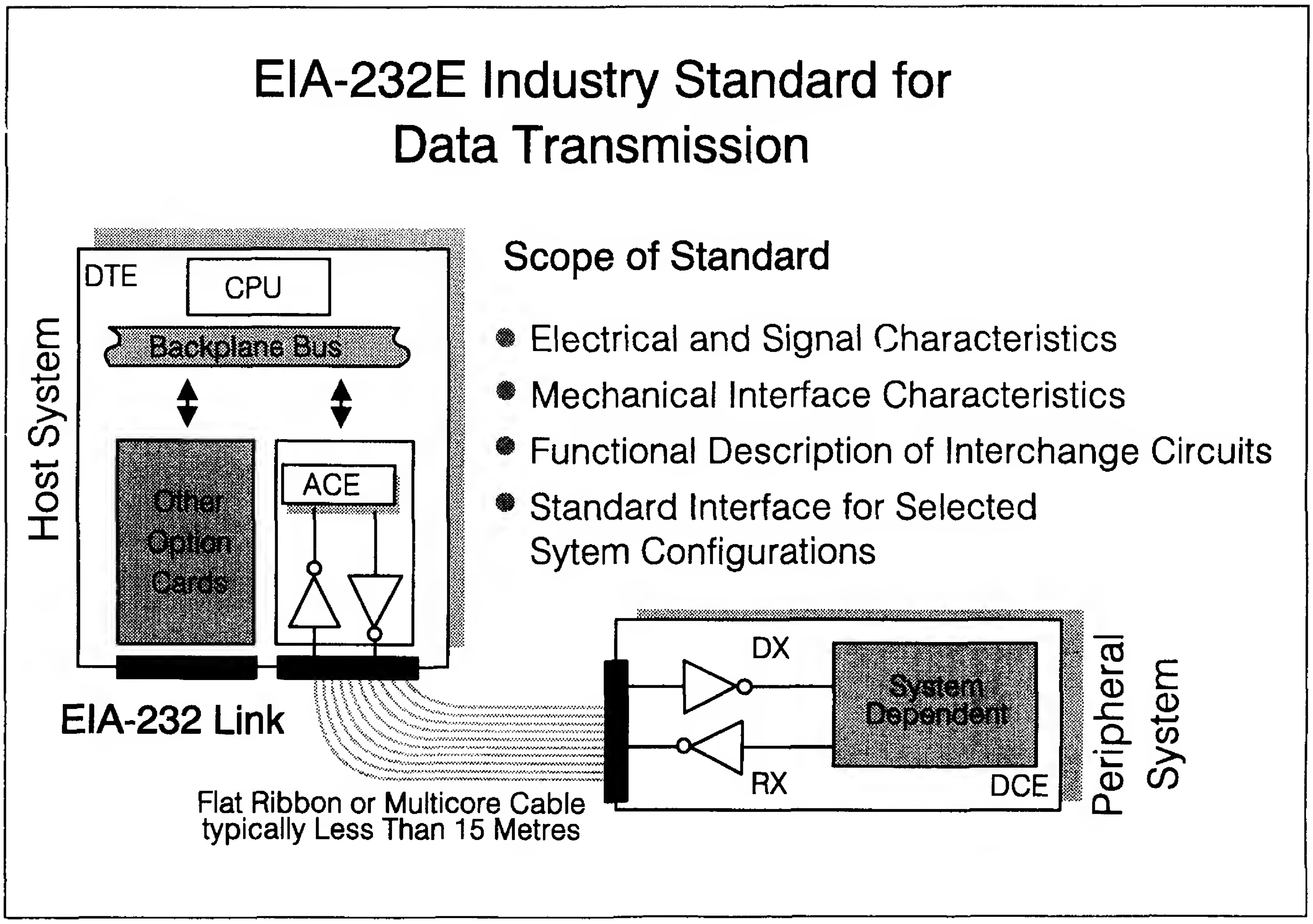
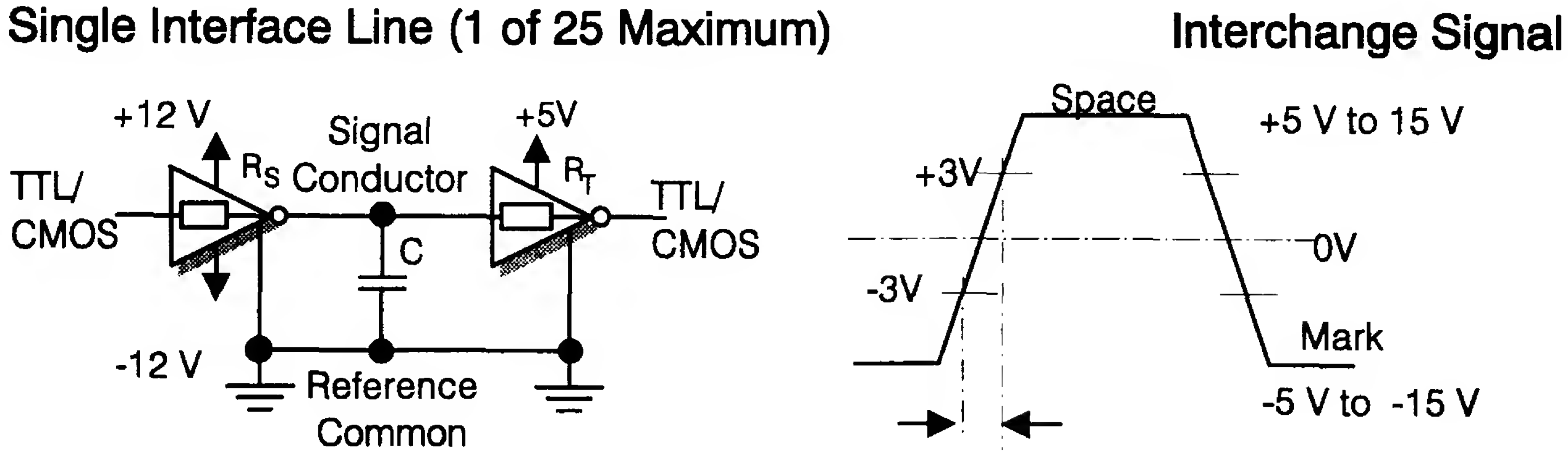

EIA-232E Industry Standard for
Data Transmission
Scope of Standard
● Electrical and Signal Characteristics
● Mechanical Interface Characteristics
● Functional Description of Interchange Circuits
● Standard Interface for Selected Sytem Configurations
Host System
DTE
CPU
Backplane Bus
Other Option Cards
ACE
EIA-232 Link
Flat Ribbon or Multicore Cable typically Less Than 15 Metres
DX
RX
System Dependent
DCE
Peripheral System

Figure 4.9 - EIA-232-E Industry Standard for Data Transmission

The Electronic Industries Association (EIA) introduced the RS-232 standard in 1962 in an attempt to standardise the interface between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE). The DTE comprises the data source, data sink or both. The DCE provides the functions to establish, maintain and terminate a connection, and to code/decode the signals between the DTE and the data channel. Although emphasis was then placed on interfacing between a modem unit and data terminal equipment, other applications were quick to adopt the EIA-232 standard. The growing use of the PC (personal computer) quickly ensured that EIA-232 became the industry standard for all low-cost serial interfaces between the DTE and peripheral. The mouse, plotter, printer, scanner, digitiser, and tracker-ball, in addition to the external modem unit, are all examples of peripherals that connect to an EIA-232 port. Using a common standard allows widespread compatibility plus a reliable method for interconnecting a PC to peripheral functions.

EIA - 232E Electrical Specifications



- Receiver Input Impedance, R_T = 3 kΩ to 7 kΩ
- Driver Power-off Impedance, R_S > 300 Ω
- Load Capacitance < 2500 pF Includes Receiver Input
- Tx Rise/Time Fall within Transition Region;

1 ms	Below 40 bps
4% of Unit Interval	40 to 20 kbps

- Slew Rate: 30 V/μs max

Figure 4.10 - EIA-232-E Electrical Specifications

The EIA RS-232-C standard, revised in 1969, was superseded by EIA-232-D (1986), and recently has been once again superseded by EIA/TIA-232-E which brings it in-line with CCITT V24, V.28 and ISO IS2110. (TIA refers to the Telecommunication Industry Association). The latest revision includes an update on the rise time to unit interval ratio and reverses the changes made by the 'D' revision, see figure 4.10. Although an older standard, with problems like high-noise susceptibility, low data rates and very limited transmission length, EIA-232 fulfils a vital need as a low cost communication system. Consequently new products are being developed at a faster rate than ever.

2.3 EIA-232 Specification

The standard sets out to ensure:

i. Compatible voltage and signal levels

ii. Common pin wiring configurations

iii. A minimum amount of control information between the DTE and DCE.

It accomplishes this by incorporating the following areas in the standard:

Electrical and Signal Characteristics

Electrical and signal characteristics of the transmitted data in terms of signal voltage levels, impedance's, and rates of change.

Mechanical Interface Characteristics

Mechanical interface characteristics defined as a 25-way "D" connector, with dimensions and pin assignments specified in the standard. Although the standard only specifies a 25-pin D-type connector, most laptop and desktop PCs, today use a 9-pin "DB9S" connector shown in figure 4.14. The reader should note the DCE equipment connector is male for the connector housing and female for the connection pins. Like wise the DTE connector is a female housing with male connection pins.

Handshake Information

A functional description of the interchange circuit enables a fully interlocked handshake exchange of data between equipment's at opposite ends of the communication channel. However, V24 defines many more signal functions than RS-232, but those that are common are compatible. Twenty two of the twenty five connector pins have designated functions, although few, if any, practical implementations use all of them. The most commonly used signals are also shown in figure 4.14.

It is worth noting that for applications which use the 25-pin D-type connector there is often a problem in communication due to different handshaking signals employed by each system.

2.3.1 EIA-232-E Electrical Specifications

All EIA-232 circuits carry bipolar voltage signals with the voltage at the connector pins not to exceed ±25 V. Any pin must be able to withstand short circuit to any other pin without sustaining permanent damage. Each line should have a minimum load of 3 kΩ and maximum load of 7 kΩ which is usually part of the receiver circuit. A logic '0' is represent by a driven voltage of between +5 V and +15 V and a logic '1' of between -5 V and -15 V. At the receiving end a voltage of between +3 V and +15 V represents a '0' and a voltage of between -3 V and -15 V represents a '1'. Voltages between ±3 V are undefined and lie in the transition region. This effectively gives a 2 volt minimum noise margin at the receiver.

The maximum cable length was originally defined in RS-232C as 15 metres, however this has been revised in EIA-232-D and EIA/TIA-232-E and is now more correctly specified as a maximum capacitive load of 2500 pF. This equates to around 15 to 20 metres line length depending on cable capacitance.

As mentioned in an earlier section, EIA-232 specifies a maximum slew rate of the signal at the output of the driver to be 30 V/µs. This limitation is concerned with the problem of cross talk between conductors in a multiconductor cable. The faster the transition edge the greater the cross talk. This restriction together with the fact of the driver and receiver using a common signal ground and the associated noise introduced by the ground current severely limits the maximum data throughput.

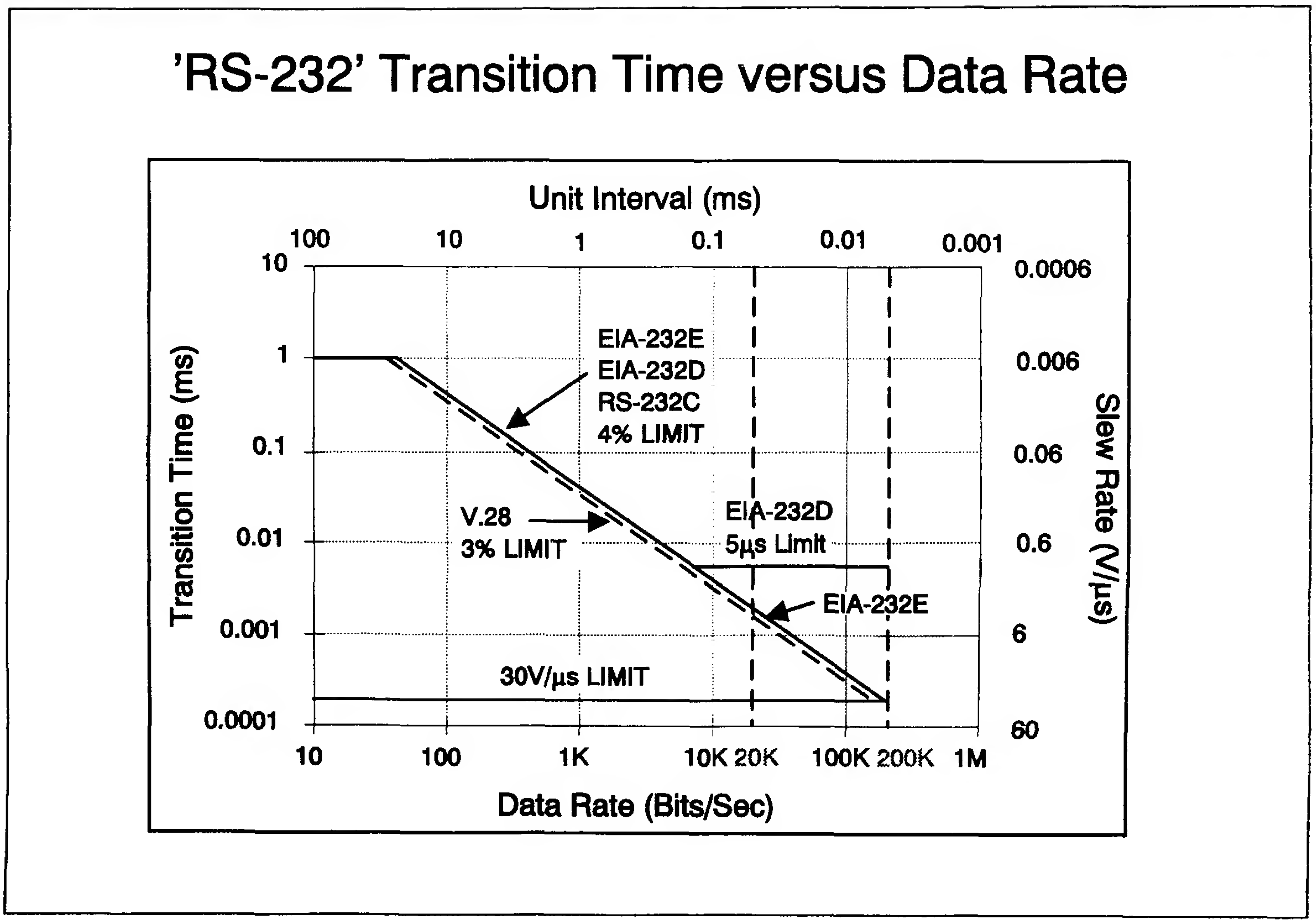


Figure 4.11 - 'RS-232' Transition Time versus Data Rate

For this reason the EIA-232 standard specifies a maximum data rate of 20 kbps. The standard also specifies the relationship between unit interval and rise time through the transition region (+3 V to -3 V) or t_T. This is the main difference between the 'E' and the 'D' revision. This is shown more clearly in figure 4.11. EIA-232-D up to 8 kbps specified the relationship between transition time and unit interval or bit time t_b to be 4% maximum. Above 8 kbps this was relaxed to 5 µs maximum independent of the data rate. Both the 'C' and the 'E' revision specify the ratio of t_T/t_b to be 4% all the way up to 20 kbps. One can extrapolate this further, using the 4% figure and with the maximum slew rate of 30 V/µs, the maximum achievable data rate is 200 kbps however practically this is limited to around 120 kbps. A number of software programs operate at transfer rates of 116 kbps. Furthermore over longer line lengths the maximum drive current or short circuit current of the line driver becomes the dominant feature on data rate as against the 30 V/µs slew rate. As the line length increases the load capacitance also increases requiring more current to maintain the same transition time. The curves shown in figure 4.12 indicate the drive current required to maintain the 4% relationship at different data rates. In today's low power systems, this level of output current is not sustainable at above say 20 kbps. In practice the line length is usually limited to around 4 metres for the higher data rates. Most drivers can handle the higher transmission rates over this line length without seriously compromising supply current.

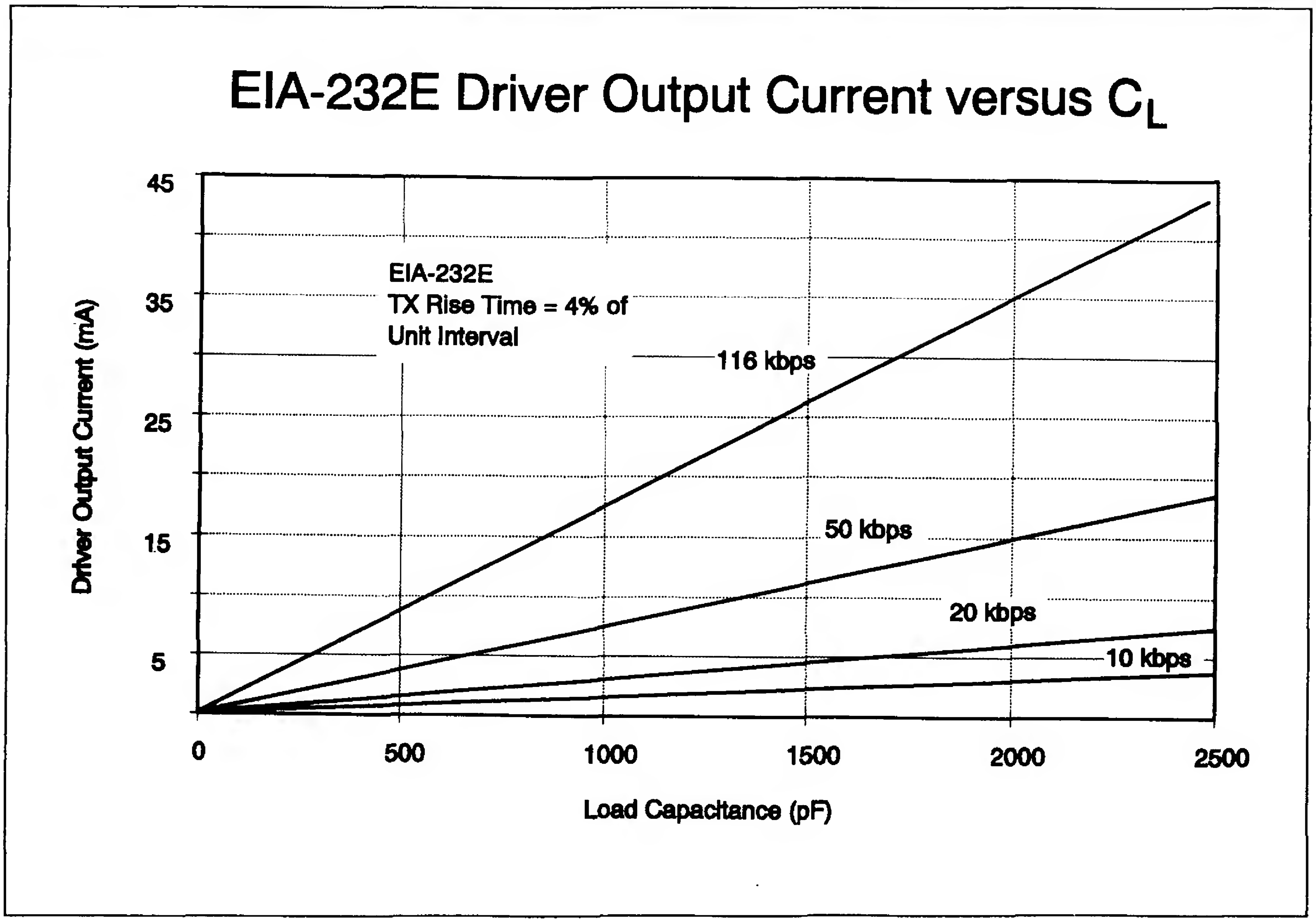


Figure 4.12 - EIA-232-E Driver Output Current versus C_L

The curves shown in figure 4.12 were generated using the following equation which is an approximate equation relating transition time t_T, line capacitance C_l, receiver input impedance R_i, driver short circuit current I_0, and the initial and final line voltage (-3 V and +3 V) of the transition region, V_i and V_f respectively,

$$t_T = R_i \times C_l \times \ln\left[\frac{|R_i \times I_o| + |V_f|}{|R_i \times I_o| - |V_i|}\right]$$

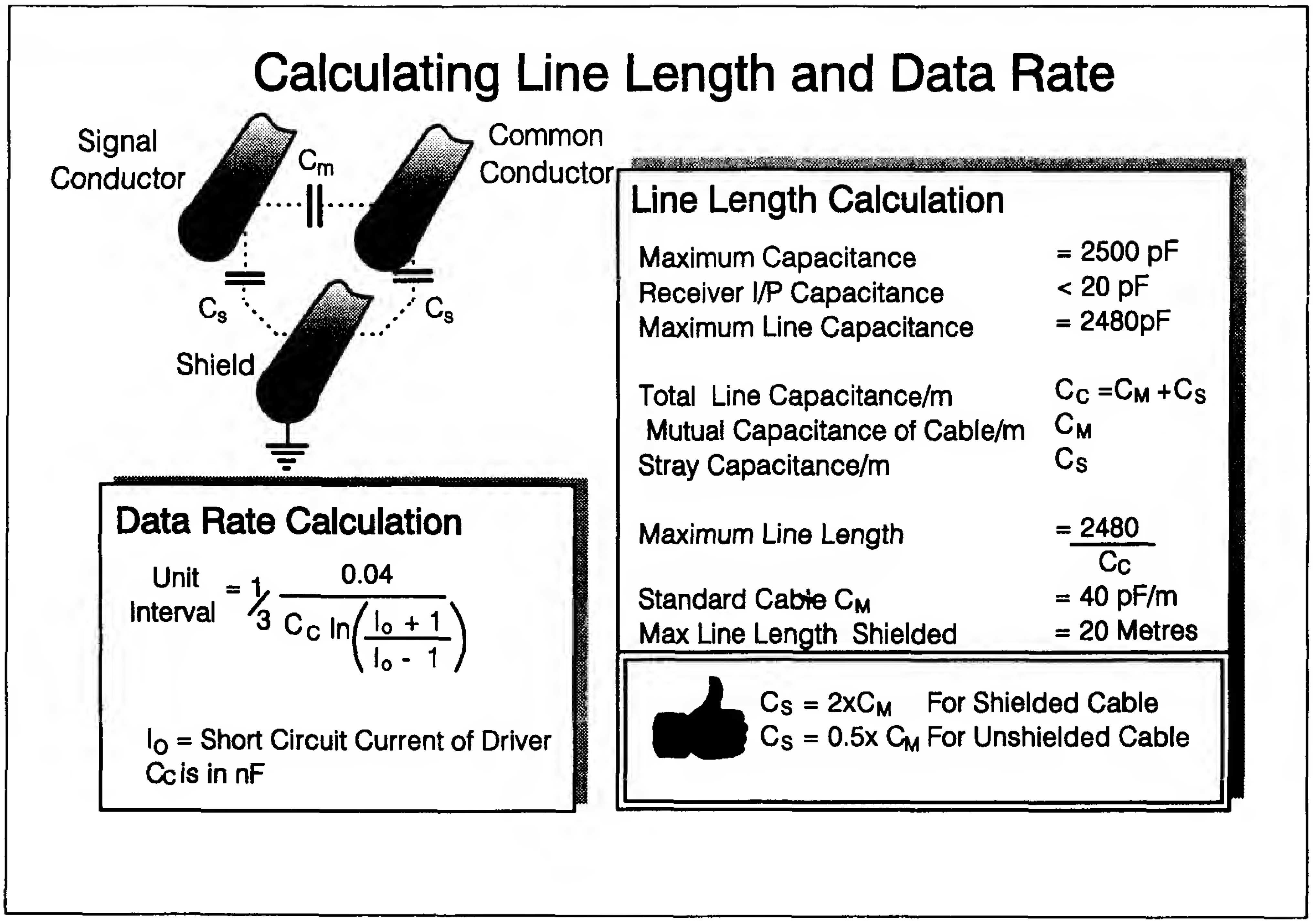
Turning this equation around with respect to C_l, and cancelling R_i, V_i and V_f we get:

$$C_l = \frac{1}{3} \times \frac{t_T}{\ln\left[\frac{I_o + 1}{I_o - 1}\right]} \text{ nF}$$

The voltage levels, V_f and V_i, used in this equation are the extremes of the transition region. Assuming a typical driver short circuit current of 20 mA and a receiver input resistance of 5 kΩ, the typical time taken to pass through the transition region would be :-

$$t_T = 300 \times C_l \qquad \text{seconds.}$$

This equation can be manipulated further to gain a relationship of unit interval with line length in terms of load capacitance and short circuit driver current. The equation in figure 4.13 assumes conformance to the 4% rule.



Calculating Line Length and Data Rate

Data Rate Calculation

$$\text{Unit Interval} = \frac{1}{3}\,\frac{0.04}{C_C \ln\left(\frac{I_o + 1}{I_o - 1}\right)}$$

I_O = Short Circuit Current of Driver
C_C is in nF

Line Length Calculation

Maximum Capacitance	= 2500 pF
Receiver I/P Capacitance	< 20 pF
Maximum Line Capacitance	= 2480pF
Total Line Capacitance/m	$C_C = C_M + C_S$
Mutual Capacitance of Cable/m	C_M
Stray Capacitance/m	C_S
Maximum Line Length	$= \dfrac{2480}{C_C}$
Standard Cable C_M	= 40 pF/m
Max Line Length Shielded	= 20 Metres

$C_S = 2xC_M$ For Shielded Cable
$C_S = 0.5x\ C_M$ For Unshielded Cable

Figure 4.13 - Calculating Line Length and Data Rate

2.3.2 Calculating maximum line length

So far we have discussed line length in terms of load capacitance. For practical purposes we must now consider turning this value for load capacitance into true line length. The standard states a maximum line capacitance of 2500 pF. The input capacitance of a receiver is say 20 pF which leaves 2480 pF as the maximum line capacitance.

We must now consider the type of cable to be used. Standard EIA-232 cable as supplied by a number of manufacturers has a mutual capacitance of approximately 40 pF per metre. In addition to this we must add the stray capacitance. Stray capacitance varies considerably on whether the line is shielded. For non shielded cable the stray capacitance is approximately half the mutual capacitance, for shielded cable it is double the mutual capacitance. As can be seen from figure 4.13, for shielded cable the maximum line length is 20 metres, with unshielded cable it is over 40 metres.

2.3.3 The DB9S Connector

As mentioned earlier today's notebook and laptop PCs, with their quest for reduced size, no longer use the standard 25-way D-type connector detailed in the standard but have substituted it for a 9-way D-type. This is commonly known as the DB9S connector. Like the 25-way, the DCE equipment connector is a male outer casing with female connection pins, and the DTE is a female outer casing with male connecting pins.

As the interface is now made up of only nine pins the handshaking lines have been reduced accordingly but still are sufficient for most applications. Figure 4.14 shows the pins assignments for the interconnect cable into the DTE connector. An explanation of the function of each signal is given below:

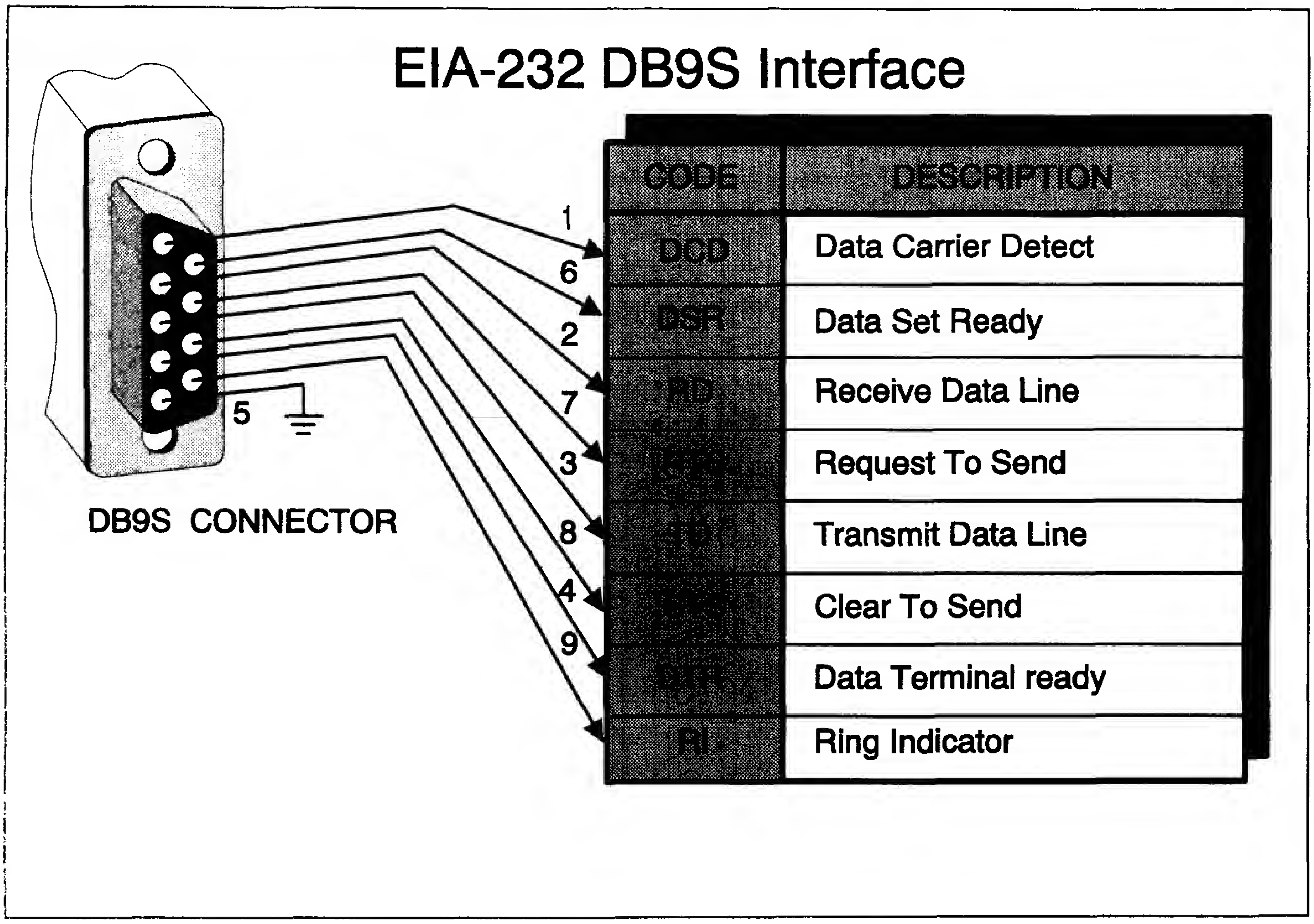

EIA-232 DB9S Interface
DB9S CONNECTOR
CODE
DESCRIPTION
1
DCD
Data Carrier Detect
6
DSR
Data Set Ready
2
RD
Receive Data Line
7
RTS
Request To Send
3
TD
Transmit Data Line
8
CTS
Clear To Send
4
DTR
Data Terminal ready
9
RI
Ring Indicator
5

Figure 4.14 - EIA-232 DB9S Interface

Data Carrier Detect (DCD) - Received Line Signal Detector

The ON condition on this signal line as sent by the DCE informs the DTE that it is receiving a carrier signal which meets its suitability criteria from the remote DCE. In modems, this circuit is held on as long as it is receiving a signal that can be recognised as a carrier. On half duplex channels, DCD is held off when RTS is in the on condition.

Data Set Ready (DSR)

This is a signal turned on by the DCE to indicate to the DTE that it is connected to the line.

Receive Data Line (RD)

The signals on the RD line are in serial form . When the DCD signal is in the off condition the RD line must be held in the Mark state.

Request to Send (RTS)

This signal is turned on by the DTE to indicate it is now ready to transmit data. The DCE must then prepare to receive data. In half duplex operation, it also inhibits the receive mode. After some delay the DCE will turn the CTS line on to inform the DTE it is ready to receive data. Once communication is over and no more data is transmitted by the DTE, RTS is then turned from on to off by the DTE. After a brief time delay to ensure all data has been received that was transmitted, the DCE turns CTS off.

Transmit Data Line (TD)

The signals on this circuit are transmitted serially from DTE to DCE. When no data is being transmitted the signal line is held in the Mark state. For data to be transmitted, DSR, DTR, RTS and CTS must all be in the on state.

Clear to Send (CTS)

This signal is turned on by the DCE to indicate to the DTE that it is ready to receive data. CTS is turned on in response to simultaneous on condition of the RTS, DSR and DTR signals.

Data terminal Ready (DTR)

This in conjunction with DSR indicate equipment readiness. DTR is turned on by the DTE to indicate to the DCE it is ready to receive or transmit data. DTE must be in the on condition before the DCE can turn on DSR. When DTR is turned off by the DTE, the DCE is removed from the communication channel following the completion of transmission.

Ring Indicator (RI)

The ring indicator is turned on by the DCE while ringing is being received and is a term left over from the use of the standard in telephone line modem applications. Primarily used in auto-answer systems.

Signal Ground (pin 5)

This is the ground which provides the common ground reference for all the interchange circuits and is separate from the protective ground. The protective ground is electrically bonded to the equipment frame and is usually directly connected to the external ground. Any static discharges are then routed directly to ground without affecting the signal lines.

While all these pins are assigned, once again not all equipment uses every pin. Consider the mouse which can use as few as 4 lines, Signal ground, RI, TD and RD. Most equipment does however utilise a minimum of RTS, DTR, TD, RD, CTS and DSR.

Also of note is the usage of the DTE interface. The majority of equipment uses this interface and makes use of the null modem as a means of communication between DTEs. The null modem makes use of feeding back the RTS signal to the CTS line on each interface, Figure 4.15 details the connections for implementing a full null modem for the DB9S connector.

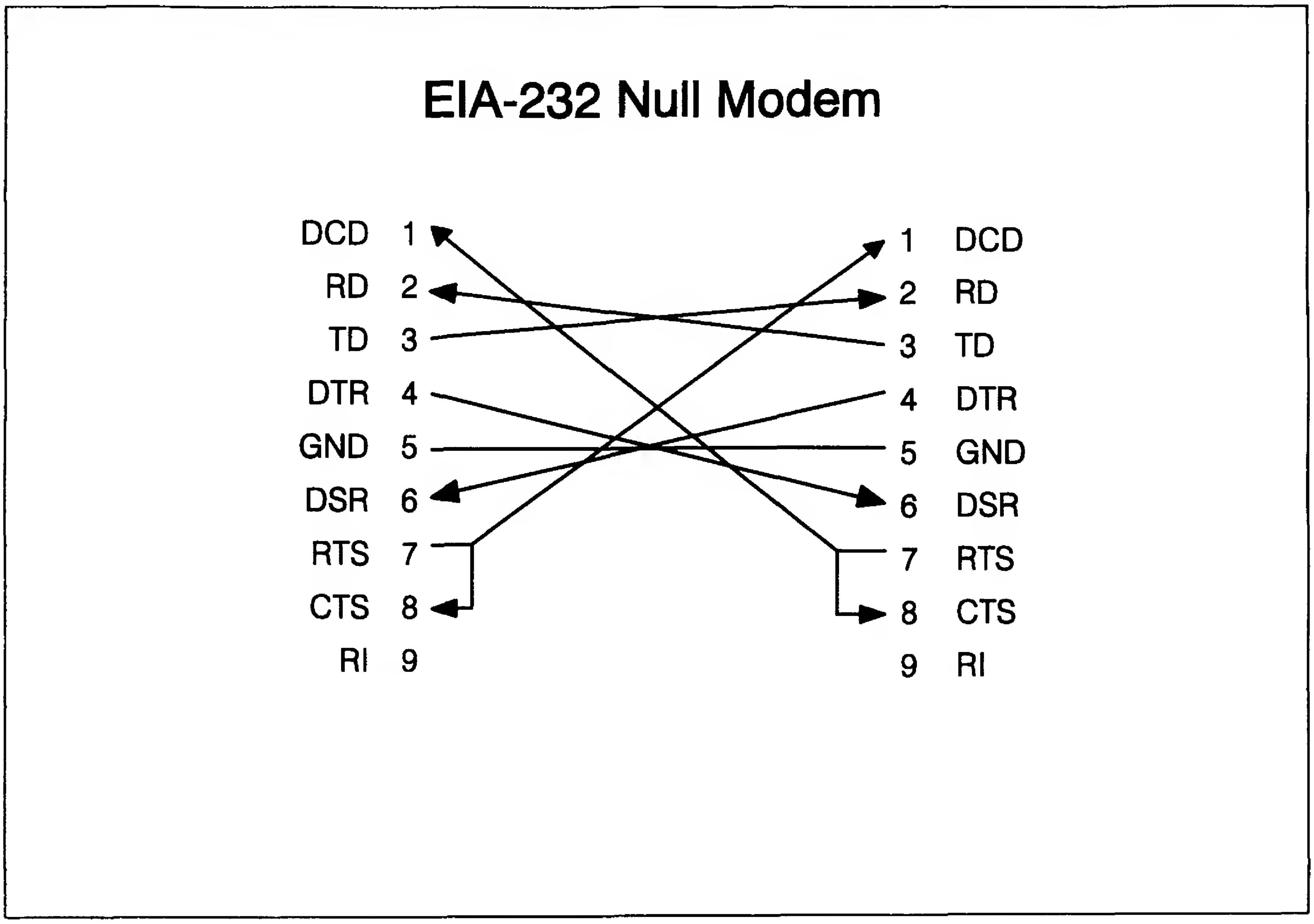


Figure 4.15 - EIA-232 Null Modem

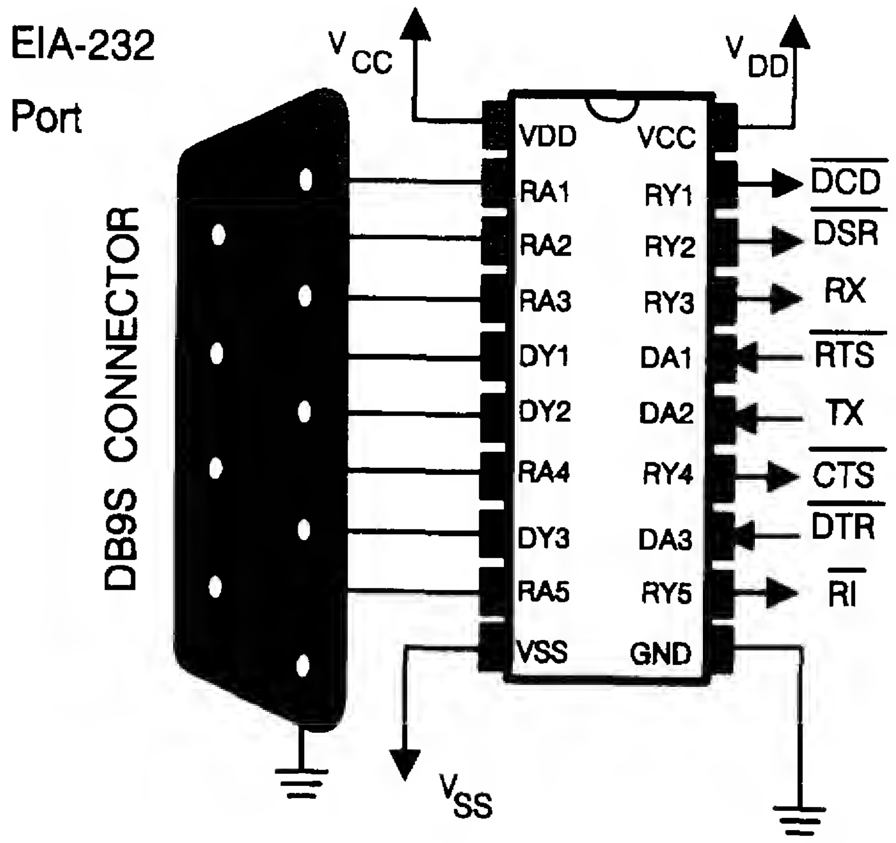
2.4 SN75C185: Optimised PC Interface

If we study the DB9S DTE interface further we see there are 3 transmit lines and 5 receive lines. This is an awkward combination for the standard EIA-232 IC configurations in use today. Consider the ubiquitous SN75188 and SN75189 quad drivers and receivers. To implement this interface would require 3 ICs, one '188 and two '189s. Equal combinations of drivers such as the triple driver/receiver of the SN75C1406 still requires two chips to implement the interface.

For this reason TI has developed the SN75C185. By providing the exact combinations of driving and receiving elements, along with the necessary passive components, a highly optimised solution can be provided – the SN75C185 is just that. The SN75C185 integrates three drivers and five receivers and includes the necessary capacitors for driver slew-rate limit (30 V/µs) and receiver filter implementation, all in a single 20-pin package

The designer's dilemma is eased further by the use of a flow-through pin out architecture, see figure 4.16. By aligning one side of the SN75C185 with the pins of the DB9S connector and the other to industry standard ACEs or UARTs, printed circuit board (PCB) layout can be greatly simplified.

SN75C185; Optimised PC Interface


EIA-232
Port
DB9S CONNECTOR
V_{CC}
V_{DD}
VDD
VCC
RA1
RY1
RA2
RY2
RA3
RY3
DY1
DA1
DY2
DA2
RA4
RY4
DY3
DA3
RA5
RY5
VSS
GND
$\overline{DCD}$
$\overline{DSR}$
RX
$\overline{RTS}$
TX
$\overline{CTS}$
$\overline{DTR}$
$\overline{RI}$
V_{SS}

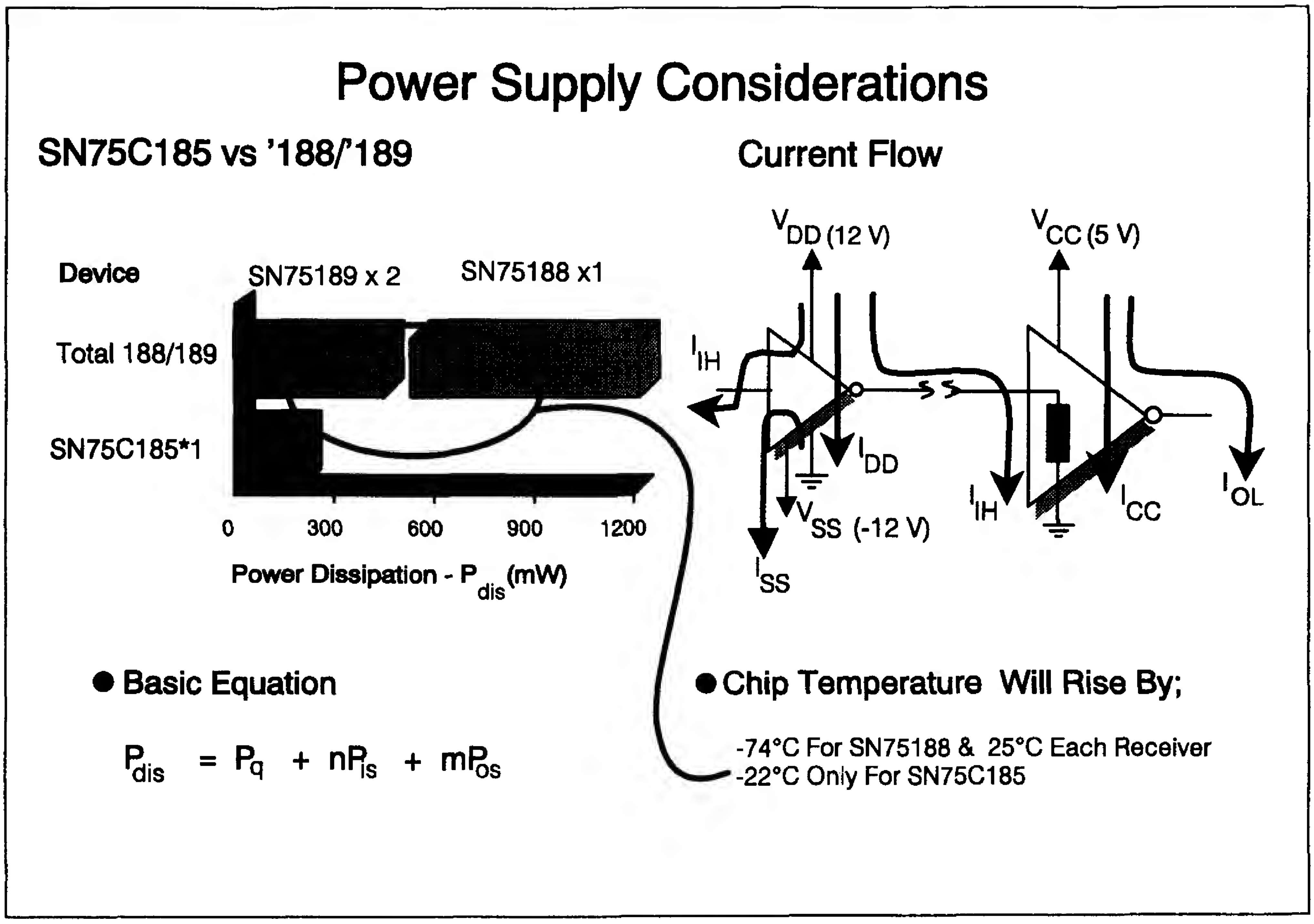
- Contains Five Receivers and Three Drivers - Replaces 2x SN75189 and 1xSN75188 = 35% Board Saving
- Easy Interface Between ACE and Serial Port Connector (Flow Through Pin Out)
- Less than 8 mW Power Consumption

Figure 4.16 - SN75C185; Optimised PC Interface

2.4.1 Low Power as Well

In common with all of Texas Instruments BiMOS products, these devices combine the benefits of Bipolar's drive capability and robustness along with the low-power consumption of CMOS. This power saving, when compared to the alternatives is calculated in the following pages and is illustrated graphically in figure 4.17.

Available in either a single 20-pin, wide-bodied SO pack or DIP pack, the SN75C185 offers designers greater than 25% saving in board space, compared to alternate solutions.



Power Supply Considerations

SN75C185 vs '188/'189

Current Flow

- **Basic Equation**

$$P_{dis} = P_q + nP_{is} + mP_{os}$$

- **Chip Temperature Will Rise By;**

-74°C For SN75188 & 25°C Each Receiver
-22°C Only For SN75C185

Figure 4.17 - Power Supply Considerations

2.4.2 SN75C185; Power Considerations

System power consumption is often considered very late in the design cycle. Of even more concern is that the power consumption of the interface circuitry, being the least attractive circuit to design, is often totally overlooked. The consequences of this can be catastrophic especially when using devices in confined spaces. These areas will normally have very poor air circulation, causing the ambient temperature of the whole system to increase.

These types of problems are particularly difficult to diagnose as failure can often be intermittent as devices pass into and out of thermal shutdown.

For these reasons, low quiescent-power devices are becoming a necessity for modern applications. As digital technologies advance, their power consumption decreases, making the interface circuits the limiting factor as far as system power consumption is concerned.

2.4.3 Interface Power Consumption Calculations

Before the availability of the SN75C185 common implementations of EIA-232 require one quad-driver package and two quad-receiver packages; in the driver chip, one device is redundant while in the receiver chips, three devices are redundant. These devices would, however, still be taking their quiescent current and hence wasting power. In order to provide the interface signals, three integrated circuits were required while only two-thirds of the capability was being used. The calculations below demonstrate this difference.

When comparing the 'C185 solution to that provided by the SN75188 and SN75189 devices, the power saving is enormous.

Both implementations require three supply voltages; a 5 V and ±12 V supplies. The power dissipated, P_{dis}, within each device is the quiescent power of the device, P_q, plus the power dissipated in the input stage, P_{is}, and the power dissipated in the output stage, P_{os}, (when it is driving the line).

Hence,

$$P_{dis} = P_q + nP_{is} + mP_{os}$$

Where n is the number of active input stages and m is the number of active output stages.

SN75188/SN75189 Combination

Using an SN75188 for the driver, the quiescent power consumption would be 576 mW. In addition to this the power dissipated in the input stage, P_{isd}:-

$$\begin{aligned} P_{isd} &= V_{CC} * I_{IL} \\ &= 12 * 1.6 \text{ mW} \\ &= 19.2 \text{ mW.} \end{aligned}$$

This is multiplied by four to take into account all four drivers, putting the fourth driver into a defined state so as to reduce any noise problems that could be introduced by leaving the input floating.

The power dissipated in the output stage, P_{osd}, is:

$$\begin{aligned} P_{osd} &= (V_{CC} - V_{OH})* \frac{V_{OH}}{R_L} \\ &= (12 - 9) * \frac{9}{3} \text{ mW} \\ &= 9 \text{ mW.} \end{aligned}$$

This figure will be multiplied by three to take into account the active three drivers driving the interface line. These sum up to give a total power dissipation of

$$\begin{aligned} P_{dis} &= 576 + 4 \times 19.2 + 3 \times 9 \text{ mW} \\ &= 680 \text{ mW.} \end{aligned}$$

The junction temperature of a DIP device would have risen by 74°C.

Using the SN75189 receivers, a quiescent power of 130 mW would be dissipated by each package. This would be multiplied by two to take into account both chips.

The power dissipated in the output stage has a similar equation to that of the driver.

$$\begin{aligned} P_{osr} &= V_{OL} * I_{OL} \\ &= 0.45 \times 10 \text{ mW} \\ &= 4.5 \text{ mW} \end{aligned}$$

This power dissipated is multiplied by five to take into account the five receivers being used. The input stage can also dissipate some power, but this power is not supplied by this part of the interface system. The power dissipated within the IC will however cause the junction temperature to rise.

$$P_{isr} = \frac{V_{OH(d)}^2}{R_L}$$

$$= \frac{9^2}{3} \quad mW$$

$$= 27 \text{ mW}$$

This power dissipation is then multiplied by five. The remaining receivers will require tying to a state where they will not be susceptible to noise. Tying them to the 5 V supply increases the power dissipation by a further 8.3 mW per receiver.

Assuming three receivers in one SN75189 are being used and two receivers in the other, the power dissipated for the first receiver is:

$$P_{dis} = 130 + 4 \text{ x } 27 + 3 \text{ x } 4.5 \quad mW$$

$$= 233 \text{ mW.}$$

The power dissipated in the second receiver is:-

$$P_{dis} = 130 + 4 \text{ x } 27 + 2 \text{ x } 4.5 \quad mW$$

$$= 210 \text{ mW.}$$

This raises the temperature of the first and second receiver by 25°C and 23°C, respectively.

The total power dissipated by the SN75188/189 combination is the sum of these three powers, equalling **1.12 W.**

Using the SN75C185

The power dissipation of the SN75C185 can be calculated in a similar manner. The quiescent- power consumption of the SN75C185 is equal to:-

$$P_q = V_{DD} * I_{DD} + V_{SS} * I_{SS} + V_{CC} \text{ x } I_{CC}$$

$$= 12 * 200 + -12 \text{ x } -200 + 5 \text{ x } 750 \quad \mu W$$

$$= 8.55 \text{ mW}$$

The power dissipated in the input stage of the driver is:-

$$P_{isd} = V_{DD} \text{ x } I_{IL}$$

$$= 12 \text{ x } 1 \quad \mu W$$

$$= 12 \text{ } \mu W.$$

This is multiplied by three to take into account all of the drivers.

The power dissipated in the output stage of the driver, P_{osd}, is:

$$P_{osd} = (V_{DD} - V_{OH}) \times \frac{V_{OH}}{R_L}$$

$$= (12 - 10) \times \frac{10}{3} \quad mW$$

$$= 6.67 \text{ mW.}$$

This is multiplied by three to take into account the three drivers driving the interface line, giving a power dissipation of 20 mW.

The power dissipated in the output stage of the receiver has a similar equation to that of the driver, so:

$$\begin{aligned} P_{osr} &= V_{OL} \times I_{OL} \\ &= 0.4 \times 3.2 \quad \text{mW} \\ &= 1.28 \text{ mW} \end{aligned}$$

This value is multiplied by five giving a total of 6.4 mW of power dissipated in the receiver's output stages. The input stage will also dissipate some power, but this power will not be supplied by this part of the interface system. The power dissipated within the chip will however cause the junction temperature to rise.

The power dissipated in the input stage, P_{isr}, equals:

$$\begin{aligned} P_{isr} &= \frac{V_{OH(d)}^2}{R_L} \\ &= \frac{10^2}{3} \quad \text{mW} \\ &= 33.3 \text{ mW} \end{aligned}$$

This power dissipation will also require multiplying by five. Giving a total input power dissipation of 167 mW.

Summing all the power contributors the total power dissipation is given by;

$$\begin{aligned} P_{dis} &= P_q + 3P_{isd} + 3P_{osd} + 5P_{isr} + 5P_{osr} \\ &= 8.55 + 3 \times 12 \times 10\text{-}3 + 3 \times 6.67 + 5 \times 33.3 + 5 \times 1.28 \quad \text{mW} \\ &= 201 \text{ mW}. \end{aligned}$$

The total power dissipated by the SN75C185 is **201 mW**

This is represents a tremendous power saving, especially when considering that the line is still being driven. The temperature rise within the SN75C185 would only be 22°C, enabling it to operate more reliably and with higher ambient temperatures.

2.4.4 On Chip Slew Rate Limiting

The EIA-232-E standard specifies a maximum slew rate through the transition region of **30 V/µs**. Relating this to capacitance and current only 100 µA of output current into 30 pF load capacitance is needed to exceed the slew-rate limit. All devices are capable of supplying more than 5 mA. Therefore if the slew rate limit is not to be exceeded, the switching speed of the driver's output stage needs to be reduced. An established solution is to place loading capacitors on the output of the driver. The value of the loading capacitor required will depend upon the line length, but it is generally in the order of 330 pF. The effect of this capacitor is to cause the output transistors to saturate, causing it to short circuit current limit, thus preventing fast switching edges.

There are some major problems with this established process; one being the variance in current at which the output short-circuit current limit operates, especially when taking temperature changes into consideration. Again the value of capacitance placed on the line will depend upon the driver's output short-circuit capability as well as line length. For example a device capable of sourcing 10 mA will need a total capacitance of 330 pF placed on its output to meet the 30 V/µs slew rate limit, while placing this value across a device capable of sourcing 4 mA will have its slew rate limited to less than 12 V/µs.

Another problem encountered is the increase in power dissipation through the output stage. The output voltage of the driver will normally be close to one supply rail, so when it tries to switch to the other, the active transistor will have almost all of the supply voltages across it. The extra external capacitor will clamp the driver's voltage close to the supply voltage causing the output transistor to source large amounts of current. The combination of a large source current and large voltage cause it to dissipate large amounts of power. Operating at these prolonged bursts of high current will ultimately increase the chip temperature which in turn can affect the long-term life of the device. Bipolar technologies are normally much better able to withstand such effects

A better solution, and that employed by the drivers in the SN75C185, is to place the slew-rate limiting within the chip itself. Using similar techniques to those employed for slew-rate-limited operational amplifiers, the slew rate of line drivers can also be limited. Using the Miller capacitance multiplying effect, the slew rate of the driver can be slowed down. The on-chip capacitors are normally in the order of 5 pF, while the currents driving the on-chip capacitor are the order of micro amperes, thus reducing power consumption within the device. The biasing current to the output transistors is unaffected by this technique and will be more than sufficient to drive the 3 kΩ load as offered by the receiver.

2.4.5 Internal Noise Filtering

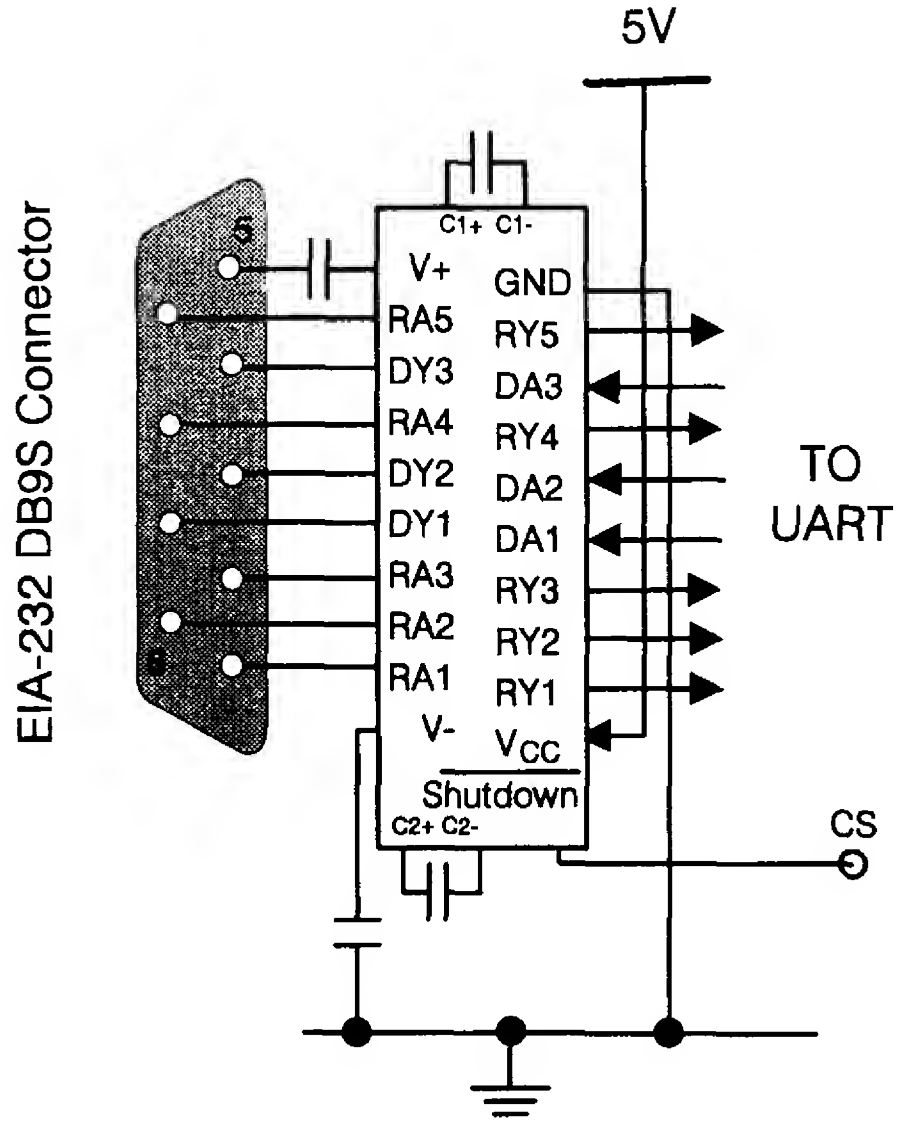
The standard states a maximum line cable capacitance of 2500 pF, which corresponds to an approximate line length of 20 metres. As the interface line gets longer, it becomes more susceptible to noise pick-up from the surrounding environment. This pick-up is due in part to the inductive nature of the line. As the signal switches, a rapidly changing magnetic field induces noise currents into the line, thereby corrupting signal data. The level and cause of this noise will dictate the nature of solutions or precautions that should be taken.

For operation at high data rates, the use of a differential line might be the best solution. If however, a low cost and simple single-ended solution is required then standard EIA-232 devices can be modified to give noise protection. This is achieved by slowing down the response of the receiver's input stage, making them too slow to respond to fast switching noise pulses. Even small levels of input noise can falsely trigger the receiver. The maximum data rate specified in the standard is 20 kbps, corresponding to a minimum pulse period of 100 µs. Therefore in normal applications, most devices are far faster than the specification requires.

To slow down older bipolar receivers such as SN75189s, a capacitor, C_C, needed to be placed on each of its response control pins. This means an additional four capacitors per device, which can be awkward and costly. The effect of this response control capacitor is to set up a low-pass filter on the receiver's input. In order to provide large pulse rejection, the capacitor needs to be quite large. Furthermore, the filter response is asymmetric, affording protection against positive noise voltage spikes only, negative spikes are unaffected, and will tend to attenuate rather than reject short noise pulses.

Receivers in the SN75C185 integrate on-chip filtering which reject fast transient noise pulses. The on-chip filters are more precise than filters implemented using external passives. Consequently the receiver response is unaffected. These filters are totally symmetrical, offering protection against both positive and negative noise pulses and with the ability to reject rather than attenuate short noise pulses. To approach the level of filtering offered by the 'C185 receivers the standard '188 type receivers require much larger capacitors and even then fall well short of filtering requirements.

SN75LBC187; Optimised for Portables



- Switched Capacitor Converter
  - Generates +/- 8.5V Supplies from 5V.
  - Only 0.1 µF External Capacitors
- Shutdown Mode
  - Icc = 10 µA (Max)
- High Data Rate Capability
  - >116 kbps with 2500 pF Load
- Robust Bipolar I/O Structures
  - ±30 V Receiver Input Range
  - 6 KV ESD Protection
- SSOP Packaging

Figure 4.18 - SN75LBC187; Optimised for portables

2.5 SN75LBC187; Optimised for Portables

The SN75C185 is the ideal choice for computer applications where the bipolar supplies required by EIA-232 are available within a computer system. Most desk top computers generate ±12 volt supplies for powering the internal disk drive. However for portable equipment, e.g. laptops, notebooks, hand held measuring equipment, the EIA-232 interface may be the sole user of a negative supply. The cost of implementing a switch mode supply, using inductive switching regulators, to generate the negative supply can make this option unattractive. Switch mode supplies also have the draw back of increasing the EMI emissions, a factor becoming an increasingly important design constraint. Integrating a switch mode power supply on silicon would reduce the emissions, and has been the dream of semiconductor manufacturers, but thus far no one has yet managed to integrate the inductor.

An alternative way, and the basis of modern technology charge pumps, is to make switching regulators using capacitors. In essence they operate by applying charge to a capacitor via an input voltage and then adding, subtracting or inverting the voltage on the positive or negative voltage terminals. This charge is transferred into a holding reservoir capacitor that is then used to supply the output voltages. Furthermore such a scheme can be integrated into silicon. Using a network of capacitors both voltage doublers and invertors can be made.

The SN75LBC187 integrates the charge pump on the same IC as the EIA-232 drivers and receivers. It is fabricated in Texas Instruments' proprietary LinBiCMOS™ technology and contains three independent drivers and 5 independent receivers together with the switched-capacitor voltage converter. The SN75LBC187 provides a single 5 V supply interface between the asynchronous communications element (ACE or UART) and the serial port connector of the data terminal equipment (DTE). This device has been designed to conform to standards EIA/TIA-232-E-1986 and EIA/TIA-562 and CCITT recommendation V.28.

The switched-capacitor voltage converter of the SN75LBC187 uses four small (0.2 µF) external capacitors to generate the positive and negative voltages required by EIA-232 line drivers from a single 5 V logic supply input. Like the SN75C185 the drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without sustaining damage. Furthermore the 'LBC187 is guaranteed to withstand up to 6KV ESD on any of its pins making it Texas Instruments' most rugged EIA-232 product.

The device also features a reduced power or shutdown mode that virtually eliminates the quiescent power supply when the IC is not active.

The primary application for the 'LBC187 is for battery operated, portable equipment where power consumption is a key factor. A separate consideration, and one that usually goes hand in hand with these factors, is that of shear physical size. With the 'LBC187, TI has used the latest SSOP packaging to reduce board area to an absolute minimum. The new SSOP package reduces board space to 43% of the standard 28-pin SOIC package Couple this with the small 0.2 µF and you have the ideal single supply solution for space restricted applications.

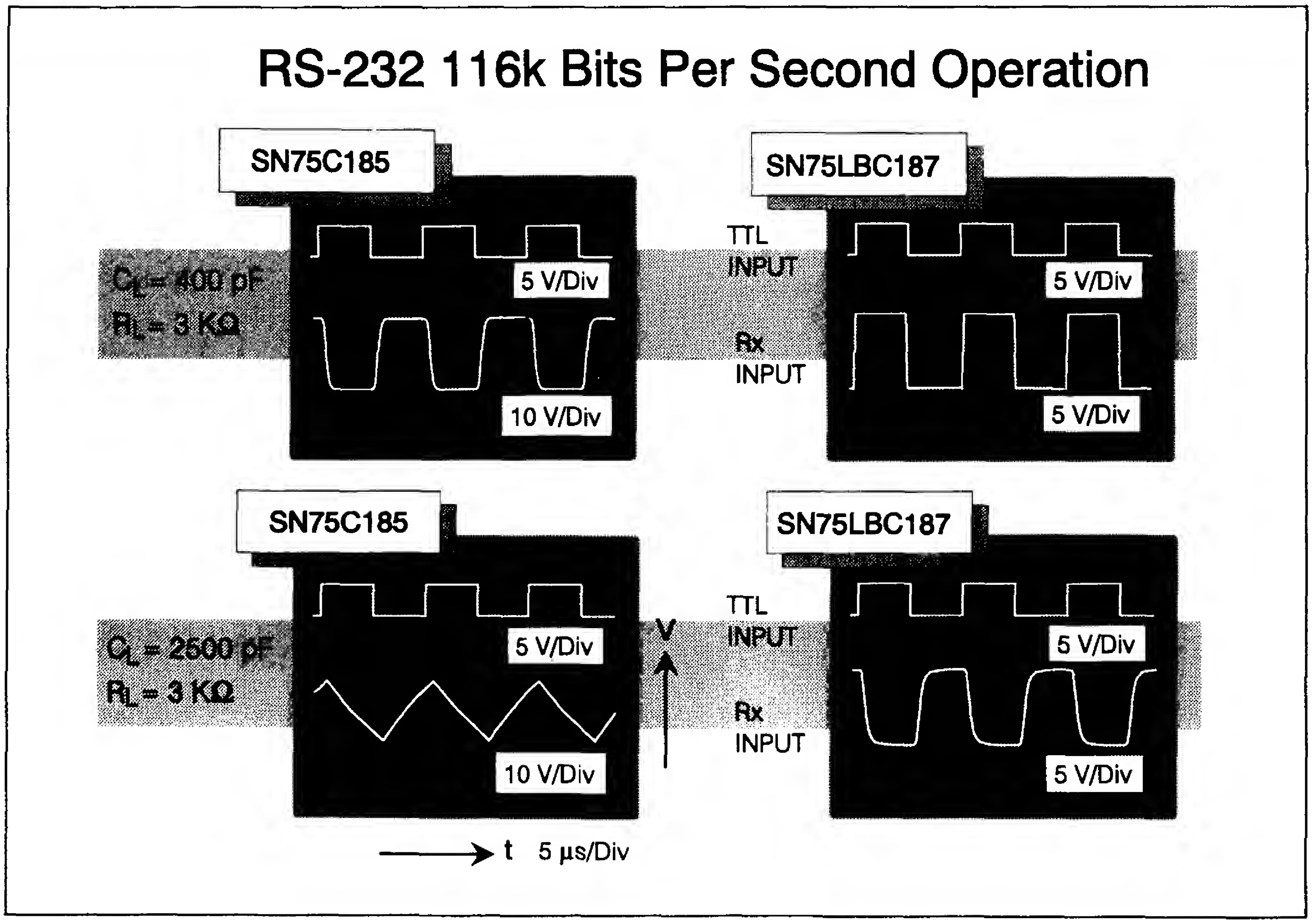


Figure 4.19 - RS-232 116k Bits Per Second Operation

2.5.1 SN75LBC187; 116 kbps operation

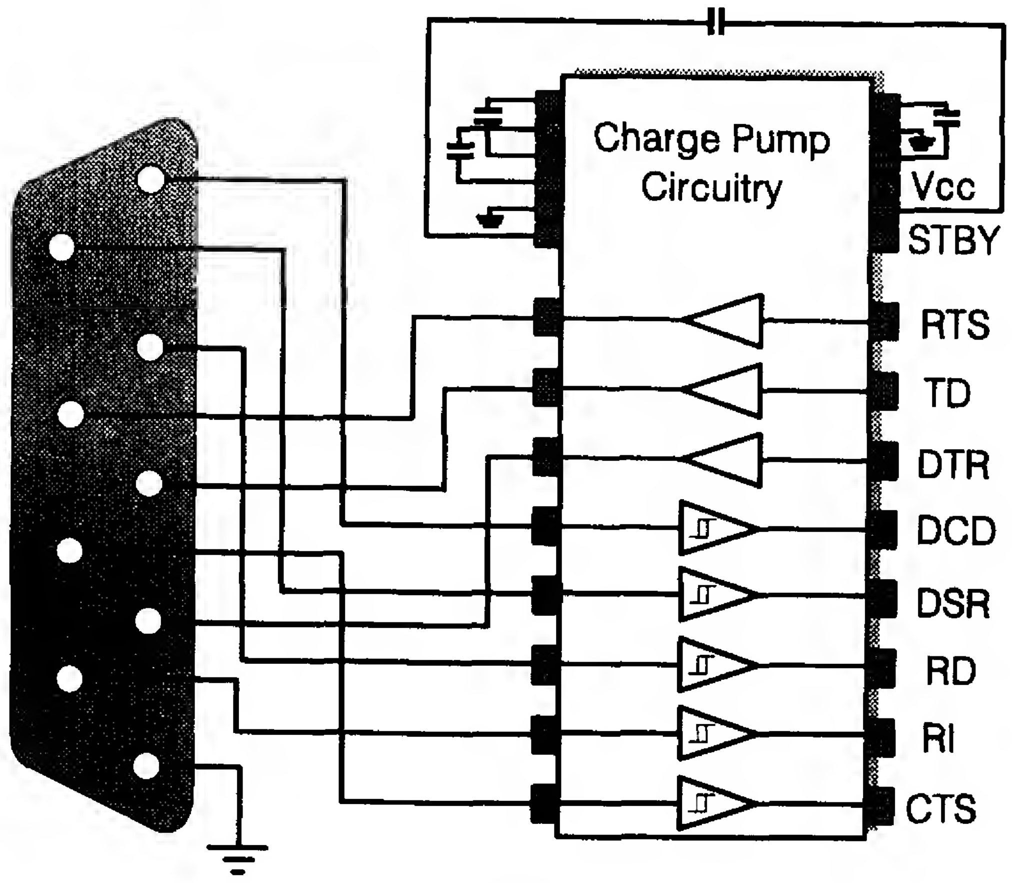
As discussed in section 2.3.1 the limitation on data rate is one of short circuit output current and the actual load capacitance. With the 'LBC187 the driver short circuit current, I_{OS}, is higher than say the SN75C185 and is therefore able to drive longer line lengths at higher data rates. Figure 4.19 illustrates this. The 400 pF load in the top half of the figure represents a cable approximately 3 metres long. As the 'scope traces show, the 'C185 produces a perfectly acceptable output trace at 116 kbps. Similarly with the 'LBC187 trace.

If the line length is now upped to 20 metres or 2500 pF load, we can see how the short circuit current limit now limits the slew rate. With the 'LBC187 the trace is still acceptable and will provide reliable data transmission. With the 'C185, the data will still be transmitted but the probability of error is now increased. Most software programs that operate 116 kbps, e.g. Laplink™ (Laplink is a trademark of Travelling Software Inc.) provide the interconnect cable as part of the system. In most cases this cable is less than 3 metres in line length so either the 'C185 or 'LBC187 would be able to transmit data reliably. It is interesting to note that both devices would meet EIA-232-D if the rise time to unit interval relationship was extrapolated, however both would fail EIA-232-E. Of course conformance to EIA-232 is not relevant above 20 kbps.

2.5.2 Conformance to EIA-562

A new standard has recently been introduced in an attempt to provide a low power standard for 5 volt systems and also to increase the data rate over EIA-232. Known as EIA-562, the standard increase the maximum data rate from 20 kbps to 64 kbps and facilitates lower driver voltages. The downside is the reduced noise margin at the receiver. The specification also details the rise time and ripple conditions of the driver. The SN75LBC187 is fully conferment to this standard.

SN75LV4735; 3.3V EIA-232 PC Interface



- Fully Meets EIA-232 Driver Requirements
  V_{OH} Min = 5.5 V, V_{OL} Min = -5.0 V
- Operates from Single 3.3 volt Supply 10% Tolerance
- Supply Current 10 µA in Standby Mode and 8.5 mA when Active
- Drives 2500pF Load at 20 kbps
- Uses 5x0.47 µF Capacitors For Charge Pump

SSOP Package

Figure 4.20 - SN75LV4735; 3.3V EIA-232-E PC Interface

2.6 SN75LV4735; 3 Volt EIA-232 PC Interface

Continuing the move to lower power systems the obvious choice is to reduce the supply voltage of the system. Assuming supply current remains constant power dissipation is instantly reduced. The driving force behind this reduction is once again the notebook type PC equipment. To facilitate the move to 3 Volts, TI has introduced the SN75LV4735. From 3 volts the device is still capable of producing the required V_{OH} and V_{OL} for conformance with EIA-232.

Once again the device is designed specifically for the DB9S PC DTE interface containing 3 drivers and 5 receivers for a single package solution.

The device is packaged in the TSSOP package with a board area of only 22 mm^2 and a maximum package height of 1 mm.

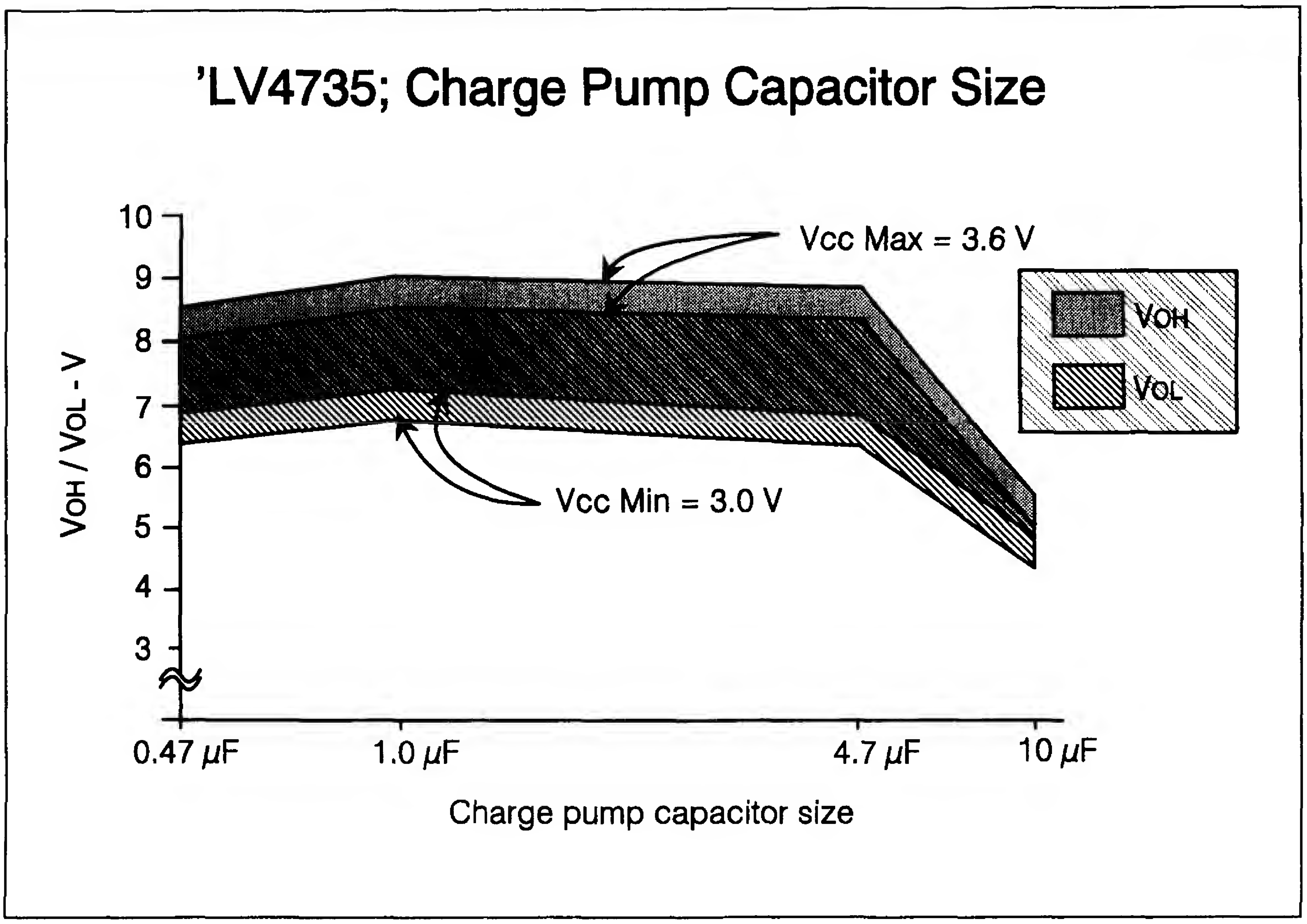


Figure 4.21 - 'LV4735; Charge pump capacitor size

2.6.1 Charge Pump Capacitor Selection

The data sheet for the SN75LV4735 states the minimum capacitor size to be 0.47 µF with a typical specified at 1 µF. Figure 4.21 shows the effect of increasing the capacitor size on the sustainable EIA-232 line output voltage when loaded with a 3k ohm load. It is clear peak performance is reached at 1 µF, increasing beyond this value begins to degrade the performance of the charge pump in its ability to charge the capacitors before their charge is transferred. The designer should bear this in mind when designing his system.

2.7 ACEs (UARTs) From Texas Instruments

Most EIA-232 systems use dedicated communication controllers. Termed ACEs (Asynchronous Communication Elements) or UARTs (Universal Asynchronous Receiver Transmitter), these devices are responsible for controlling the exchange of information over the EIA-232 interface.

The ACE

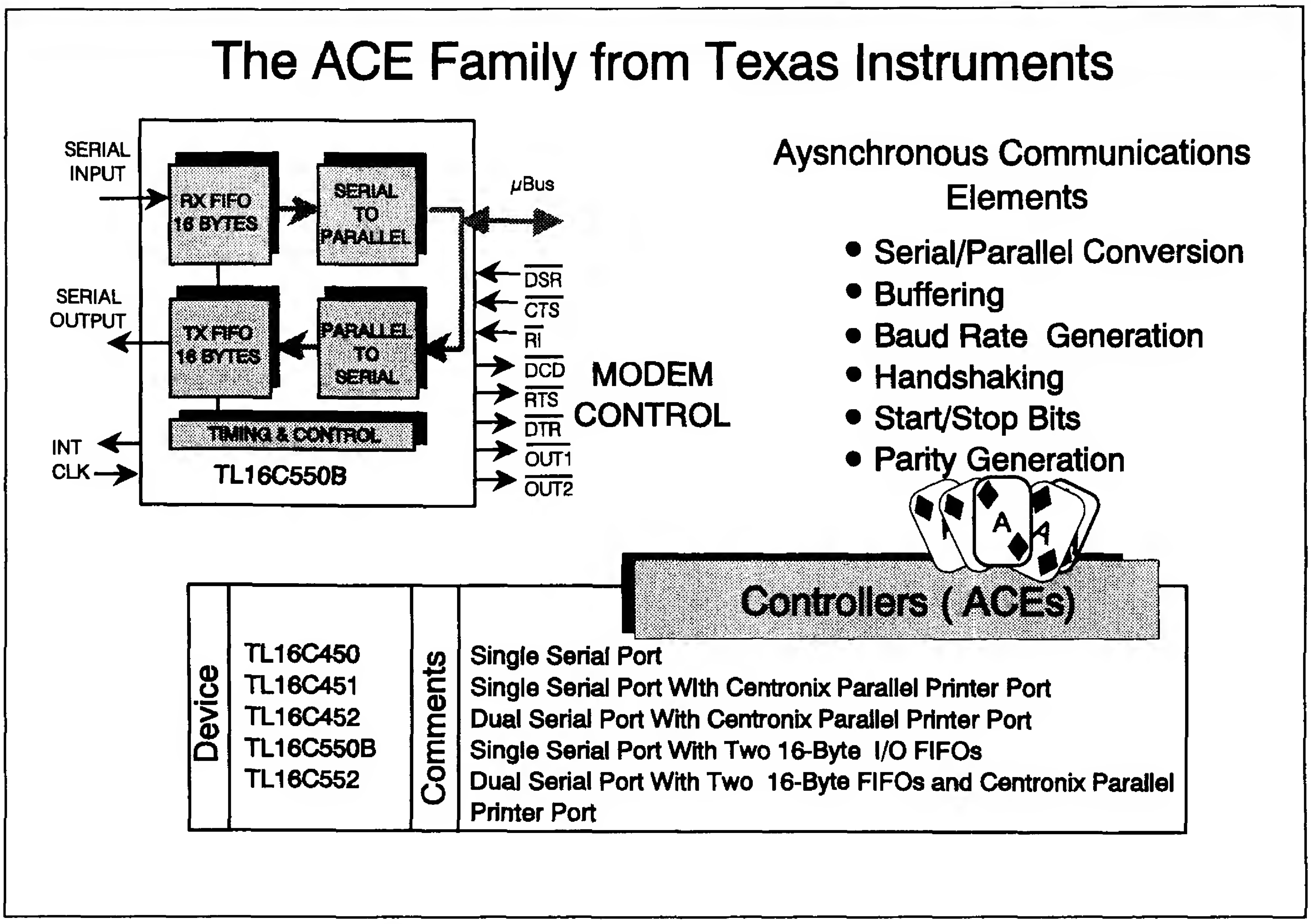
The ACE is a dedicated asynchronous communications controller designed to off load most of the communication activities from the CPU, thus freeing the CPU for other activities. It has the ability to add or delete start and stop bits and provide odd/even parity code generation and detection. Industry standard devices such as the **TL16C450** family contain many extra features as listed below:

- **Programmable bps-rate generator**
- **Adds and deletes standard asynchronous communication bit**
- **Fully programmable serial interface characteristics**
- **Data communication diagnostic capability**
- **Modem-control functions**
- **Simple interface to microprocessors**
- **Maximum data rate of 256 k bits per second**

All devices are designed using Texas instruments EPIC™ CMOS process and operate from a single 5 V supply. The **TL16C450** is the most common choice for standard PC applications as well as many other asynchronous serial applications. The TL16C450, housed in a 40-pin package, contains all the necessary facilities for implementing a single asynchronous serial port. The CPU within the system can read and report on the status of the ACE at any point in the ACEs operation. Reported status information includes the type of transfer operation in progress, the status of the operation, and any error conditions encountered, parity, overrun etc.

The TL16C450 ACE includes a programmable, on-board, bps-rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to (2^{16} -1) and producing a 16 x clock for dividing the internal transmitter logic. Provisions are included to use this 16 x clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimise the computing required to handle the communications link. The **TL16C451** is similar to TL16C450 with the single serial port, but also contains a Centronix parallel printer port. The IBM PC AT/XT sets the standard for this parallel printer interface that all "compatible" manufactures have to follow. TTL-level signals are presented on a 25-pin D-type socket. Apart from the choice of connector, this parallel printer port is directly compatible with the "Centronix" standard printer interface. The **TL16C452** has two serial ports plus a parallel Centronix printer port. Using this ACE together with two SN75C185s provides a simple three chip complete solution for the two EIA-232 ports plus a printer port that is common on basic PC configurations.

EPIC is a trademark of Texas Instruments Incorporated



The ACE Family from Texas Instruments

Aysnchronous Communications Elements

- Serial/Parallel Conversion
- Buffering
- Baud Rate Generation
- Handshaking
- Start/Stop Bits
- Parity Generation

Device	Comments
TL16C450	Single Serial Port
TL16C451	Single Serial Port With Centronix Parallel Printer Port
TL16C452	Dual Serial Port With Centronix Parallel Printer Port
TL16C550B	Single Serial Port With Two 16-Byte I/O FIFOs
TL16C552	Dual Serial Port With Two 16-Byte FIFOs and Centronix Parallel Printer Port

Figure 4.21.1 - The ACE Family from Texas Instruments

2.7.1 The FIFO (First-In-First Out)

The CPU can send data at much faster rates than a normal ACE can handle. This is particularly true for today's multitasking applications that demand high performance microprocessors. This can be expensive in CPU overheads as the CPU will be tied to the speed of the serial interface, i.e., data will be transferred over the interface through the ACE and onto the CPU bus. This is true also when the data is exchanged from the CPU to interface via the ACE.

Devices like the **TL16C550B** and **TL16C552** alleviate this problem by including buffer registers and FIFOs in series with the ACE's transmitter and receiver. These are quick access registers that hold data until the CPU can be freed. The CPU can then execute a block read or write.

The ACE is, in effect, isolated from the slow communications channel.

The TL16C550B is similar to the TL16C450, but two 16-byte FIFOs are included to buffer the transceiver and receiver data stream, further reducing the number of interrupts from the microprocessor.

2.7.2 Forward-Looking Performance With Backward Compatibility

By allowing two modes of operation, the TL16C550B allows users to maintain software compatibility with earlier industry standard ACEs such as the TL16C450. In addition to the TL16C450 mode, the TL16C550B can operate in the FIFO mode. In FIFO mode, two 16-byte FIFOs (First-In-First-Out) are enabled to relieve the CPU of excessive software overheads. The independent receive and transmit FIFOs act as buffers, vastly reducing the number of interrupts required. Furthermore two dedicated pins serve as handshaking lines to a DMA (Direct Memory Access) controller, thus allowing the FIFOs to load and unload data without direct intervention from the CPU.

The flagship of the range is the TL16C552, which is similar to the TL16C452 in structure but with the added advantage of input/output FIFOs as in the TL16C550B

This device serves two serial input/output interfaces simultaneously in either microcomputer or microprocessor-based systems. In addition to its dual asynchronous serial communication capabilities, the TL16C552 provides a fully bi-directional parallel data port that fully supports the parallel Centronix-type printer. The parallel port and the two serial ports provide IBM PC/AT compatible computers with a single low-power device to serve the three-port system. Like the TL16C550B, the TL16C552 contains 16-byte receive and transmit FIFOs that act as buffers to reduce the number of interrupts on the CPU. Also in common with the TL16C550B, the device contains two pins for each ACE that serve as handshaking lines for DMA control. The TL16C552 is housed in a 68-pin plastic-leaded chip carrier, PLCC.

Integration of FIFO and DMA signalling circuitry onto a single chip makes the TL16C550B and TL16C552 one of the most efficient solutions for higher performance multitasking systems.

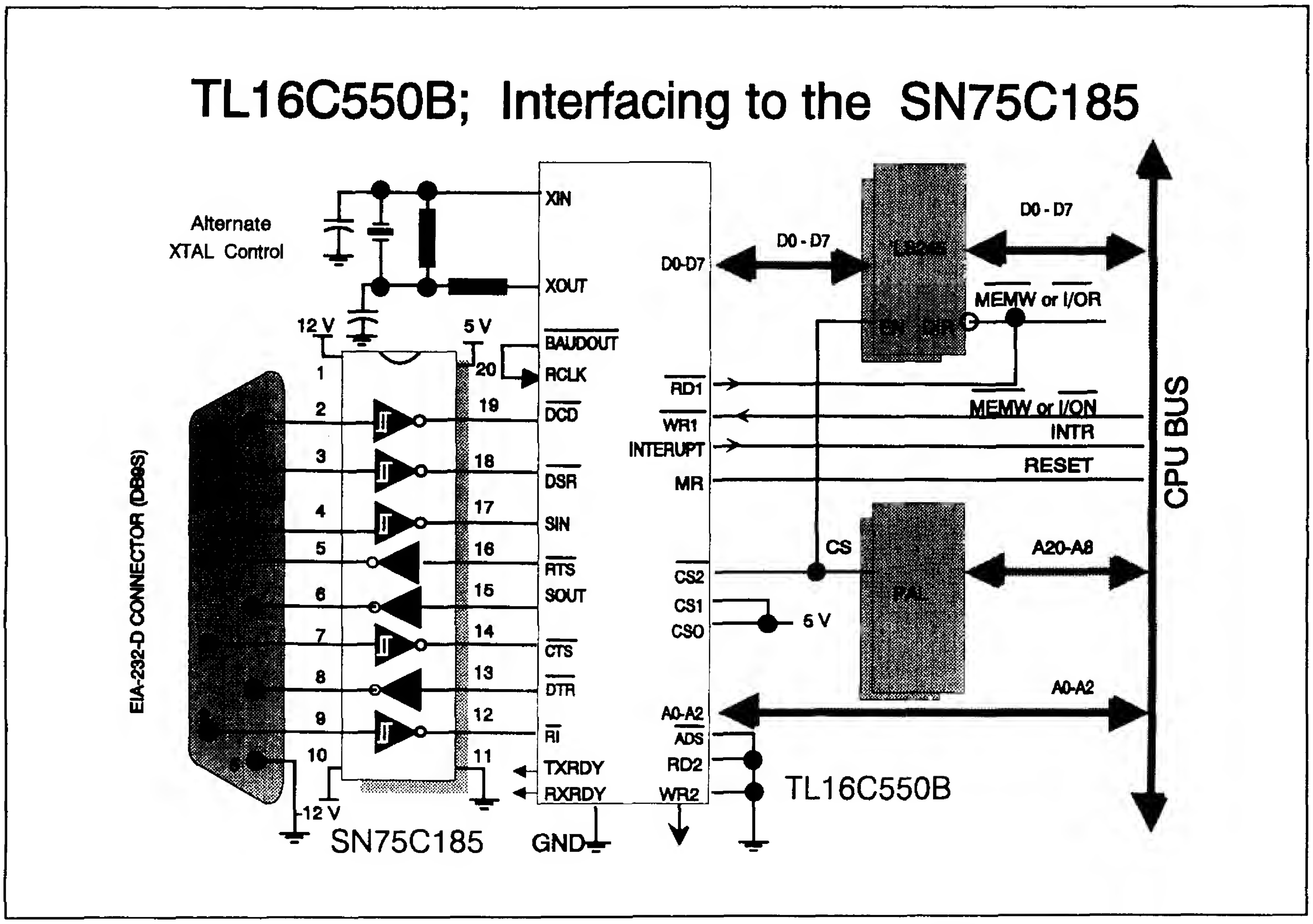

TL16C550B; Interfacing to the SN75C185
Alternate XTAL Control
12 V
5 V
EIA-232-D CONNECTOR (DB9S)
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
-12 V
SN75C185
XIN
XOUT
BAUDOUT
RCLK
DCD
DSR
SIN
RTS
SOUT
CTS
DTR
RI
TXRDY
RXRDY
GND
D0-D7
RD1
WR1
INTERUPT
MR
CS2
CS1
CS0
A0-A2
ADS
RD2
WR2
TL16C550B
D0 - D7
LS245
EN DIR
D0 - D7
MEMW or I/OR
MEMW or I/ON
INTR
RESET
CS
PAL
A20-A8
A0-A2
6 V
CPU BUS

Figure 4.21.2 - TL16C550B; Interfacing to the SN75C185

2.7.3 Interfacing Between the TL16C550B and the SN75C185

The circuit shown demonstrates the simplicity, in hardware terms, in implementing an asynchronous serial interface with the SN75C185 driver/receiver and the communications controller TL16C550B.

When interfacing between the TL16C550B ACE and the Intel CPU bus, minimal glue logic is required. Namely an 'LS245 Octal bus transceiver is used to provide drive current to an 'off-card' CPU, and programmable array logic (PAL) to decode address lines and generate a chip select signal. While an exhaustive description of this interface is beyond the scope of this section, a discussion of key interface lines can be useful.

Xin/Xout:

External clock. Connects the ACE to the main timing reference (clock or crystal).

$\overline{\text{baudout}}$,RCLK:

The transmitter reference clock is available externally via the $\overline{\text{baudout}}$ pin. In this application bpsout is fed into the receiver clock to provide a timing reference for the receiver circuitry. Clock rate is established by the reference oscillator clock frequency (xin) and divided by a driver specified by the bps generator divisor latches.

$\overline{\text{TXRDY}}$:

Transmitter Ready Output. This pin is used during DMA signalling.

$\overline{\text{RXRDY}}$:

Receiver Ready Output. This pin is also used during DMA signalling.

D0 to D7:

Databus. Eight 3-state data lines provide the bi-directional path for data, control, and status information between the ACE and CPU bus.

$\overline{\text{RD1}}$, RD2:

Read inputs. When either input is active (high or low respectively) during ACE selection, the CPU is allowed to read status information from the selected ACE register. Since only one of these inputs is required for the transfer of data during the read operation, RD2 is tied to its inactive state, i.e., low.

$\overline{\text{DCD}}$, $\overline{\text{DSR}}$, SIN, $\overline{\text{RTS}}$, SOUT, $\overline{\text{CTS}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$:

These signals are the EIA-232 compatible modem control lines. Devices such as the SN75C185 are employed to convert the TTL/CMOS level signals from the ACE to EIA-232 compatible bipolar voltages of between ±5 V to ±15 V. The signal can then be transmitted over distances of up to 15 m.

The advantages of the SN75C185 can be clearly seen by the simplicity of the interface connections. For example, driving/receiving combinations precisely match the interface requirement, plus the pin-out is aligned directly to the DB9S connector.

$\overline{\text{WR1}}$, WR2:

Write inputs. A logic applied to $\overline{\text{WRI}}$, during ACE selection allows the CPU to write either control words or data into a selected ACE registers. WR2 is tied in active, i.e.: logic low.

INTERRUPT:

When active (high) the interrupt pin informs the CPU that the ACE has an interrupt to be serviced. This interrupt could occur for one of four reasons;

- **Receiver error**
- **Received data available or time-out (FIFO mode only)**
- **Transmitter holding register empty**
- **Enable modem status interrupt**

The interrupt is reset (deactivated) either when the interrupt has been serviced or by a master reset (MR).

MR:
Master reset. When active (high), MR clears most ACE registers and sets the states of various outputs (i.e. interrupt).

CS0, CS1, $\overline{\textbf{CS2}}$:

Chip Select. An active low on the $\overline{\text{CS2}}$ pin selects the ACE. CS0 and CS1 must be tied active (high) to ensure proper functioning of the $\overline{\text{CS2}}$ chip select. A logic high on $\overline{\text{CS2}}$ will de-select the ACE.

A0 to A2:
Register Select. These three inputs are used during read or write operations to select the appropriate ACE registers. For example, providing the correct write/read operation had taken place at logic 0 at A2, A1, and A0 would cause the receiver buffer (read) or the transmitter buffer to write.

$\overline{\textbf{ADS}}$:

Address strobe. An active low on $\overline{\text{ADS}}$, the register select signals (A0 TO A2) and chip-select signal ($\overline{\text{CS2}}$) drive the internal logic directly.

2.8 EIA-232 Products Summary

In this section we have discussed devices which are concerned primarily with the DB9S connector. TI also has a wide range of other EIA-232 ICs which offer differing combinations of drivers and receivers which can offer the optimum solution for your system. The reader is advised to consult the current edition of Data Tranmssion Circuits Data Book (Reference SLLD001) which contains a complete selection guide of EIA-232 products.

2.9 EIA-232 Selection Guide

Data Transmission Circuits

Function	Per Package	Type	Features
	2	SN75150	Industry Standard
		UA9636AC	Industry Standard
Line Driver	4	LT1030	Robust bipolar design, with 3-state driver outputs
		SN55188	-55°C to 125°C temperature range
		SN75188	Industry standard
		SN65C188	-40°C to 85°C temperature range
		SN75C188	Low-power BiMOS
		SN65C198	-40°C to 85°C temperature range
		SN75C198	Low-power BiMOS with sleep-mode
Line Receiver	4	SN75154	Industry standard
		SN55189	-55°C to 125°C temperature range
		SN75189	Industry standard
		SN55189A	-55°C to 125°C temperature range
		SN75189A	-55°C to 125°C temperature range
		SN65C189	-40°C to 85°C temperature range
		SN65C189A	-40°C to 85°C temperature range
		SN75C189	Low-power BiMOS
		SN75C189A	Low-power BiMOS
Line Driver / Receiver	1/1	SN75155	On-chip 5-v regulator
	2/2	MAX232	On-chip charge pump
	2/2	LT1080	On-chip charge pump and 3-state outputs
	2/2	LT1080	On-chip charge pump
	3/3	LT1039	Robust bipolar design, with 3-state outputs

Function	Per Package	Type	Features
Line Driver / Receiver	3/3	SN65C1406	–40°C to 85°C temperature range
	3/3	SN75C1406	Low-power BiMOS
	4/4	SN75186	Robust bipolar design, with loopback
	4/4	SN65C1154	–40°C to 85°C temperature range
	4/4	SN75C1154	Low-power BiMOS
	3/5	SN65C185	–40°C to 85°C temperature range
	3/5	SN75C185	Optimised for DB9S (9-pin) connector
	3/5	SN75LV4735	3 volt operation
	3/5	SN75LBC187	Optimised for Laptop Applications

Control Circuits

Function	Type	Features
ACE[+]	TL16C450	Single ACE
	TL16C451	Single ACE with parallel port
	TL16C452	Dual ACE with parallel port
	TL16C550B	Single ACE with FIFO[§]
	TL16C552	Dual ACE with parallel port and FIFO

Notes

[+] **ACE: Asynchronous Communications Element.**
[§] **FIFO: First In First Out.**

2.9 Single Ended Transmission Beyond EIA-232

Because of its inherent simplicity and relatively low cost single ended transmission is used in a variety of applications more 'challenging' than EIA-232. In the following section we consider how to extend the use of single ended transmission, including the need for line termination, and the effects of having multiple loads attached to a line.

2.9.1 Increasing The Single Ended Data Rate

At relatively low data rates such as those employed in EIA-232 we can treat the cable as a pure short circuit and assume that the propagation delay of the signal along the cable is negligible. Any signal reflections will return back to the transmitter terminals before the original signal has reached its peak value, and do not therefore impact the overall system performance. Systems such as this can be considered as lumped parameter models, in which termination is not required.

Ads data rates are increased then the speed and shape of the data signal will start to be governed more by the electrical characteristics of the cable, such as its capacitance, inductance, and resistance. Reflections caused by the original signal transition will now be seen at the transmitter terminals after the original signal has reached its peak level. The data transmission system, therefore, needs to be treated as a true transmission line and terminated accordingly.

The impact of incorrect termination is covered later in this book, but it is sufficient to note here that even if termination impedances are carefully chosen, in a real life system it is almost inevitable that reflections will still occur. Once the reflections have eventually settled, the value of the voltage left on the line is equal to the ideal open circuit voltage multiplied by the termination impedance and divided by the sum of the driver output impedance and termination impedance.

It is not only the final steady state d.c. voltage level which is of importance in achieving increased single ended data rates. It is also desirable that the initial signal level should exceeds the receiver threshold voltage in a single transition. The value of this initial signal step depends upon the low level driver output voltage, the amount of current in the line, and the characteristic impedance of the line (Z_0) ;

$$V_s = V_{ol} + Z_0 I_l$$

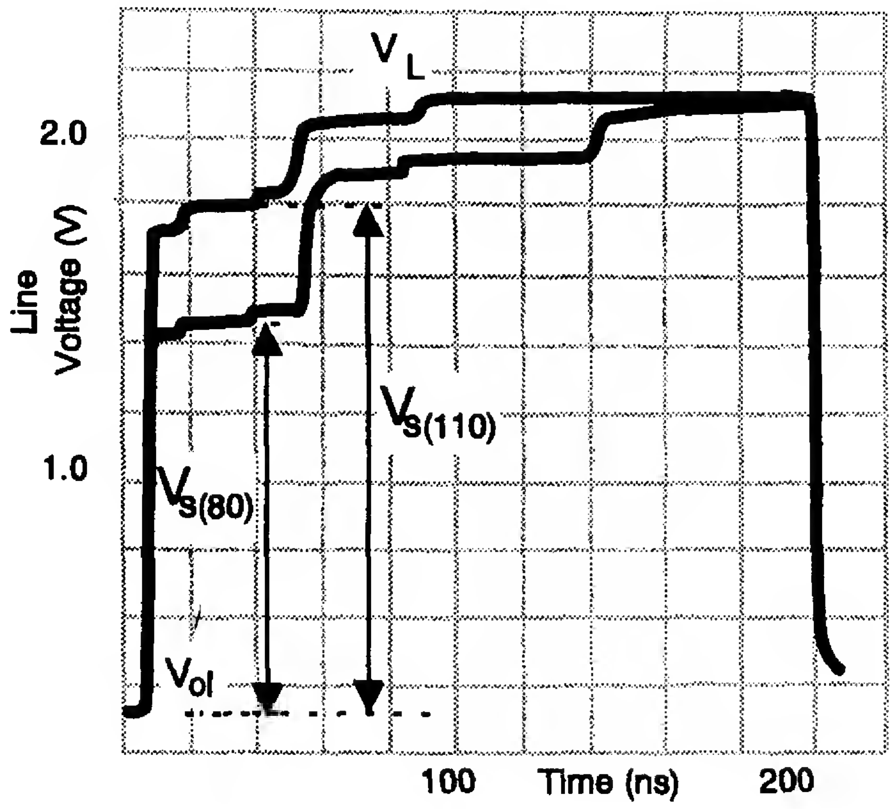
The indicated characteristic impedance of any given cable, however, will not normally be the impedance seen by the signal as it travels along the line. The primary reason for this is the capacitance associated with each driver connected to the line.

Extending The Use of Single Ended Transmission

Increased Data Rates/ Line Lengths :

$t_T < 2\,t_{pd} \longrightarrow$ Terminate !

$$\boxed{V_L = \frac{Z_D \cdot V_{max}}{Z_D + Z_T}}$$



Multiple Stations

- Additional loads
- Additional Capacitance

Need To Recover the Step Voltage !

$$\boxed{V_S = V_{OL} + Z_L\, I_L}$$

Figure 4.22 - Extending The Use Of Single Ended Transmission

2.10 Multi-Point Single Ended Communications

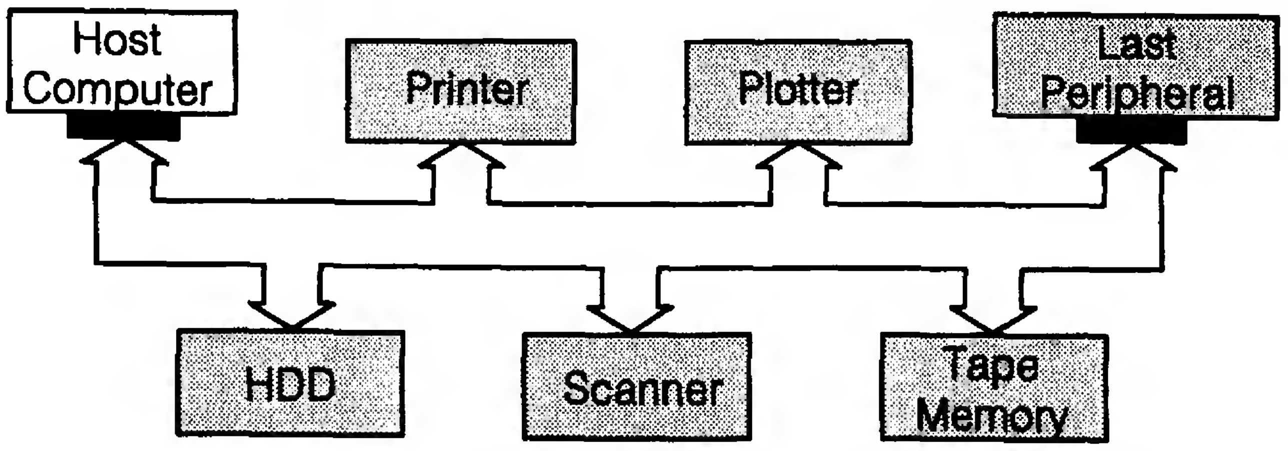
Multi-point communication attaches extra loads, in the form of transmitters and receivers, to be added to the transmission line. Provided they do not cause too great a shunting effect on the line, and are evenly distributed, these loads can be treated as an extra distributed capacitance along the line. This additional capacitance decreases the effective line impedance, sometimes by as much as 50%.

If we consider two lines with different characteristic impedances, we can illustrate the effect of the reduction in transmission line impedance seen by the signal. Even a relatively small (20%) decrease in line impedance has a significant impact on the first level step voltage as can be seen in figure 4.22. Therefore, if we are to maximise the data rates in multi-point communication systems it is important that we somehow counteract the effects of these additional capacitive loads.

In order to do this, the terminator in a high speed, or true transmission line, system is required to source as much current as possible during de-assertion. This can be better illustrated if we take a look at a common example of a high speed single ended multi-point communication system such as the Small Computer Systems Interface, otherwise known as SCSI.

2.10.1 SCSI Overview

Small Computer Systems Interface - Physical Layer



- Multi-point half duplex transmission
- 18 (8-bit data) or 27 (16-bit data) I/O lines
- Single ended and differential (RS-485) interface
- 25 metre maximum line length for differential SCSI
- Up to 10 million data transfers per second

Figure 4.23 - SCSI Overview

As noted above SCSI is the acronym for the Small Computer Systems Interface which details the ANSI specification for a peripheral bus and command set. The objective of the interface is to provide high speed data transfer between computer peripherals independently of the host, helping to free up the host for more user oriented commands or activities. Although a relatively new standard, there are already a large number of disk drives, notebooks, PCs, and CD-ROM drives which incorporate a SCSI port.

Basic SCSI is an eight bit (plus parity) parallel I/O bus with nine control/handshaking lines, making 18 lines in total. More recently, to increase the data throughput, the standard has made provision for the data bus to be extended to 16 bits whilst maintaining the nine control lines. This is referred to as wide SCSI.

It is beyond the scope of this book to discuss the complete SCSI standard, so we shall concern ourselves with the physical layer only. For more information on the standard the reader is encouraged to refer to the numerous publications on SCSI

2.10.2 Single Ended SCSI - High Speed Multi-Point Communication

There are two electrical specifications referred to in the SCSI standard, single ended and differential. Here we are concerned only with the single ended interface, the differential standard being discussed elsewhere in this book.

Single ended SCSI employs a driver and receiver configuration utilising TTL logic levels as shown, and is primarily intended for applications within a cabinet, with the maximum line length being limited to 6 metres, and with up to 6 devices connected to the line.

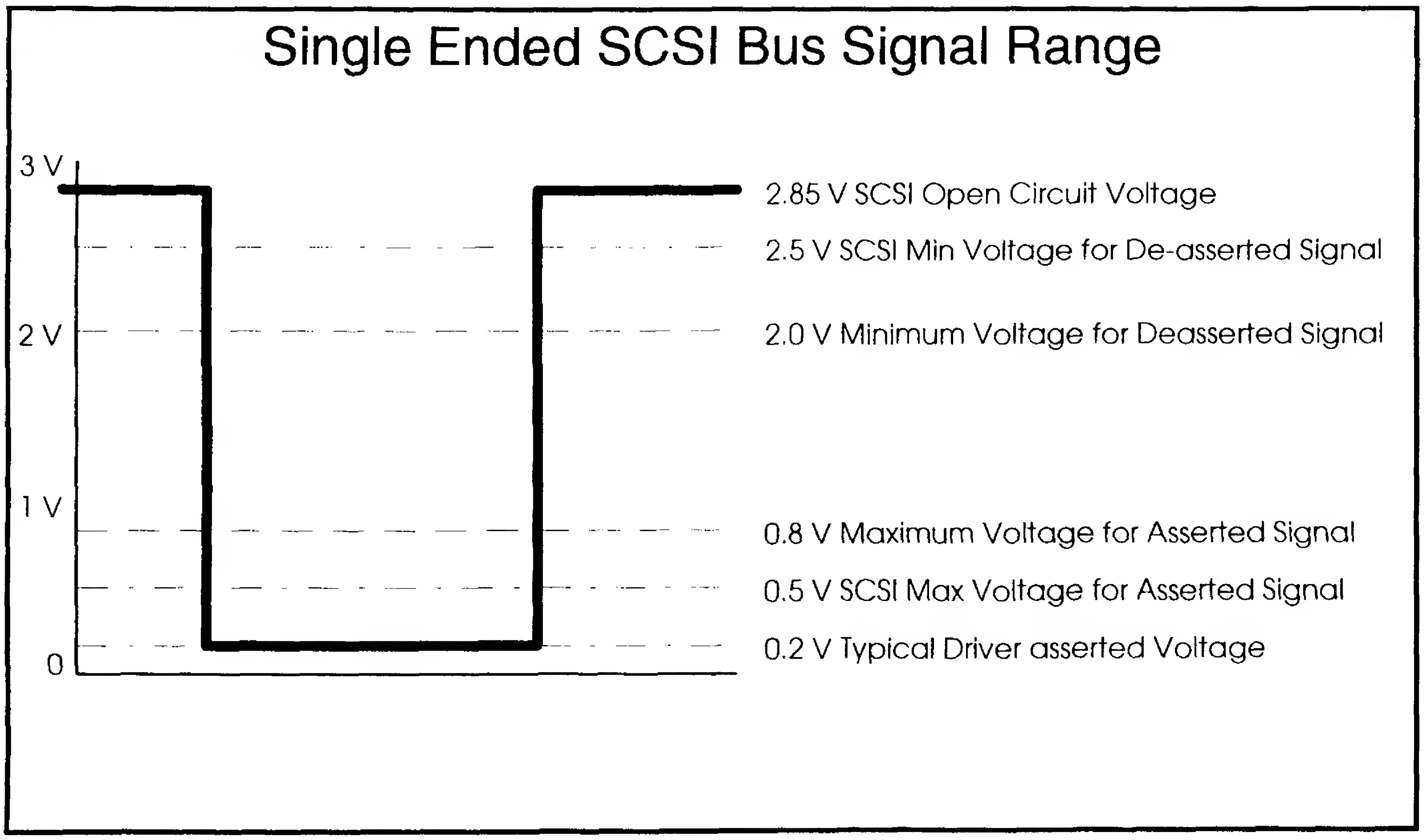


Figure 4.23.1 - SCSI Bus Signal Range

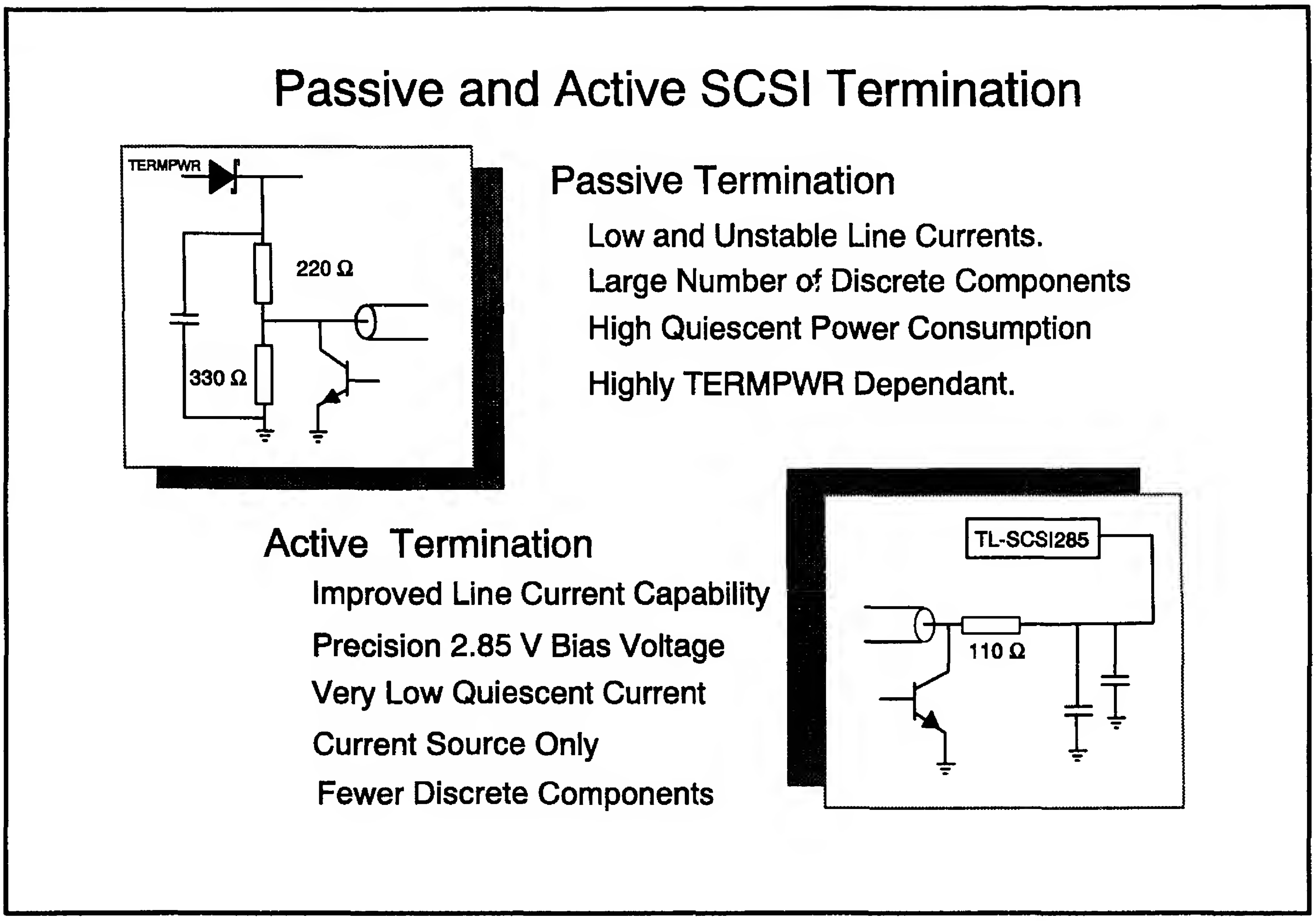
Whereas EIA-232 had data rates of 20 kbps, single ended SCSI is intended for data rates of between 1 and 5 Million Transfers per second (equivalent to 10-40MBytes/sec) The importance of termination in high speed multi-point communications is clearly demonstrated as innovative techniques are enabling the maximum transfer rate to approach 10 MTps, or 80 Mbps.

2.10.3 Single Ended SCSI Termination

Proper termination of a bi-directional bus such as SCSI requires terminators at each end of the cable, with the terminators job being to source as much current as possible during de-assertion. This role is restricted by the SCSI specification, however, which limits each terminator to supplying a maximum of 24 mA thus preventing the line current from exceeding the 48 mA current sink limit of the open collector drivers.

The role of the SCSI terminator is not confined to low to high signal transitions. Once a signal has been de-asserted the terminator is required to bias the bus lines to the correct open circuit voltage level to ensure maximum noise margins.

We shall now take a look at the two best known methods of single ended SCSI termination.



Passive and Active SCSI Termination

Passive Termination

Low and Unstable Line Currents.
Large Number of Discrete Components
High Quiescent Power Consumption
Highly TERMPWR Dependant.

Active Termination

Improved Line Current Capability
Precision 2.85 V Bias Voltage
Very Low Quiescent Current
Current Source Only
Fewer Discrete Components

Figure 4.24 - Passive & Active SCSI Termination

2.10.4 Passive and Active SCSI Termination

SCSI termination has traditionally been carried out using passive termination networks. As illustrated in figure 4.24 these consist of 2 resistors per signal line ; a 220 Ω pull up resistor connected to the termination power source (Termpwr), and a 330 W pull down resistor connected to ground. The Schotky diode is needed by all termination schemes to protect the power source from reverse currents.

This type of termination typically results in a maximum line current of around 17 mA. Assuming the terminator is on a heavily loaded bus, signified by an impedance of approximately 75 Ω, then the above equation gives a first step value of 1.76 V - well short of the desired 2.0 V level.

In addition to this limited current capability and the power consumption penalty imposed by the resistor dividers, passive terminators also suffer from an unregulated line bias voltage. As a result the line voltage will fluctuate with variations in the load current and Termpwr, leading to smaller noise margins, lower line currents, and reduced data rates.

The most common alternative to passive termination replaces the resistive network with a voltage regulator in series with a single 110 Ω resistor per line (fig 4.34). This method, known as Active, Boulay, or Alternative 2 termination, was developed to overcome two of the main shortcomings of passive termination.

The 110 Ω resistors increase the typical line current available on de-assertion to 21 mA, which, from a transmission line viewpoint, is equivalent to a 35% increase in line impedance. The line current and the high-level noise margins are also more stable since

Termpwr is no longer used to set the bias voltage directly. Instead it is used to form the input to the voltage regulator, which then provides a regulated bias voltage.

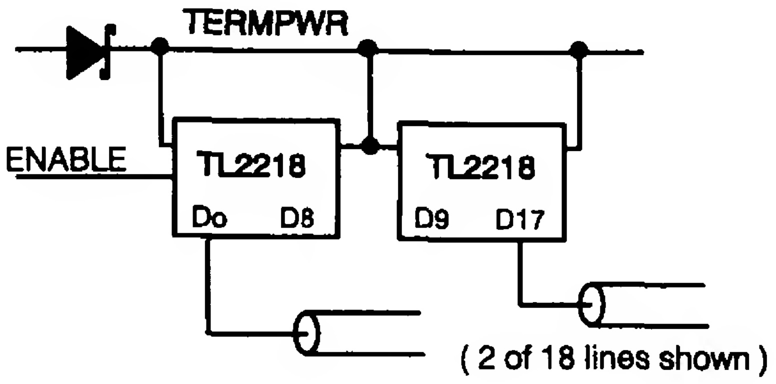
The TL-SCSI285 and TL2217-285 low dropout regulators from Texas Instruments are specifically designed for active SCSI termination. With an overall accuracy of 2 % and a maximum dropout voltage of 0.6V the TL-SCSI285 is the highest performance dropout regulator available for SCSI active termination.

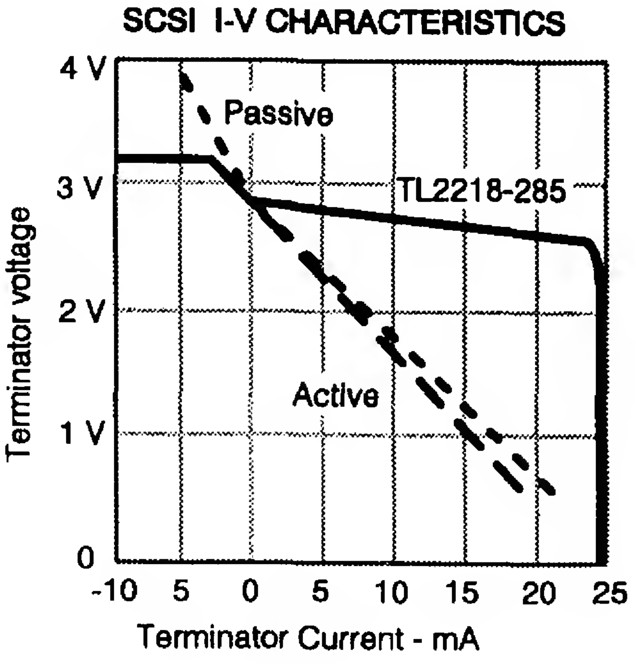
2.10.5 Current Source Termination Using the TL2218

Although active termination brings a number of advantages to SCSI termination these can be further improved upon. The TL2218-285 from Texas Instruments is a completely new type of SCSI terminator which does just that.

TL2218-285 - Current Source Termination

TL2218-285 Enables Single Ended Data Rates of 10 MHz





- **23 mA Applied at First High-Level Step**
- **Very Low Output Capacitance, Typically 6 pF**
- **No External Components Required**
- **Compatible with Active Negation**
- **Thin Shrink Small Outline Package (TSSOP)**

Figure 4.25 - TL2218-285 - Current Mode SCSI Termination

The TL2218-285 is a current mode, or non-linear, device which does not contain a voltage regulator. This means that no filtering or stabilizing capacitors are needed, and so unlike 'completely integrated' active terminators, the TL2218-285 needs no external components.

Another major difference between the TL2218-285 and an active terminator is that the current available on deassertion is independent of the voltage on the output of the terminator (see figure 4.25).

During deassertion the TL2218-285 operates as a 23.5 mA current source which is able to maintain this current level until the signal reaches the correct SCSI open circuit voltage. At this point the TL2218-285 becomes a voltage source of 2.85 V.

The additional current supplied by the TL2218-285 reduces the low-to-high transition time by ensuring that each voltage step is consistently the largest possible. The effect of this can be seen in figure 4.26, which shows the signal wave forms obtained after using a TL2218-285, a commercially available active terminator, and a passive termination network to terminate a 50 W cable (the equivalent of a heavily loaded bus). Even at 10 MHz the first step voltage of the TL2218-285 terminated system still exceeds the desired 2.0 V level.

Another feature of the TL2218-285 is the inclusion of a disable function which allows the terminator output to be shut down. This is particularly useful for a peripheral which finds itself somewhere other than the physical end of the bus, and needs some way of easily 'removing' it's terminator.

If disabled the TL2218-285 consumes just 500 µA of current, and maintains an output capacitance of 6 pF. Allowing for the 15 - 16 pF typical output capacitance of a peripherals transceivers, this will give a total node capacitance well within the 25 pF SCSI limit. An active terminator, on the other hand, will normally maintain a disabled output capacitance of 10 pF, often leaving the system to operate outside of the SCSI specification.

Use of the TL2218-285 also removes two possible causes of system failure or driver damage associated with active termination. Firstly the 2 % output tolerance of the TL2218-285 ensures it does not supply more current than allowed by the driver protecting SCSI limit. The tolerances of the voltage regulator and the 110 Ω resistors used in active termination, however, can result in the terminator supplying in excess of the 24 mA maximum.

The other potentially damaging situation arises when active negation drivers are being used. These devices sense bus voltages and source sufficient additional current to ensure that first step voltages reaches the minimum SCSI level. Despite this attractive feature their relatively high cost has limited their use to ultra fast changing control lines such as ACK and REQ.

To be compatible with active negation drivers it is clear that any terminator connected to the bus must be able to sink current. Again this is a problem with active termination but not with either the TL2218-285 or a passive terminator. The voltage regulator of an active terminator will shutdown when any driver voltage exceeds 2.85 V. This allows the line voltage to rise and any driver which then pulls low may sink more than their 48 mA limit.

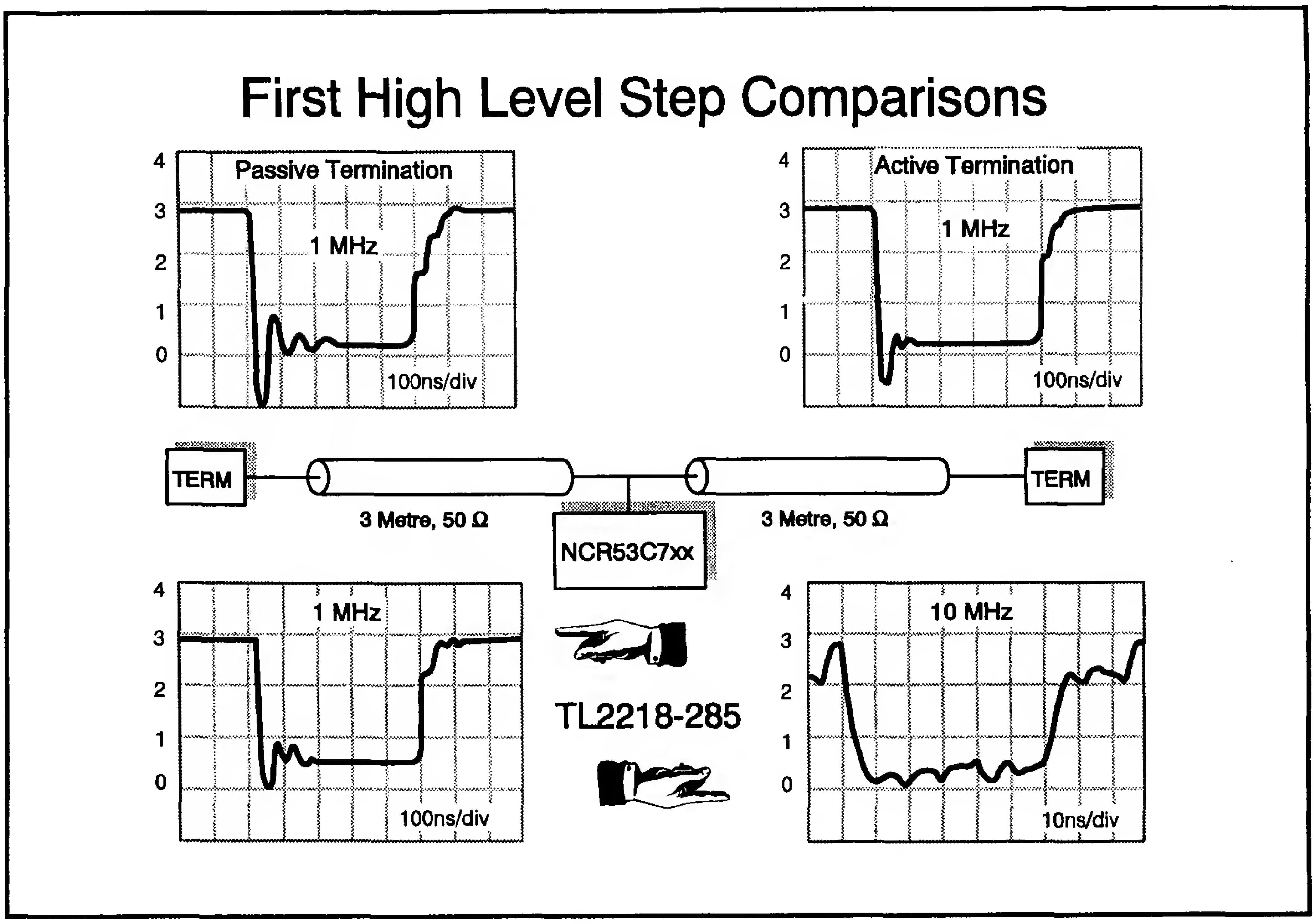


Figure 4.26 - First Step Voltage Comparisons

2.10.6 Power Considerations

As well as enabling increased data rates, termination will also increase the power consumption of a SCSI system. As SCSI has found increased usage in portable or battery powered systems this has become more important. Exactly how much depends upon the method of termination, but not quite as obviously as might at first be thought.

During data on periods, the power dissipation of each of the SCSI termination methods is very similar. For an 8 bit bus with all the data lines asserted the power dissipation in each case will be around 1 W.

During data off periods the position is significantly changed. The resistor dividers of a passive terminator will still draw around 750 mW of power. Both the TL2218-285 and active terminators, however, require a total quiescent current of less than 10 mA, providing a 30x saving in power consumption.

For a single TL2218-285 it is possible to calculate a worst case dynamic power dissipation of 493 mW. This assumes that all nine lines in the package are asserted simultaneously and experience a 50% duty cycle. In some systems it may be desirable to avoid any single device dissipating this much power. This can be achieved by partitioning the SCSI bus lines in an appropriate manner. One such method is to split the data lines between the two devices (for an 8 bit system) and also assign the REQ and ACK lines to separate packages.

Battery powered systems will also benefit from the extended Termpwr range of the TL2218-285. Compared to competing solutions which require a minimum Termpwr of 4 volts, the 3.5 V to 5.5 V range of the TL2218-285 greatly increases the potential for prolonged operation.

3 Differential Data Transmission

3.1 The Need for Differential Transmission Line Standards

This section focuses on balanced transmission line standards. After reviewing key aspects of the standards, the reader will be introduced to the practicalities of implementing a differential transmission scheme based on a factory automation example. Finally, new additions to Texas Instruments EIA product range will be discussed along with their application, where appropriate.

Data transmission between computer system components and peripherals over long distances and under high noise conditions, usually proves to be very difficult if not impossible with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long line system requirements.

A differential communication system involves the use of two signal carrying wires between transmitter and receiver , such that the signal current flows in opposite directions in each wire. The net effect of this is the receiver is only concerned with the difference in voltage between the two wires. The absolute value of the dc common mode voltage of the two wires is not important. In practice, transmitters and receivers have a finite common mode voltage range in which they can operate.

The use of differential communications interface allows transmission at higher data rates over longer distances to be accomplished. This is because the effects of external noise sources and cross talk are much less pronounced on the data signal. Any external noise source coupling onto the differential lines will appear as an extra common mode voltage which the receiver is sensitive to. The difference between the signal levels on the two lines will therefore remain the same. By the same argument, a change in the local ground potential at one end of the line will appear as just another change in the common mode voltage level of the signals The differential output to the line will also provide doubling of the driver's single ended output signal. Twisted pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair..

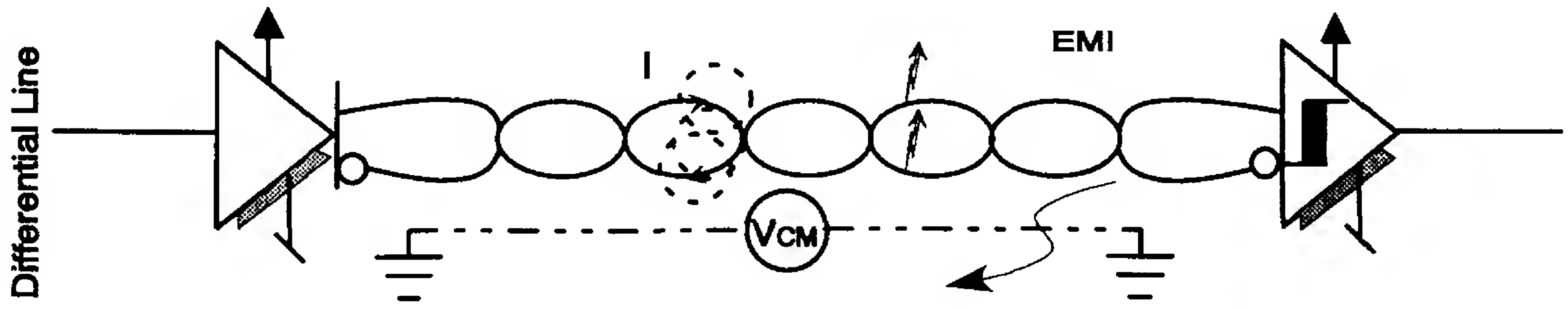
The main disadvantage of a differential system lies in the fact that two cables are required for each communication link. This increases system cost but provides superior performance when data is transmitted at high rates over long distances.

RS-485 and RS-422 are balanced (differential) digital transmission line interface standards developed to incorporate and improve upon the advantages of the current-loop interface and improve on the EIA-232 limitations.

The advantages are;

- **Data rate - to 10 Mbps and beyond**
- **Longer line length - up to 1200 metres**
- **Differential transmission - less noise sensitive**

Differential Transmission



Advantages	Disadvantages
• Noise & cross talk rejection	• More signal wires
• Ground shift rejection	• Moderate - high cost
• Higher data rates	• More complex
• Longer line lengths	

Figure 4.27 Differential Data Transmission

3.1.1 Application Areas

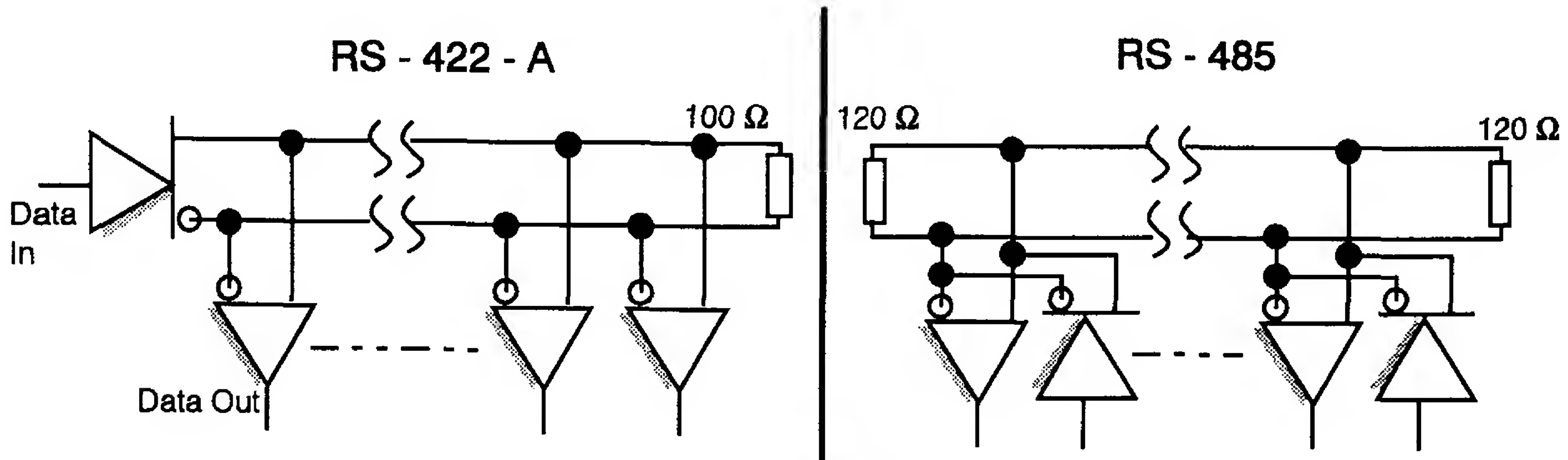
RS-485 is an upgraded version of RS-422-A extending the number of peripherals and terminals that a computer can interface to, particularly where longer line length or increased data rates are called for. Additionally, RS-485 allows for bi-directional multi-point party line communication and can effectively be used for "mini-LAN" applications, such as data transmission between a central computer and remote intelligent stations. For example, between point of sales terminals and a central computer for automatic stock debiting.

As a result of its versatility an increasing number of standard's committees are embracing the RS-485 as the physical layer specification of their standard. Examples include the ANSI (American Nationals Standards Institute) Small Computer Systems Interface (SCSI) which we will discuss in section 4, the Profibus standard, the DIN Measurement Bus.

3.1.2 EIA RS-485 and EIA RS-422

The balanced transmission line standard EIA RS-485 was developed in 1983 to interface a host computer's data, timing or control lines to its peripherals. The standard specifies the physical layer only. Protocols, timing, serial or parallel data, connector choice are all left to be defined by the user

RS-422-A & RS-485; SPEC DETAILS



- 1 Driver - up to 10 receivers
- Simplex communication

- Up to 32 tranceivers (typ)
- Half Duplex communication

KEY PARAMETERS	RS-422-A	RS-485
Maximum common mode voltage	- 7 V to + 7 V	-7 V to + 12 V
Receiver input resistance	4 kΩ	12 kΩ
Driver load	100 Ω	60 Ω
Driver output short circuit limit	150mA to GND	150mA to GND 250 mA to -7 V or 12 V

Figure 4.28 - RS-422 and RS-485 Specification Highlights

RS-485 was originally defined as an upgrade and more flexible version of RS-422-A. Where RS-422 facilitates simplex communication only, RS-485 allows for multiple drivers and receivers on a single line facilitating half-duplex communication. Like RS-422 the maximum line length is not specified but, based on 24 AWG cable, is nominally around 1.2 km. Maximum data rate is unlimited and is set by the ratio of rise time to bit time, similar to EIA-232. In many cases it is the line length of the cable which limits the data rate more than the drivers due to transmission line effects, see section 1.

The differences between the RS-485 standard and the RS-422 standard lie primarily in the features that allow reliable multi-point communications.

3.1.3. RS-422A Driver features

i. Balanced (differential) output voltage source with an impedance of 100Ω or less. Its output differential voltage is in the range 2V minimum to 6V maximum. Additionally the output voltage of either output with respect to ground shall not exceed 6V.

ii. Driver output current, with either output shorted to ground, shall not exceed 150mA.

iii. Output off-state leakage current, with any voltage between -0.25V and 6V applied to either output shall not exceed 100μA.

iv. Output voltage transition times (t_r) are the transitional times between 0.1 and 0.9 V_{SS} and must occur within 10% of a unit interval (t_b) or 20ns, whichever is the greater.

v. Ringing and resulting overshoot and undershoot shall not exceed 10% of V_{ss} where V_{SS} is defined as the difference between two steady state values of the output.

3.1.4 RS-422A Receiver features

i. Differential data input threshold sensitivity of +/- 200mV over a common mode range of -7 to 7V.

ii. Input impedance of greater than 4kΩ.

iii. Input voltage current characteristics shall be balanced such that its output remains in the intended binary state with a differential input of 400mV applied - through 500Ω +/- 1% to each input terminal and common mode range varied between -7V and 7V.

3.1.5 RS-485 Driver features

i. One driver can drive as many as 32 unit loads (one unit load is typically one passive driver and one receiver).

ii. The driver output, off-state, leakage current should be 100 µA or less with any line voltage from -7 V to +12 V.

iii. The driver should be capable of providing a differential output voltage of 1.5 V to 5 V with common-mode line voltages from -7 V to 12 V.

iv. Drivers must have self protection against contention (multiple drivers contending for the transmission line at the same time).

3.1.6 RS-485 Receiver features

i. High receiver input resistance, 12 kΩ minimum.

ii. A receiver input common-mode range of -7 V to 12 V.

iii. Differential input sensitivity of ±200 mV over a common-mode range of -7 V to 12 V.

3.2 Process Control Design Example

To fully understand the considerations of designing an RS-485 system it is advantageous to take a specific design example. In this case we will consider a factory automation system with a host controller and several out-stations. Each out-station is capable of transmitting as well as receiving data.

The general system specification is shown in figure 4.29 and comprises:

i. Furthest out-station is 500 m from the host controller.

ii. We require up to 31 out-stations on the line. With the host controller this totals 32 stations in total.

iii. System data rate will be 500 kilobits per second.

iv. Only one cable will be used for data transmission operating in half duplex mode.

With this system specification the main design consideration are:

i. Line Loading including termination.

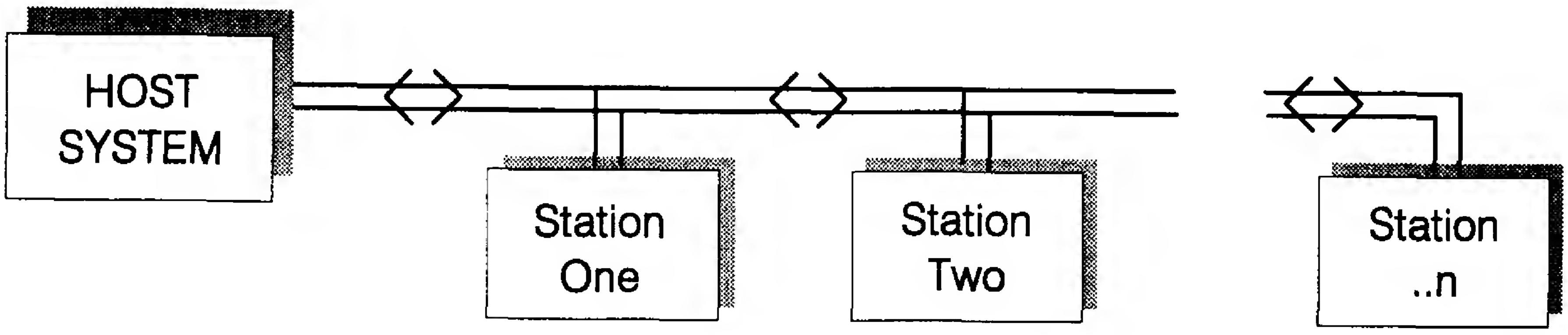
ii. Cable choice

iii. Signal Attenuation and distortion

iv. Fault Protection including fail safe operation

Consider each one of these points:

Process Control Design Example



Considerations:

- Signal Attenuation
- Line Loading
- Cable Choice
- Fault Protection

System Spec:

- 500 m Furthest Station
- 32 Stations
- 500 kbps
- Asynchronous Half Duplex Communication

Figure 4.29 - Process Control Design Example

3.3 Line Loading

The RS-485 standard takes into account the need for line termination and the subsequent loading on the transmission line. The decision on whether to terminate or not will be system dependent and will be affected by the choice of line driver and the maximum line length.

The Unit Load Concept

The maximum number of drivers and receivers that can be placed on a single RS-485 communication bus depends upon their loading characteristics relative to the definition of a unit load (U.L). RS-485 recommends a maximum of 32 unit loads per line.

One U.L (at worst case) is defined as a load that allows 1 mA of current under a maximum common-mode voltage stress of 12 V. The loads may consist of drivers and/or receivers but does not include the termination resistors, which may present additional loads as low as 50Ω total for doubly terminated lines.

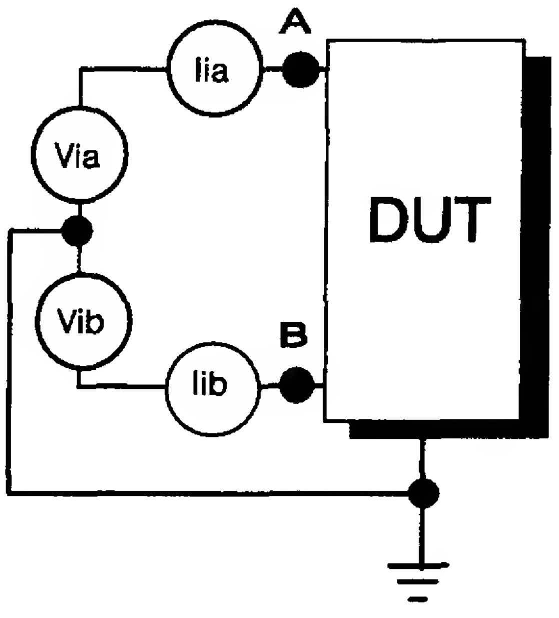
The example in figure 4.30 shows a unit load calculation for the SN75ALS176B. Since this device is internally connected as a transceiver, i.e. driver output and receiver input connected to the same bus, it is difficult to obtain separate driver leakage and receiver input currents. For this calculation reference is made to the receiver input resistance, 12 kΩ, giving a transceiver current of 1 mA. This can be taken to represent 1 U.L. which will allow up to 32 devices to be connected to the line.

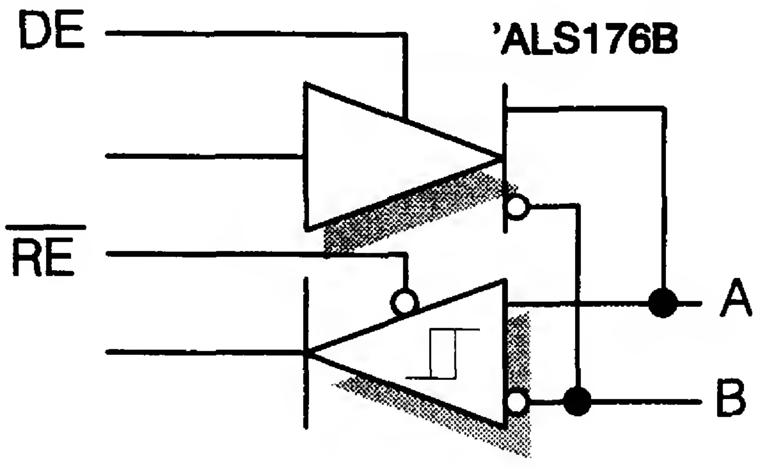
Obviously it may be possible to connect more devices than the RS-485 recommendation, but this is at the designer's risk.

RS-485 - The Unit Load Concept

RS-485 Standard

- Specifes up to 32 Unit Loads Doubly Terminated with 120 Ω
- Unit Load = Load which Allows 1 mA of Current Flowing Under a Maximum Common Mode Voltage Stress of 12 V & -7 V





Example

SN75ALS176B..............(30 Mbps Transceiver)

IL = 1 mA @ 12 V (worst case) Receiver Enabled

$UL = \frac{1}{1} = 1$ UL

i.e 32 = 32 Transceivers/Transmission Line

Figure 4.30 - The Unit Load Concept

3.3.1 Signal Attenuation

Section 1.3 discusses attenuation in more detail but a sufficient rule of thumb is where the attenuation of the line reduces the driven signal by no more than 6 dBV. Attenuation figures are usually supplied by cable manufacturers. The curve in figure 4.31 shows the attenuation curve versus frequency for 24 AWG cable. For 500 metres of cable and using the 6 dBV figure, the maximum attenuation we can tolerate is 0.35 dBV/30 metres. In this case the 500 kbps data rate attenuation is well within this limit. The attenuation of the fundamental frequency and higher frequency components of the signal up to 10 Mbps will still be detectable at the receiver. This effect coupled with the variation of signal velocity with frequency (termed dispersion) results in distortion of the pulse at the receiving end of the line.

Signal Attenuation

- DC Resistance Plus Skin Effect
- Non Linearity Due to Proximity and Radiation Loss
- Details Normally Provided by Cable Manufacturers

👍 Maximum Allowable Attenuation

6 dBV Measured at Receiver
(Half Driver Output Voltage)

Attenuation In 24 AWG Twisted Pair Cable

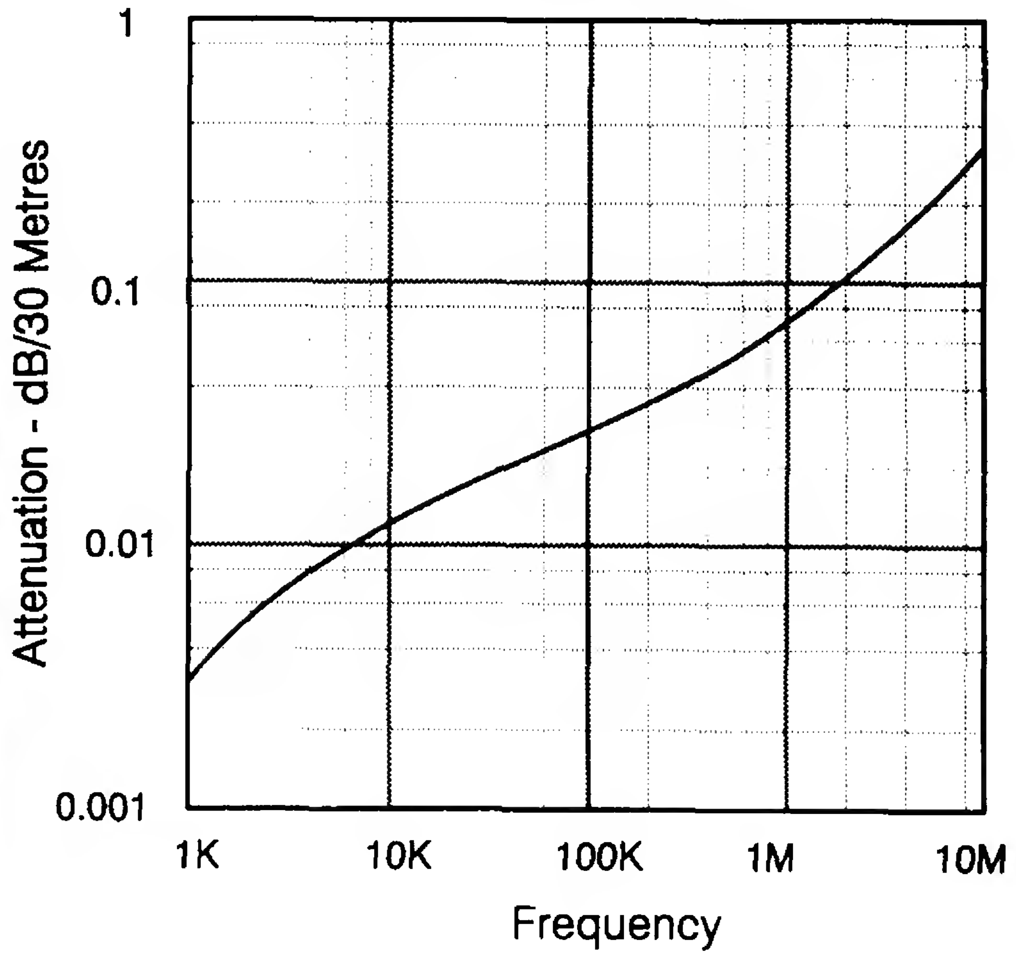
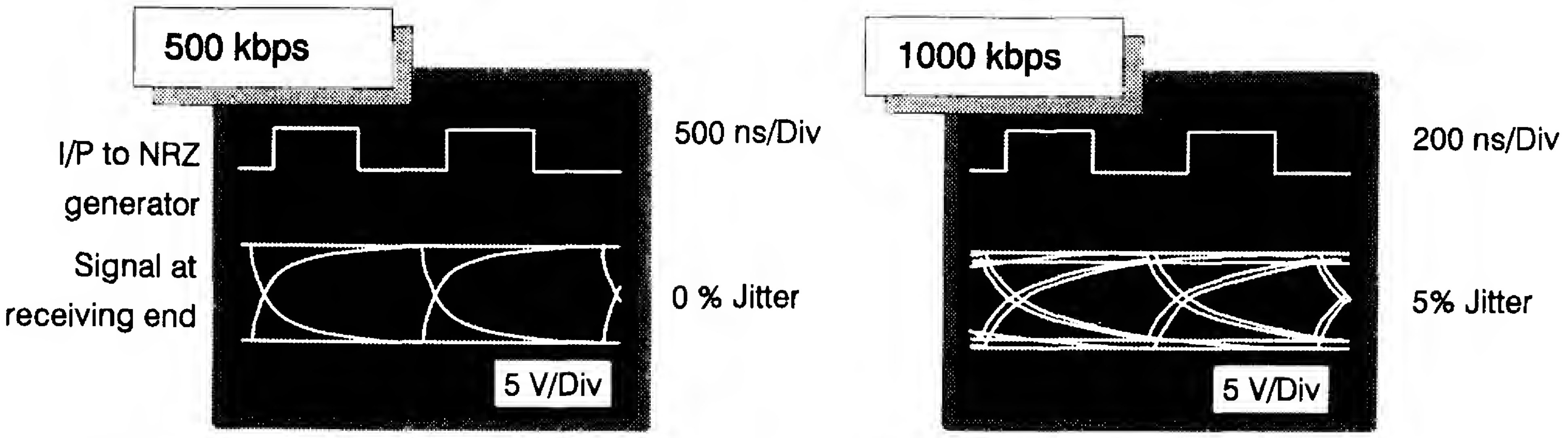


Figure 4.31 - Signal Attenuation

3.3.2 Signal Distortion Vs Data Rate

The simplest way to determine the effects of random noise, jitter, attenuation, dispersion, on the inter symbol interference is by the use of eye patterns. For information on how to set up eye patterns, refer to section 1.4 of this Section. Figure 4.32 shows the distortion of the signal at the receiving end of 500 metres of 20 AWG twisted pair cable at different data rates. Using the system constraint of 500 kbps, we see the distortion is limited to the rounding of the signal pulse. If the data rate is increased further, the effects of jitter then become noticeable. In this case at 1 Mbps we begin to observe 5% jitter. At 3.5 Mbps we start to loose the signal completely and the quality of transmission is severely degraded. The maximum allowable jitter in a system should be limited to 5%. The causes of jitter are discussed in more detail in section 1.4.2.

RS-485 Signal Distortion vs Data Rate



TEST CONDITIONS

- 20 AWG Non shielded twisted pair cable. (Belden reference type 8205).
- 500 Metres
- Doubly terminated with 100 Ω
- SN75176B type transceiver at both ends.

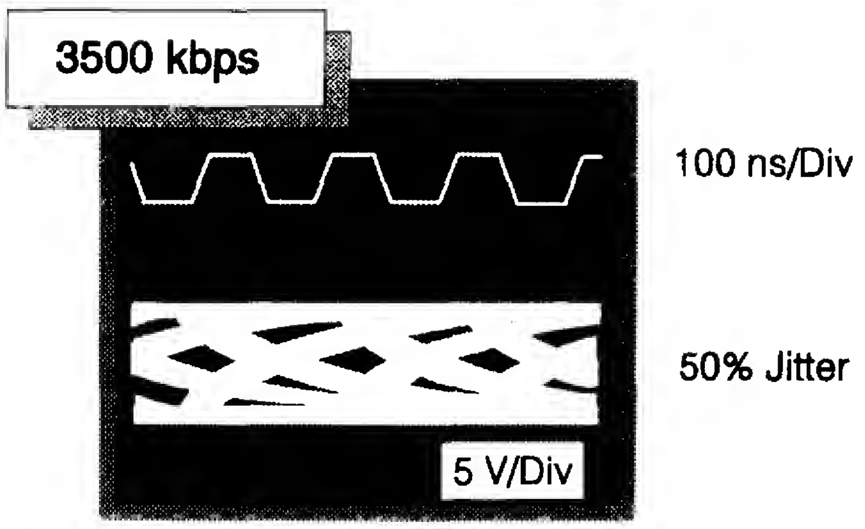


Figure 4.32 - RS-485 Signal Distortion vs. Data Rate

3.3.3 Line Termination

The behaviour of the transmitted signal and the integrity of the data at the receiving end depends upon the data rate and line length of the cable. There are two behavioural models; of a transmission cable:

i. **Lumped parameter model (Short wire)**

ii. **Distributed parameter model (Transmission line)**

The distributed parameter model models the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections and as a result the transmission line is said to have a characteristic impedance, Z_0. Z_0 is independent of distance along the line and represents the voltage and current relationship for an incident wave at any point as it travels along the line.

Transmission Line Test - Classification as a Lumped or Distributed Parameter Model

All cables can be thought of as transmission lines; but the term, transmission line, is used with differing meanings.

Consider a signal propagating down a simple data link comprising two wires. When the signal starts to change at the transmitter output the effect of this change will eventually be seen at the other end of the line. A reflection of the signal will occur, which will eventually return back to the transmitter terminals.

If this happens before the original transmitted signal has risen to its peak value then the line will normally be treated as a lumped parameter system rather than as a true transmission line. This is because the line itself does not greatly influence the performance of the system.

The test for whether a transmission line is to be considered as a distributed parameter model or a lumped parameter model is dependent upon the relationship of signal rise time, t_T, at the receiving end and the propagation time of the signal down the cable. The threshold between the two types of transmission line is given by the following equation:

$$2t_{pd} = t_T$$

If we build a margin of error into this equation a better test is to determine the relationship of twice the rise time to 5 times the propagation delay:

If the relationship $2t_{pd} \geq 5t_T$ is true then the transmission line must be treated as a distributed parameter model and terminated accordingly. If the converse i.e. $2t_{pd} \geq \frac{t_T}{5}$ is true. the transmission line can be treated as a lumped parameter model and termination is not necessary.

To determine t_T tests must be carried out on the transmission cable. For the purposes of this example we chose a low cost non shielded, twisted pair cable - 500 m of a Belden type 8205 cable as supplied by RS Components Ltd of the UK, reference number 360-964. On the driving and receiving ends we connected a SN75ALS176 single channel transceiver. The rise time at the receiver end measured :

t_T = 0.9 µs to the 10% and 90% points.

Assuming a propagation delay down the line of 5 ns/m, the time tpd = 500 x 5 = 2500 ns or 2.5 µs.

So in this case:

$5\ t_T$ = 4.5 µs and $2t_{pd}$ = 5 µs, so 2 tpd > 5 t_T and therefore the transmission line should be considered as having a distributed parameter model and consequently must be terminated in its characteristic impedance. In this case as we are using half duplex transmission the line must be terminated at the furthest ends.

To determine the characteristic impedance of the cable we used the technique described below in this case Z_0 measured 100 Ω.

Transmission Line Considerations and Effects

When the cable is operating like a transmission line, extra loads in the form of transmitters and receivers can be added, providing that they do not cause too great a shunting effect on the line. These extra loads, if they are evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. This extra load decreases the line impedance and reduces the speed of the signal along the line.

In the case of the lumped parameter model the line represents a pure fixed load to the transmitter device. For example, the capacitance of the line will be modelled as a fixed value which effectively limits the output voltage slew rate of the transmitter (assuming it can supply a finite amount of current to the line).

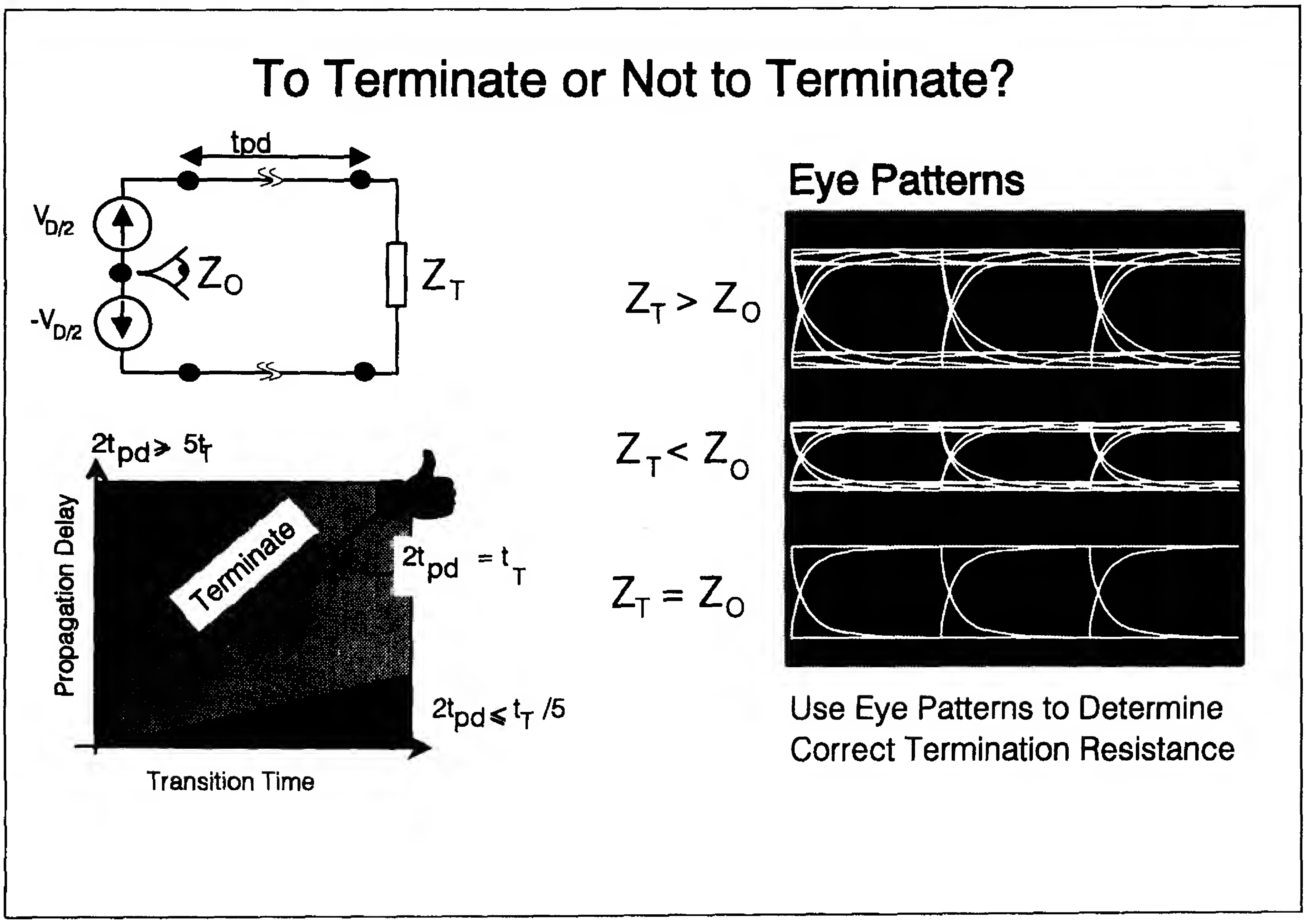

To Terminate or Not to Terminate?
tpd
$V_{D/2}$
$-V_{D/2}$
Z_O
Z_T
$2t_{pd} \geq 5t_T$
Propagation Delay
Terminate
$2t_{pd} = t_T$
$2t_{pd} \leq t_T/5$
Transition Time
Eye Patterns
$Z_T > Z_O$
$Z_T < Z_O$
$Z_T = Z_O$
Use Eye Patterns to Determine Correct Termination Resistance

Figure 4.33 - To Terminate or Not to Terminate?

Transmission Line Reflections

Consider a driver circuit driving the line. When the driver output voltage changes state, the driver appears to see the effective characteristic impedance of the line, Z_O. This will cause the voltage at the output of the driver circuit to reduce as a result of the potential divider action formed by Z_O and the driver circuit output impedance, Z_D.

At any point along the line the ideal source impedance will appear as Z_O and the ideal load impedance will also appear as Z_O. This gives the impression that the line is being driven by a voltage source of twice the magnitude of the line voltage.

When the signal reaches the receiving end of the line it sees a terminating impedance equal to the impedance (Z_O) of the line that it is already travelling on. It interprets this as a continuation of the line. The voltage on the line will not alter and the current flowing along the line will flow through the termination resistor and back to the driver via either ground or the other line in the system. Operation of the circuit as just described would result in optimum data transmission efficiency, with little or no signal reflections. However, circuit operation in the real world is not always so perfect.

If the termination impedance is dis-similar to the characteristic impedance of the line itself, the voltage at the termination point will alter. The voltage at the termination point is dependent on the relative size of the termination impedance to the line impedance. If the termination impedance is higher than the line impedance, the line voltage will increase causing a positive voltage reflection of the signal. When the termination impedance is lower than the line impedance, the line voltage will decrease leading to a negative reflection. The same effect will occur at the driver output terminals due to impedance mismatches between driver and line.

Reflections at each end of the line will eventually settle and leave a constant dc voltage on the line. The value of this voltage is equal to the ideal open circuit output voltage multiplied by the termination impedance divided by the sum of the driver output impedance and termination impedance.

Reflections as described can cause problems when driving lines at high frequencies. False receiver triggering can occur and repeated signal reflections will cause signal wave distortion.

Using Eye Patterns to Determine Z_O

Referring back to eye patterns, these can also be used to find the characteristic impedance of a transmission line. Figure 4.33 shows three sets of eye patterns, $Z_T > Z_O$, $Z_T < Z_O$, and $Z_T = Z_O$, where Z_T is 200 Ω, 50 Ω, and 100 Ω, respectively. Where $Z_T > Z_O$ the signal is larger with multiple traces, while with $Z_T < Z_O$ the signal is similar but much reduced in amplitude and could cause signal to noise ratio problems at the receiver. With $Z_T = Z_O$, the signal is very clear with a near perfect eye pattern. In practice it is possible to use a variable resistance and the eye pattern to determine the correct termination impedance for zero reflections.

3.3.4 Fault Protection and Fail Safe Operation

Fault Protection

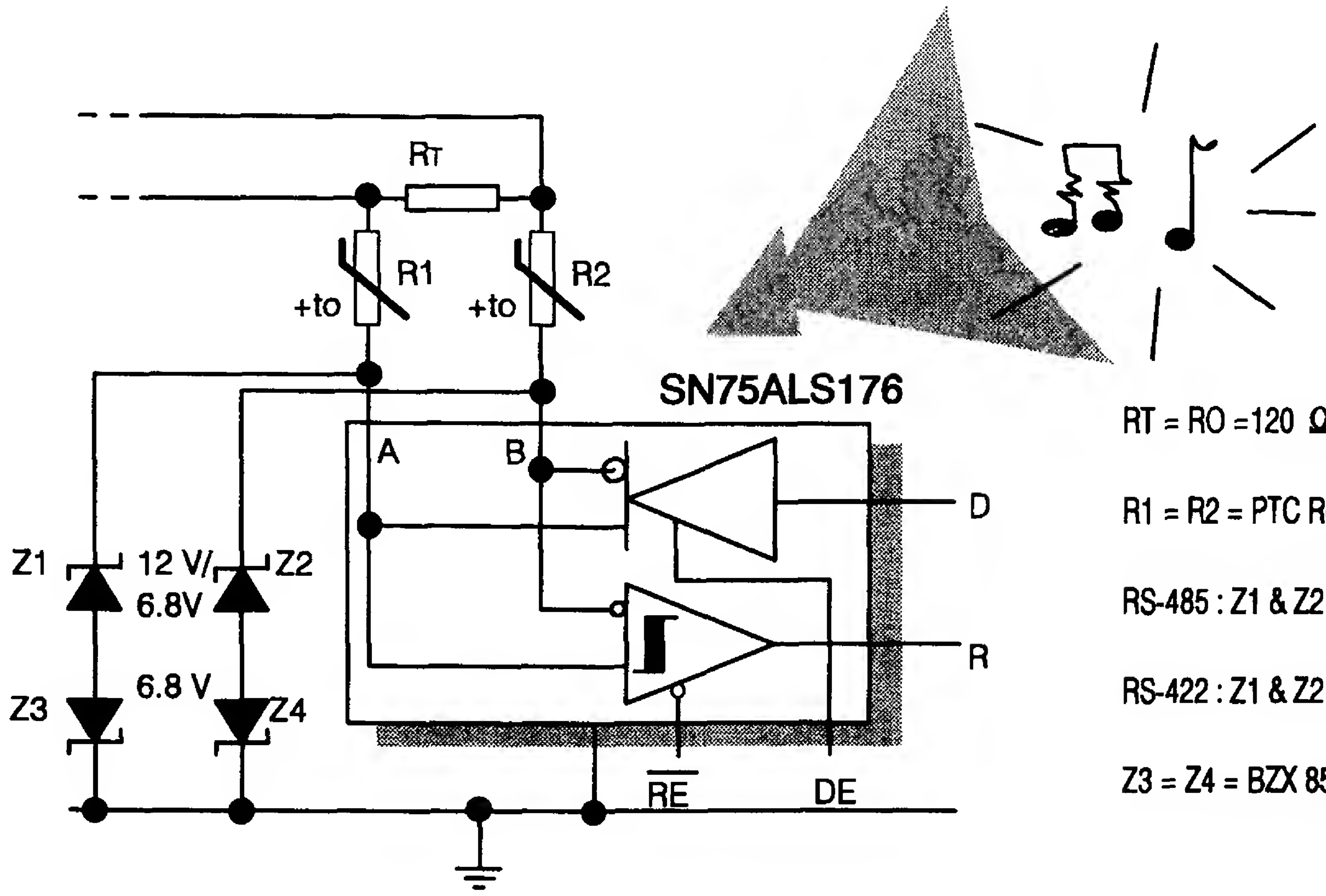
Factory control applications generally require protection against excessive noise voltages. The noise immunity afforded by the differential transmission scheme, and in particular the wide common mode voltage range of RS-485 can be insufficient. Protection can be accomplished in a number of ways, the most effective being through galvanic isolation which we will discuss later. Galvanic isolation provides system level protection but does not necessarily limit the voltages induced on the transmission lines with respect to the RS-485 driver/receiver grounds. This can be accomplished by the use of protection diodes.

Figure 4.34 shows how external diodes offer transient spike protection for the SN75ALS176 RS-485 transceiver.

R_T is the usual termination resistance and is equivalent in value to the characteristic impedance of the line. Positive Temperature Coefficient resistors, R_1 and R_2, provide current limiters for the diode chain. Provided their ambient temperature resistance is kept below 50Ω they will be transparent during normal usage and will not alter the termination value or attenuate the driver output voltage.

Z_1 and Z_2 are chosen to protect the input from positive spikes greater than 12 V for RS-485 and 6.8V for RS-422 whilst Z_3 and Z_4 protect the device from negative going spikes greater than -6.8 V.

Input Protection for Noisy Environments



RT = RO =120 Ω

R1 = R2 = PTC Resistor

RS-485 : Z1 & Z2 BZX 85 Rated @ 12V

RS-422 : Z1 & Z2 BZX 85 Rated @ 6.8V

Z3 = Z4 = BZX 85 Rated @ 6.8V

Figure 4.34 - Input Protection for Noisy Environments

Fail Safe Operation

The feature of fail safe protection is also a requirement in many RS-485 applications, however its usefulness needs to be considered and understood at an application level.

The Need For Fail Safe Protection

In any party line interface system, with multiple driver/receivers, there will be long periods of time when the driving devices are in-active. This state known as line idle and occurs when the drivers place their outputs into a high impedance state. During line idle, the voltage along the line is left floating, i.e. indeterminate - neither logic high or logic low. As a result the receiver could be falsely triggered into either a logic high or logic low state, depending upon the presence of noise and the polarity of the floating lines. This is obviously undesirable as the circuitry following the receiver could interpret this as valid information. The receiver should be able to detect such a situation and place its outputs into a known, and pre-determined state. The name given to methods which ensure this condition is called **fail safe**. An Additional feature which a fail safe should provide is to protect the receiver from shorted line conditions which can again cause erroneous processing of data and/or receiver damage.

There are several ways implement a fail safe, including a hard-wired fail safe using line bias resistors or protocols. Protocols, although complicated to implement, are the preferred method. However since most system designers, hardware designers in this case, prefer to implement such functions in hardware a hard-wired fail safe is often implemented.

A hard wired fail safe should provide a defined voltage across the receiver's input regardless of whether the line is shorted to either supply rail or is left open circuited. The fail safe should also be incorporated into the line termination if present when at the extremes of the line.

Internal Fail safe

Manufacturers have gone part way to facilitating fail safe design by including some form of open line fail safe circuitry within the integrated circuits. Unfortunately, due to power consumption constraints, the extra circuitry has proved of little use. The extra circuitry is quite often just a large pull-up resistor on the non-inverting receiver input, and a large pull-down resistor on the inverting input of the receiver. These resistors are normally in the range of 100 kΩ, and so when used in conjunction with line termination resistors to form a potential divider, only a few millivolts are generated. As a result this voltage (receiver threshold voltage) is insufficient to switch the receiver. To use these internal resistors effectively means no line termination resistors can be used, which reduces the allowed reliable data rate enormously.

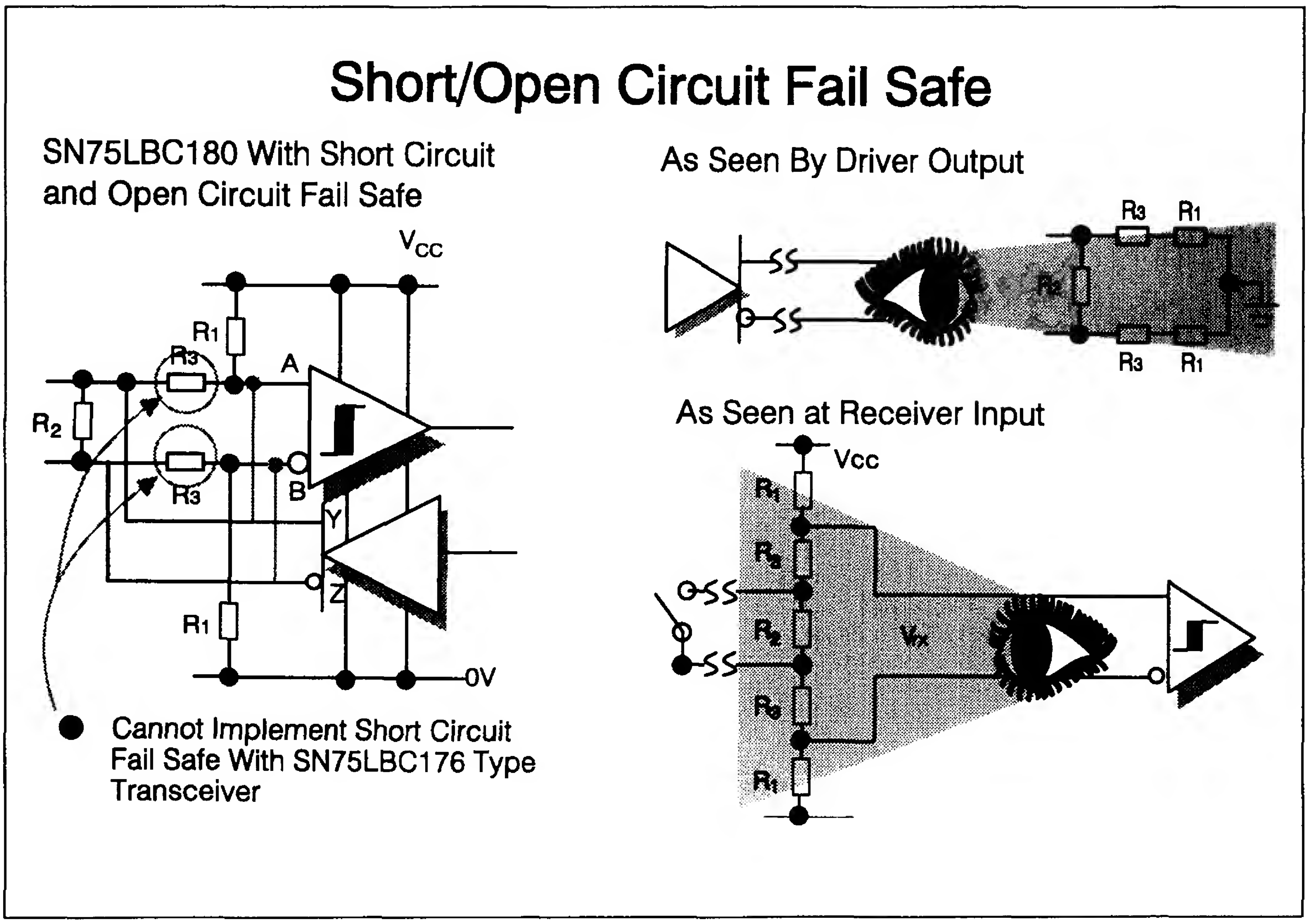

Short/Open Circuit Fail Safe
SN75LBC180 With Short Circuit and Open Circuit Fail Safe
Vcc
R1
R3
A
R2
R3
B
Y
Z
R1
0V
● Cannot Implement Short Circuit Fail Safe With SN75LBC176 Type Transceiver
As Seen By Driver Output
R3 R1
R2
R3 R1
As Seen at Receiver Input
Vcc
R1
R3
R2
R3
R1
Vx

Figure 4.35 - Short / Open Circuit Fail Safe

External Fail safe-Open Line Conditions

A more reliable way of offering open line fail safe is to use external pull-up and pull-down resistors. There two basic ways of doing this; one way is to polarise the line with the pull-up/pull-down resistors and use these resistors to match the line impedance. Another way is to use larger polarising resistors while using an extra resistor to terminate the line. The first idea has one advantage in that it provides a low impedance path to an ac. ground, so that any currents induced on to the line have a low impedance path to ground. However a problem is encountered with this method because the driver output now has to drive very much lower impedance's. If the driver output current capability is poor the device could easily go into output short circuit current limit. The second way, although requiring an extra resistor will not load the driver's output to such an excess.

Placing external pull-up and pull-down resistors R_1 on the non-inverting and inverting inputs of the receiver will produce open circuit fail safe. Terminating the transmission line with its characteristic impedance, Z_0, produces a potential divider between $2R_1$ and Z_0. The voltage formed across the line, V_{oc}, equals

$$V_{oc} = V_{cc} \times \frac{Z_0}{2R_1 + Z_0}$$

Devices meeting the RS-485 receiver threshold voltage specifications require V_{oc} to be greater than 200 mV. From this the relationship of R_1 to Z_0 can be derived:-

$$R_1 = Z_0 \times \frac{1}{2} \times \frac{V_{cc} - V_{oc}}{V_{oc}}$$

With $V_{cc} = 5V$, $V_{oc} = 200$ mV and $Z_0 = 100\ \Omega$, yields $R_1 = 1.2\ k\Omega$.

Biasing the receiver in this way will only provide open line fail safe, it will not provide shorted line fail safe. However, when using transceivers, like the SN75LBC176, it is not possible to provide shorted line fail safe configurations, since the driver output and receiver input are connected internally. Hence for devices like the SN75ALS176 and SN75LBC176 this open line configuration is the optimum fail safe available.

External Fail safe-Shorted Line Conditions

To implement protection from the shorted line condition, further resistors are required. When the line is shorted the transmission line's impedance goes to zero and the termination resistors will also be shorted. Putting extra resistors in series with the input to the receiver can provide shorted line fail safe protection.

The extra resistors, R_3 in figure 4.35, can only be added when using devices with separate driver outputs and receiver inputs. So internally wired transceivers cannot be used to offer shorted line fail safe. If this form of protection is required then a device such as the SN75LBC180, with its separate driver outputs and receiver inputs, should be used. If a transceiver type device was used then the extra resistors R_3 would cause extra attenuation of the output signal. The 'LBC180 will have its driver outputs fed directly to the line, bypassing resistors R_3.

Calculating the Resistor Values

If the line became shorted then R_2 would be removed leaving a voltage across the receiver inputs of:-

$$V_{rx} = V_{cc} \times R_3/(R_1 + R_3) \qquad \textbf{(a).}$$

For RS-485 applications the standard specifies V_{rx} to be greater than 200 mV. So

$V_{rx} = V_{th} = 200$ mV.

Using this figure, along with the minimum permissible supply voltage for the devices gives a relationship between R_1 and R_3.

When the line goes into a high impedance state the receiver will see the two R_3 in series with R_2 plus the two R_1's pulling up and down on either input. The receiver input voltage will now be:

$$V_{rx} = V_{cc} \times (R_2 + 2R_3)/(2R_1 + R_2 + 2R_3) \qquad \textbf{(b).}$$

Relating this new V_{rx} to the minimum specified in the standard, V_{th}, gives:

$$R_1 = \tfrac{1}{2} R_2 \times \left[\{(V_{cc} - \alpha V_{th})(V_{cc} - V_{th})\}/\{(\alpha - 1) V_{th} V_{cc}\}\right]$$

$$R_3 = R_2 \times (V_{cc} - V_{th})/V_{th}$$

$$\alpha = V_{co} / V_{rx}$$

Where α is the ratio of V_{oc}/V_{rx}

The transmission line will see an effective line termination resistance of R_2 in parallel with twice the sum of R_1 and R_3. This should match the transmission line's characteristic impedance, Z_0, therefore

$$Z_0 = 2R_2 \times \frac{R_1 + R_3}{2R_1 + R_2 + 2R_3} \qquad \textbf{(c)}$$

Combining equations **(a)**, **(b)** and **(c)** yields the following equations for R_1, R_2 and R_3:-

$$R_1 = \tfrac{1}{2} Z_0 \times \frac{(V_{cc} - V_{th})^2}{(\alpha - 1) V_{th} V_{cc}}$$

$$R_2 = Z_0 \times \frac{V_{cc} - V_{th}}{V_{cc} - \alpha V_{th}}$$

$$R_3 = \tfrac{1}{2} Z_0 \times \frac{V_{cc} - V_{th}}{(\alpha - 1) V_{cc}}$$

In this application assuming the supply voltage is 4.5 V and V_{th} = 200 mV with an a value α of 1.5 and driving a line with characteristic impedance of 120 Ω yields the following values:-

R_1 = 2.2k Ω

$R_2 = 120\ \Omega$

$R_3 = 110\ \Omega$

The values of R_1, R_2, and R_3 only apply for receivers at the extreme of the line; if there are more receivers on the line then fail safe can be accomplished by multiplying the values of R_1 and R_3 by half of the number of receivers on the line. This is done by assuming the input stages of all the receivers are the same, all R_1 resistors are the same, and that all R_3 resistors are the same Since all of R_1 and all of R_3 resistors will be in parallel, their overall resistance will be divided by half the number of receivers. If there is a large number of receivers on the line there is a danger of R_3 becoming too large and forming a large potential divider with the input resistance of the receiver, normally around 12 kΩ.

3.3.5 Galvanic Isolation

In the previous sections the need for line termination, receiver fail safe and noise protection was highlighted. All these elements can be found in an industrial process control and data collection application, which is shown in figure 4.36.

The capability of meeting toughened noise legislation is a key requirement for many new end products and applications. Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer, and a proven route to improved noise performance for any interface system is galvanic isolation.

Such isolation in data communication systems is achieved without direct galvanic connection or wires between drivers and receivers. Magnetic linkage from transformers provide the power for the system, and optical linkage provides the data connection. Galvanic isolation removes the ground loop currents from data lines and hence the impressed noise voltages which affect the signal are also eliminated. Common mode noise effects can be completely removed and many forms of radiated noise can be reduced to negligible limits using this technique.

For example consider the case in a process control system where the interface node, shown in figure 4.36, connects between a data logger and host computer via the RS-485 link. When an adjacent electric motor is started up, a momentary difference in ground potentials at the data logger and the computer may occur due to a surge in current. If no isolation scheme is employed for the data communication path, data may be lost during the surge interval and in the worst case damage to the computer could occur.

Circuit Description

The schematic shown forms an interface, one node, for a "distributed controlling, regulation and supervision (DCRS) system". Such a scheme could be used in a process control type application. Transmission takes place via a 2-wire bus, formed by a twisted-pair, shielded cable connected in a ring circuit.

capability. Low power is crucial in this type of application since many remote outstations will either be battery operated or require battery back-up capability.

Transceiver protection circuitry is formed by Z_1, Z_2, Z_3 and Z_4 along with current limiters PTC_1 and PTC_2 (see previous example). Line termination is formed by a combination of R_T, R_1 and R_2. The values of which can be calculated as follows;

$$R_1 = R_2 < 0.5 \times Z_O \times [1 + V_{CC}/V_{TH}]$$

and

$$R_T = Z_O\ [1 + V_{TH}/V_{CC}]$$

The bus driver used is the **SN75LBC176**, chosen for its low power consumption and high data rate Using a cable with a characteristic impedance of $Z_O = 120\ \Omega$ and a desired V_{TH} of 200 mV, requires $R_1 = R_2$ to be around 1.6 kΩ in value. The terminating resistor, R_T would be in the order of 124 Ω.

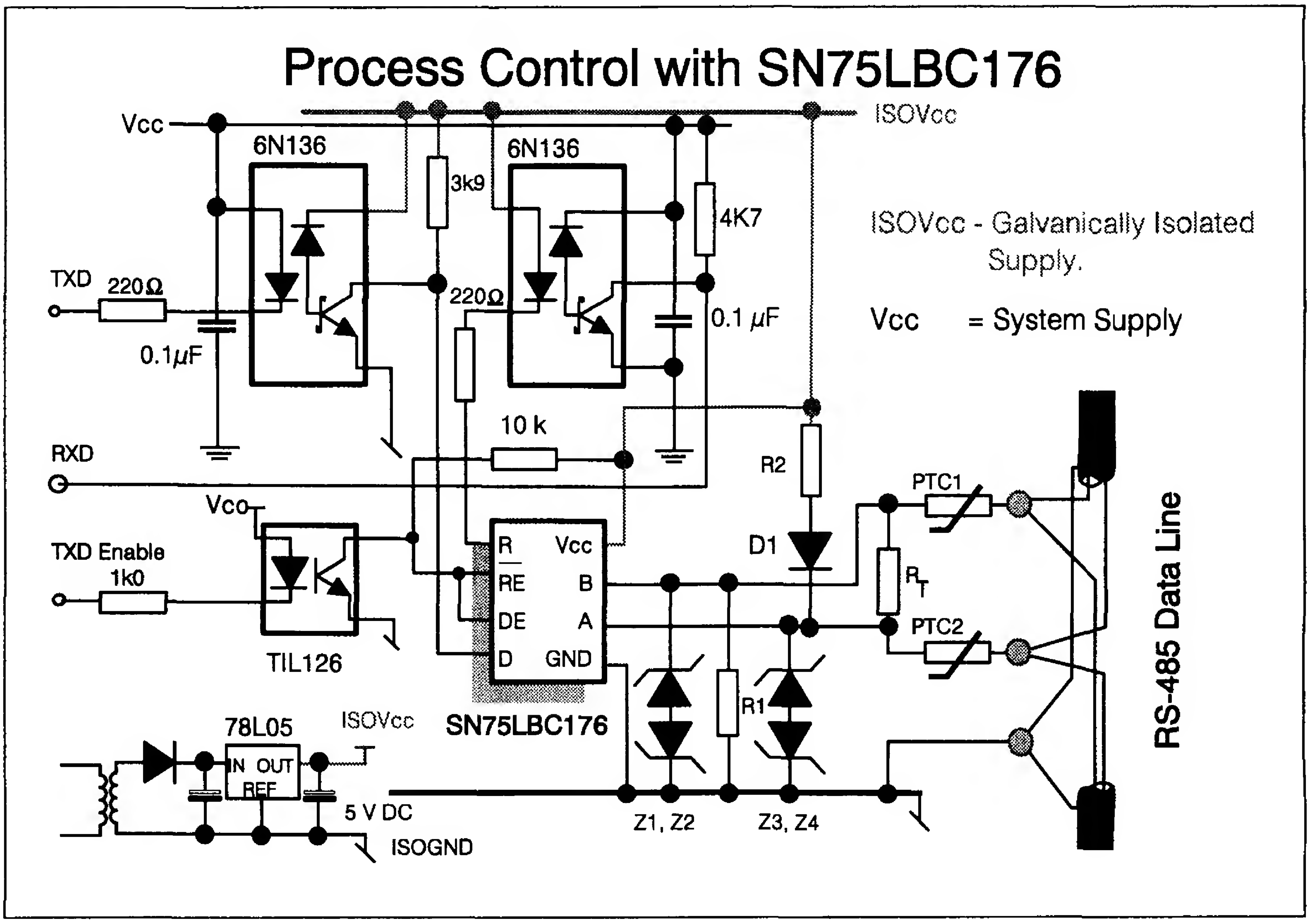

Process Control with SN75LBC176
Vcc
ISOVcc
6N136
6N136
3k9
4K7
ISOVcc - Galvanically Isolated Supply.
Vcc = System Supply
TXD 220Ω
220Ω
0.1 μF
0.1μF
10 k
RXD
R2
PTC1
Vcc
TXD Enable 1k0
R Vcc
RE B
DE A
D GND
D1
RT
PTC2
TIL126
RS-485 Data Line
78L05
ISOVcc
SN75LBC176
R1
IN OUT REF
5 V DC
ISOGND
Z1, Z2
Z3, Z4

Figure 4.36 Process Control SN75LBC176

The inclusion of $R_1 = R_2$, provides a receiver fail safe to open line conditions by biasing the polarity of the line to a logic '1' under line idle conditions. The values of $R_1 = R_2$ are best kept as low as possible to increase the noise rejection when the line is left floating, but they will place some loading onto the driver.

Galvanic isolation is afforded by means of three optocouplers/opto isolators. The 6N136 is chosen for its high data rate capability, $t_p = 75$ ns (max.), and its high voltage isolation.

The 6N136 is designed for use in high speed digital interfacing applications that require high voltage isolation between the input and output. Its use is highly recommended in extremely high ground noise and induced noise environments.

The 6N136 consists of a GaAsP light emitting diode and integrated light detector, composed of a photo diode, a high gain amplifier and a Schottky clamped open collector output transistor. An input diode forward current of 5mA will switch the output transistor low, providing an on state drive current of 13 mA (eight 1.6 mA TTL loads). A TTL input is provided for applications that require output transistor gating. Housed in a single 8-pin dual-in-line plastic package the 6N136 is characterised for operation over the temperature range of 0°C to 70°C. The internal Faraday shield provides a guaranteed common mode transient immunity of 1000 Vμs.

A 0.1 µF capacitor has been connected between V_{CC} and ground to improve switching performance.

3.4 Solving The Speed / Power Dilemma

3.4.1 LinBiCMOS™, the Technology of Choice

LinBiCMOS™ is based on Texas Instruments' highly successful LinCMOS process. LinCMOS is a 3 µm pure CMOS technology with 16 V capability, making it ideal for the design of low power analog products such as op-amps and analog-to-digital converters (many examples of which are discussed elsewhere in this book). By shrinking the geometry to 2 µm and adding a high performance 30 V bipolar structure, a new analog merged bipolar/CMOS technology has been produced.

Probably LinBiCMOS™'s greatest attribute is its modularity. When generating a new technology it is difficult to achieve a balance between performance and cost , as many "nice to have" features can make a process too expensive to address a wide range of opportunities. By making LinBiCMOS™ modular, only the process modules needed to address a particular application need be used, making it very cost effective. Modules available for LinBiCMOS™ include high speed NPNs (with an f_T of 3GHz compared with 500MHz for the standard transistor), double level metal for better logic integration and current handling, isolated high value polysilicon resistors and Schottky diodes for clamping.

Figure 4.37 shows the average supply current at the maximum data rate whilst conforming to the RS-485 standard for various transceivers using different technologies. Whilst the Advanced Low Power Schottky technology offers excellent speed performance the LinBiCMOS™ technology offers optimum speed performance combined with low power consumption

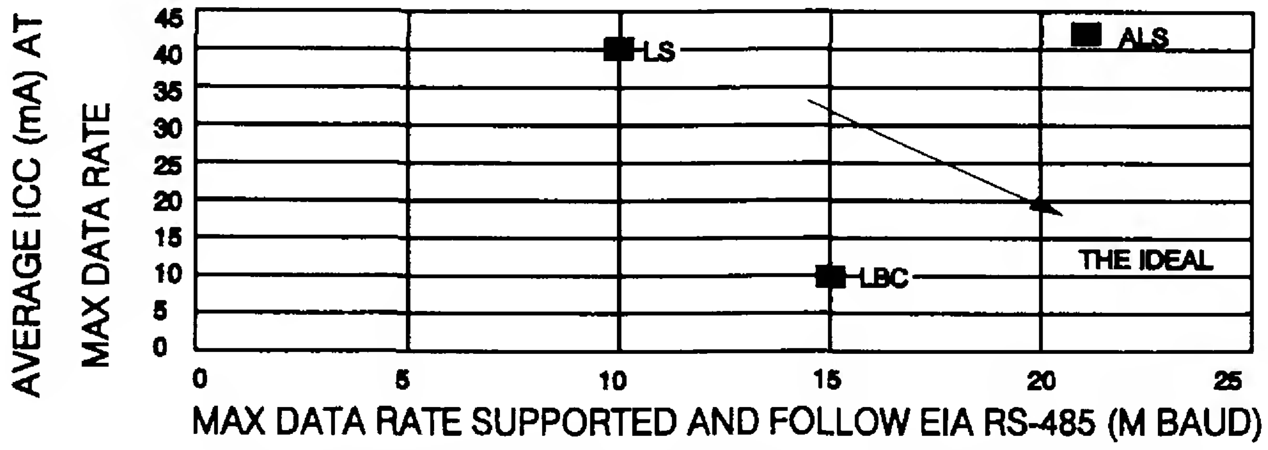
The Applications

With its high voltage capability and excellent switching speed LinBiCMOS™ is ideal to address standards such as RS-422 and RS-485. For example the RS-485 standard, demands that driver outputs can be shorted to +12V and -7V without damage. This is particularly difficult to implement as RS-485 devices are designed to operate from a single 5 V supply, meaning that parts of the chip must be designed to operate well outside its supply rails. Further more the "party line" nature of the standard requires devices that must be able to withstand contention (multiple drivers accessing the bus simultaneous) without failure. For this reason short circuit protection and thermal shutdown are built into the chip.

Improve MTBF

Reliable line interface circuits are crucial if the overall system mean time between failure (MTBF) is to be maximised. System designers have long been aware that often the weak link in ensuing system reliability has been line interface circuits. This vulnerability is due in part to the circuits close proximity to the outside world via the edge connector. Consequently interface circuits are particularly susceptible to failure from high external voltages caused by noise, ESD or incorrect insertion of cables. For this reason the technology of choice for many Texas Instruments emerging interface products is LinBiCMOS™.

The Speed / Power Dilemma : A Technology Review



The Technology Evolution in Device Terms

Trade Standard Footprint	First Generation Products	High Speed/Low Power Products	Function
AM26LS31	SN75172	SN75LBC172	QUAD DRIVER
MC3487	SN75174	SN75LBC174	QUAD DRIVER
SN75176	SN75176	SN75LBC176	TRANSCEIVER
MC34050	SN75ALS1177	SN75C1167	DUAL Rx/Tx

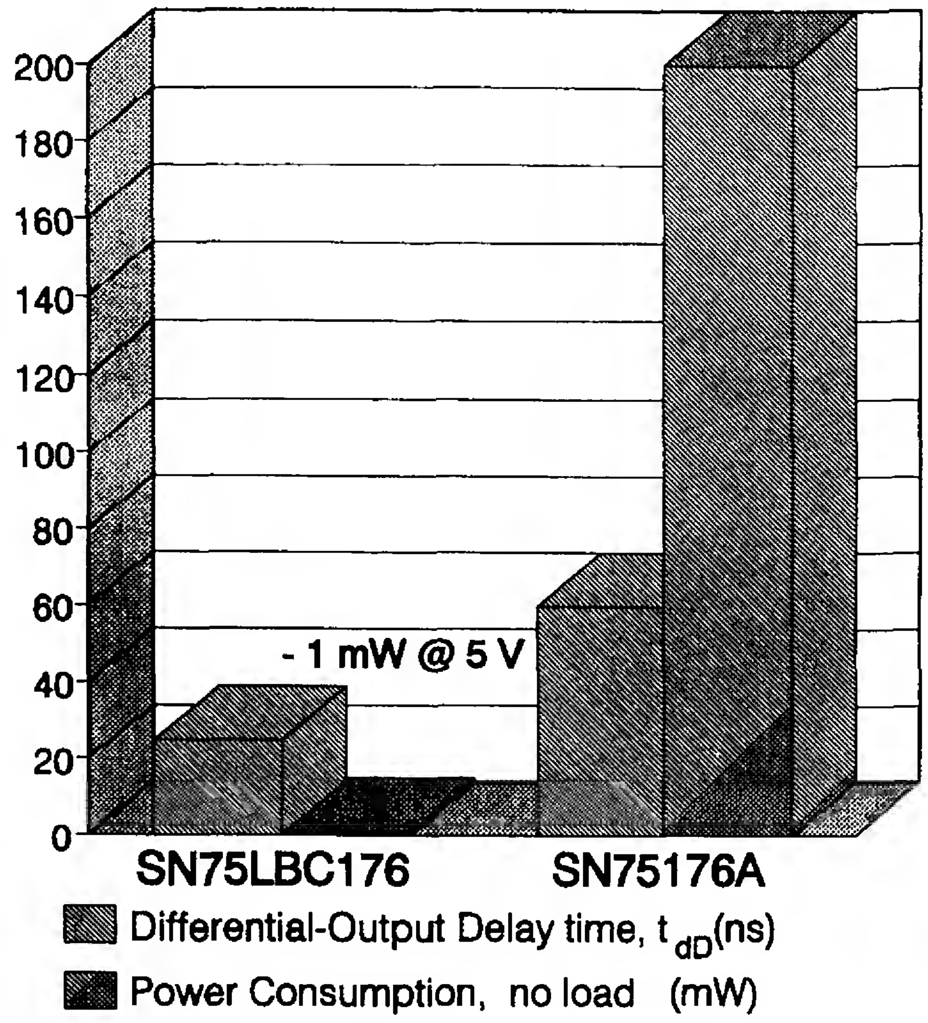
Figure 4.37 - Solving the speed / power dilemma

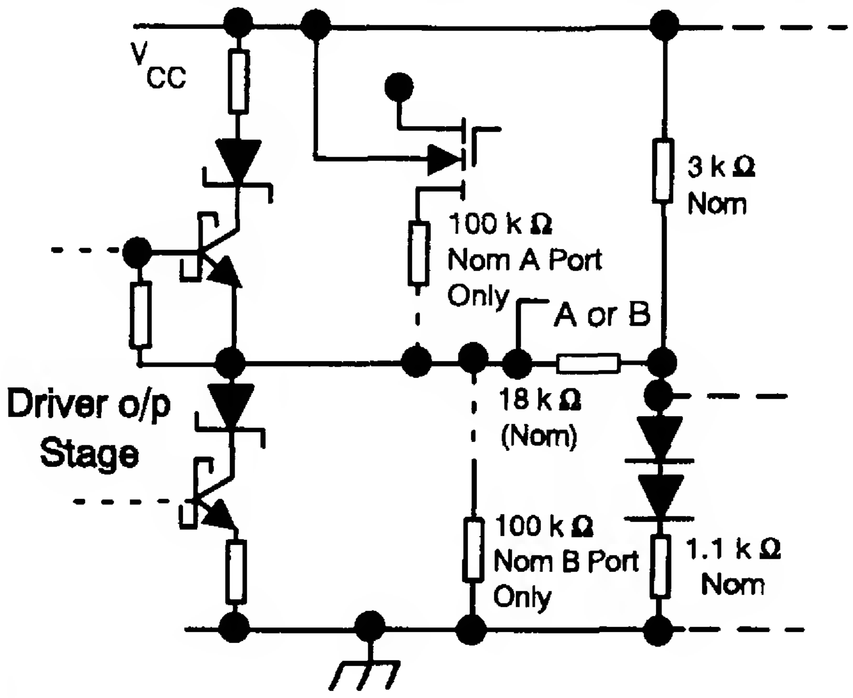
3.4.2. SN75LBC176; Ultra Low Power

The key feature of the SN75LBC176 is the very low power consumption, 1mW. Compare this to the consumption of the older generation SN75176A, where the quiescent power is as high as 200mW. Normally low power consumption signifies a reduction in ac performance. In the case of the 'LBC176 the ac performance is improved over the SN75176A. Data rates of greater than 10Mpbs are achievable while being conformant to the RS-485.

The standard SN75LBC176 is characterised for commercial temperature range applications. For more extreme conditions the SN65LBC176 extends the operating range to -40°C to +85°C.

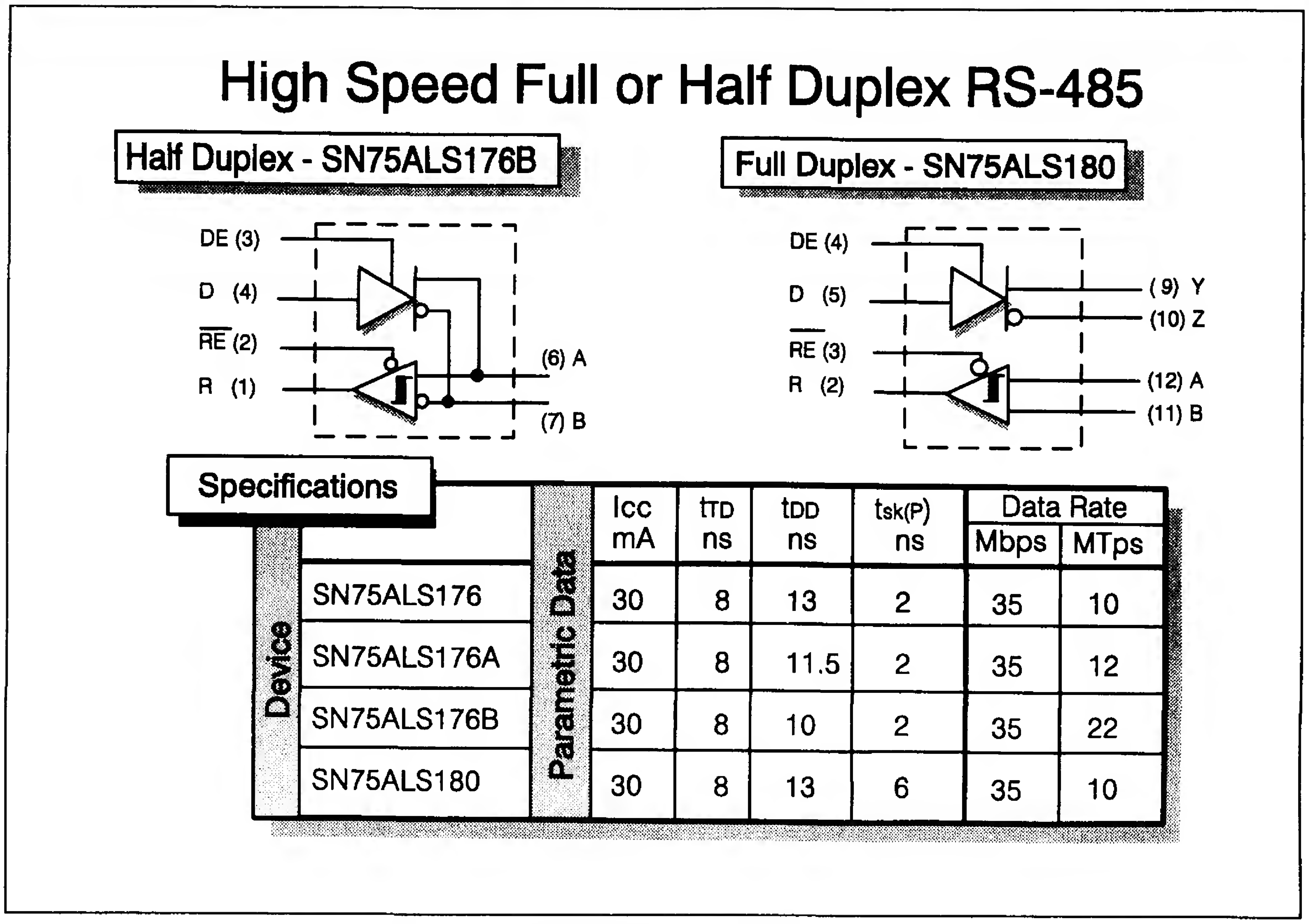
SN75LBC176; High Speed Low Power RS-485




V_{CC}
3 kΩ Nom
100 kΩ Nom A Port Only
A or B
Driver o/p Stage
18 kΩ (Nom)
100 kΩ Nom B Port Only
1.1 kΩ Nom

- Fully Meets EIA Standard RS-485
- Fabricated Using 2 µ LinBiCMOS™
- High Speed.......>10Mbps

Figure 4.38 - Low Power Consumption



High Speed Full or Half Duplex RS-485

Half Duplex - SN75ALS176B

Full Duplex - SN75ALS180

Specifications

Device	Icc mA	tTD ns	tDD ns	tsk(P) ns	Data Rate Mbps	Data Rate MTps
SN75ALS176	30	8	13	2	35	10
SN75ALS176A	30	8	11.5	2	35	12
SN75ALS176B	30	8	10	2	35	22
SN75ALS180	30	8	13	6	35	10

Figure 4.39 - High Speed Full or Half Duplex RS-485

3.4.2 Full Duplex and High Speed RS-485

In the process control example we discussed earlier, the key requirement has been for reliable data transmission over 500 metres of cable. The data rate under consideration was limited to 500 kbps however in many systems the data rate requirements are in excess of 10 Mbps. Cable length must be reduced accordingly as transmissions at this rate are only possible over short line lengths, <50 metres. We have discussed the SN75LBC176, however for speeds above 10 Mbps we must look towards a technology which is more well suited for high speed applications.

Advanced Low Power Schottky technology provides the key to the quest for speed. The SN75ALS176 utilises the true benefits of ALS pushing the data rate to over 35 Mbps. For synchronous systems where skew limits are critical, the SN75ALS176B facilitates 22 MTps (Million Transfers per second). This is the highest speed RS-485 transceiver on the market today.

The SN75ALS176, like the SN75176, DS3695, TL3695, is of a transceiver configuration. As shown in figure. 4.32, the transmit and receive pins are accessible through pins 6 and 7 only. With this configuration communication is limited to half duplex only. For quasi-full duplex operation, using two separate RS-485 lines, one must use a device like the SN75ALS180. this device allows separate lines to be connected to both the receiver and driver. The 'ALS180 has similar performance to the 'ALS176 facilitating up to 35 Mbps.

3.4.3. High Speed and Low Power Operation for RS-422

The benefits of use of technology can also be seen in the release of devices that support the RS-422 standard. The SN75C1167/68 are dual differential drivers and receivers designed using LinBiCMOS™ and the SN75ALS1177/8 are dual differential drivers designed using Advanced Low Power Schottky technology. The maximum power consumption for the ALS devices is 262mW from a 5V Vcc and for the LinBiCMOS™ devices is only 33mW. The T_{PLH}/T_{PHL} for the receiver section is 37ns for the ALS devices and 27ns for the LinBiCMOS™ devices. Therefore the combination of the low power consumption and the excellent speed performance of the LinBiCMOS™ technology can be seen.

The comparison between the LinBiCMOS™ technology and the Low Power Schottky technology can be seen comparing the AM26LS3X family of quad differential line drivers and receivers and the AM26C3X family of LinBiCMOS™ quad differential line drivers and receivers. The maximum power consumption for the LS devices is 420mW and for the LinBiCMOS™ devices is 77mW. The T_{PLH}/T_{PHL} for the receivers is 30ns for the AM26C32 devices compared with 35ns for the AM26LS32.

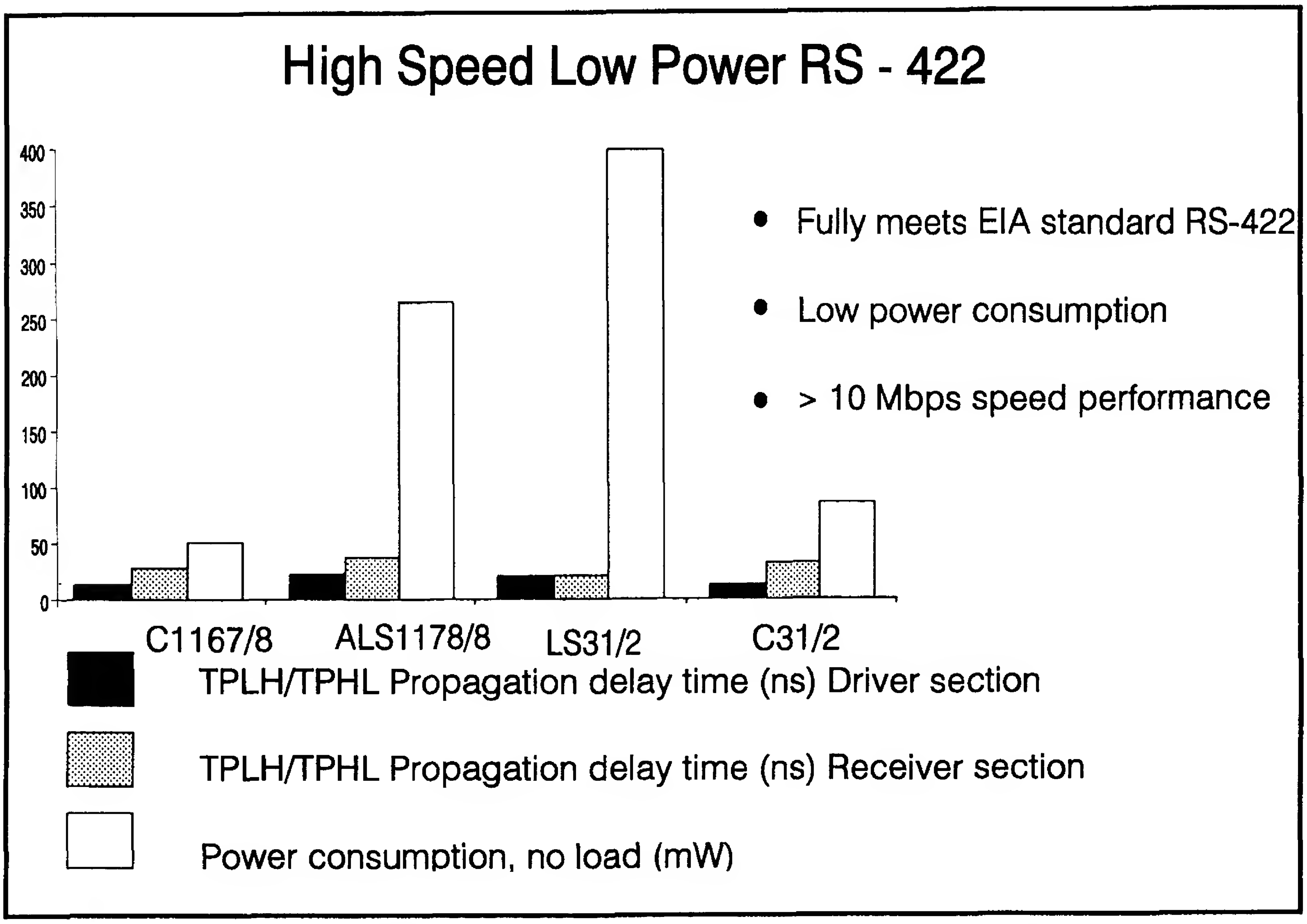


Figure 4.40 - High Speed and Low Power demonstrated by RS-422 products

3.4.4 RS-485 Selection Guide

In this section we have concentrated on the single transceiver type function. TI does however support a wide range of parts compliant with the RS-485 standard in various configurations and multiples. The below selection guide is provided for convenience. The reader is advised to consult the Data Transmission Circuits Data Book (Reference SLLD001) for the latest technical specifications.

RS-485 Data Transmission Circuits

Device	Devices	Device	Key
Line Drivers	4	SN75172	Industry Standard
		SN75174	Industry Standard
		SN75ALS172	High Speed
		SN75ALS174	High Speed
		SN75LBC172	High Speed / Low Power
		SN75LBC174	High Speed / Low Power
Line Receivers	4	SN75173	Industry Standard
		SN75175	Industry Standard
		SN75ALS173	High Speed
		SN75ALS175	High Speed
		SN75LBC173	High Speed / Low Power
		SN75LBC175	High speed / Low Power
Line Transceivers (Drivers / Receivers)	1	SN75176A	Reduced Slew-rate
		SN75176B	Industry Standard
		SN75177B	Industry Standard Repeater
		SN75178B	Industry Standard Repeater
		SN75ALS176	High Speed
		SN75ALS176A	Very High Speed
		SN75ALS176B	Ultra High Speed
		SN75LBC176	Ultra- Low Power
	1/1	SN75179B	Industry Standard
		SN75LBC179 ¥	High Speed / Low Power
		SN75ALS180	Full Duplex Communication
		SN75LBC180 ¥	High Speed / Low Power
		SN75ALS181	Full Duplex Communication
	2/2	SN751177	High Speed
		SN751178	High Speed
		SN75ALS1177	High Speed
		SN75ALS1178	High Speed
		SN75ALS170	High Speed
	3/3	SN75ALS171	High Speed
		SN75ALS1711	High Speed
	9/9	SN75LBC976	Low Power
		SN75LBC978	Low Power with WRAP

Notes

¥ Product currently under development, contact TI representative for further details.

3.5 Defining the Maximum Operating Speed in a Parallel Communication system

For multi channel systems consideration of the drivers differential transition time is not sufficient to determine the systems data rate capability. More specifically the difference in time between the slowest path and the fastest path within the system will set the limit.

There are many categories of delay in a differential system. This understanding is further complicated when you consider that a driver is really a single ended input to a differential output converter, while the receiver is a differential input to a single ended converter.

The propagation delay time is the time measured between the 50% level of the input pulse and the 50% level of the single ended output pulse. t_{PD}.

The differential propagation delay time is the time measured between the 50% level of the input pulse and 50% level of the differential output pulse t_{dD}.

The pulse skew of the driver is defined as the difference between the maximum differential propagation delay time and the minimum differential propagation delay them. The pulse skew of the receiver is defined as the difference between the maximum propagation delay time and the minimum propagation delay time.

As a rule of thumb the minimum unit interval can be defined as the bit interval time that ensures that always 80% of this bit interval appears at the output. The output bit interval in the worst case can be considered to have the skew limit deducted from the output bit interval. Therefore arithmetically the minimum unit interval can be defined as

Minimum Unit Interval = 5 x (driver pulse skew + receiver pulse skew).

Hence the maximum operating speed of the communication system = 1 / Minimum Unit Interval

3.5.1 High Speed Differential Parallel Communication

The Small Computer Systems Interface has overcome the problem of ensuring the speed of communication is guaranteed across parallel channels by defining skew limits within the specification. Lets review how this solution has been implemented. But first let us review the SCSI standard.

The Small Computer Systems Interface is a parallel multimaster I/O bus that provides a standard interface between computers and peripheral devices. The SCSI bus offers two distinct features : single ended SCSI - where each signal's logic level is determined by the voltage of a single wire relative to a common ground and differential SCSI in which the level is determined by the potential difference between two wires. Differential transmission is more robust and less susceptible to electrical noise.

The SCSI specification states that the single ended bus cannot be more than 6 metres long and should be used to connect devices with the cabinet only. A differential bus can be up to 25 metres long and can be used to connect devices in different cabinets.

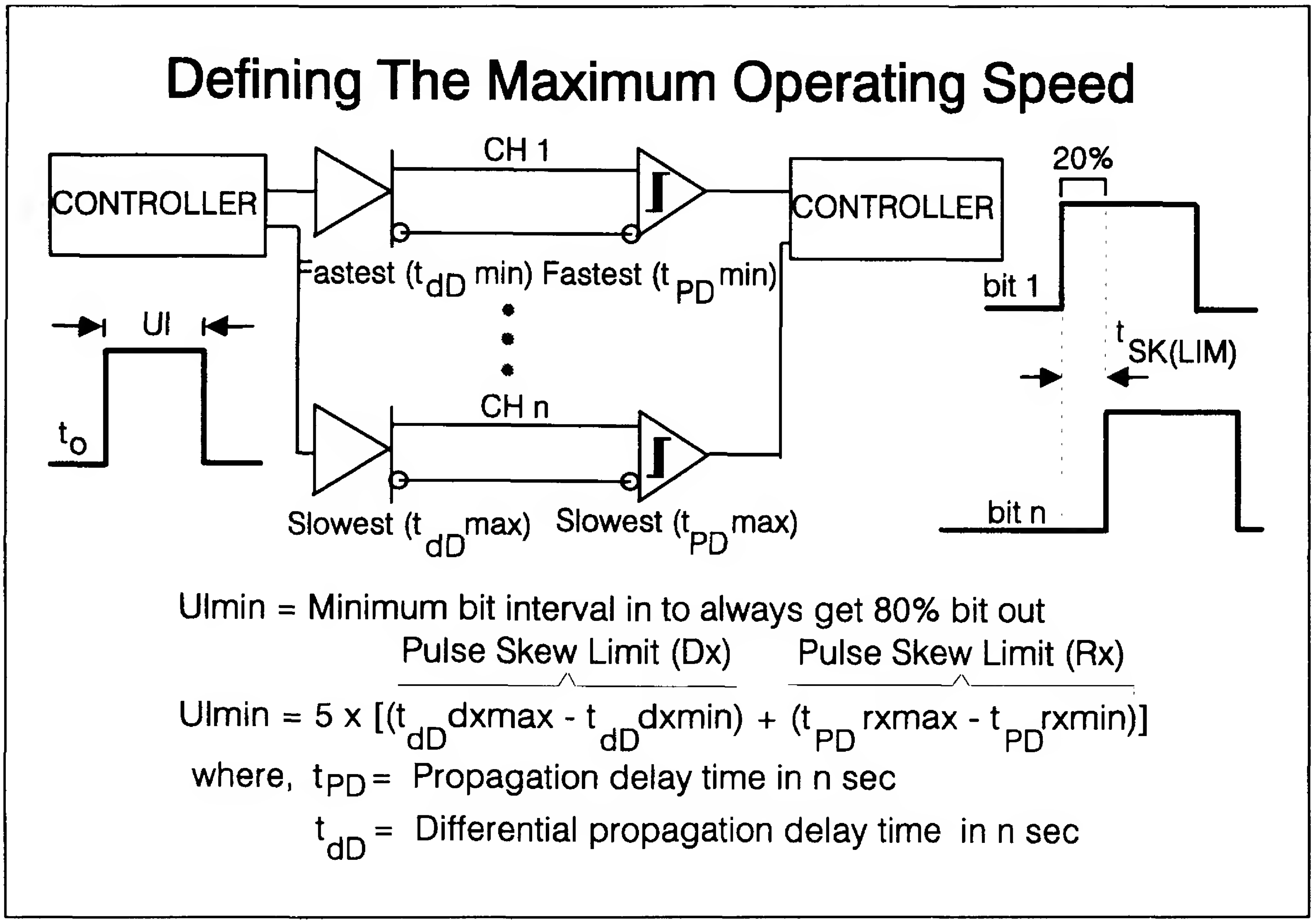

Defining The Maximum Operating Speed
CH 1
CONTROLLER
CONTROLLER
20%
Fastest (tdD min) Fastest (tPD min)
bit 1
UI
tSK(LIM)
to
CH n
Slowest (tdD max) Slowest (tPD max)
bit n
UImin = Minimum bit interval in to always get 80% bit out
Pulse Skew Limit (Dx)
Pulse Skew Limit (Rx)
UImin = 5 x [(tdDdxmax - tdDdxmin) + (tPDrxmax - tPDrxmin)]
where, tPD = Propagation delay time in n sec
tdD = Differential propagation delay time in n sec

Figure 4.41 - Defining the Maximum Operating Speed

By the parallel nature of the interface, data can be transferred over the cable more than one bit at a time. SCSI allows 8-bit (one Byte) or a 16-bit (one word) data width and transfers as often as once every 100 ns or 10 million transfers per second.

Since the logical state of any one bit can change every 100 ns, this defines a period during which the logical state should be valid across the bus. This is the unit Interval (UI). The voltage transitions which define the start and end of the UI can propagate along the bus at different velocities due to the physical differences along each electrical path. So the original UI at the start will be different at the destination.

Time variation of the defining voltage transitions is typically called skew. The limit for skew, designated $t_{sk(lim)}$, is the fastest minus the slowest propagation delays along any part of the bus. This, in effect, will reduce the UI by $t_{sk(lim)}$ establishing a minimum unit interval, UI_{min}, that can be transmitted with a particular data bus.

The proposed SCSI-3 standard for fast transfers (10 MTps), defines UI_{min} in terms of set-up and hold times at the SCSI connector for inter-operability with any other SCSI device. At the time this document is being written the requirements are as shown in figure 4.42.

The budget behind the connector is left to the designer and depends upon the SCSI controller, transceivers, and layout being used. The table shows some skew budget examples with various controller chips that would comply with the requirements at the SCSI connector. The column under 'Rec' (for recommended) is data for the worst case number for SCSI controllers surveyed by the SCSI SPI Working Group and budgets 8 ns for the external driver and 9 ns for the external receiver. This is the origin of the $t_{sk(lim)}$ specifications in the SN75LBC976 data sheet.

Parameter	Rec	Vendor A	Vendor B	Vendor C	Units
min Tx_controller_setup =	32	30	35	35	ns
min Tx_controller_hold =	42	42	45	45	ns
min Rx_controller_setup =	5	0	5	0	ns
min Rx_controller_hold =	15	20	15	10	ns
t_{sk_etch} =	1	1	1	1	ns
max t_{sk_dvr} =	8	6	11	11	ns
max t_{sk_rvc} =	9	4	9	14	ns

Transceiver Skew Budgets for Various SCSI Controllers

The time it takes one transceiver of the 'LBC976 to change logic states is called the propagation delay time. For a driver this is designated as t_{dD} and for a receiver t_{pd} and does not differentiate whether the logical transition is from high-to-low or low-to-high level. The $t_{sk(lim)}$ parameter for the transceiver is nothing more than the maximum difference of the propagation delay times between any two drivers or any two receivers on any two devices. Compliance to the $t_{sk(lim)}$ specifications of the data sheet and the recommendation of the SCSI standard is assured by measuring the propagation delay time of each channel of each 'LBC976 and accepting only those devices within the $t_{sk(lim)}$ band. To keep the production costs of the 'LBC976 reasonable, this testing is done at 25°C and at 70°C ambient temperatures at a V_{CC} of 5 volts.

Admittedly, the die temperatures and supply voltage are all the same (or nearly the same) during Texas Instruments' production testing and not necessarily the same would be seen in actual use. However the sensitivity of the propagation delay times to these factors is the same and repeatable from device to device. In other words, as long as the operating environment of all of the channels of the SCSI interface is similar, the change in propagation delay times from the data sheet conditions will be the same. This will maintain the $t_{sk(lim)}$ even though the actual propagation delay times may change.

It is nearly impossible to predict the instantaneous die temperatures of these devices in actual use. Due to the non-deterministic nature of the state of any one channel and the averaging affect of nine channels and of the package thermal time constant, the die temperature must be considered using the mean power dissipation. It is also reasonable to assume the mean power dissipation of separate devices on the same printed circuit board to be close to each other and the temperature of the air around them will not have a large (<5°C) gradient between the two. Even if there was an air temperature gradient of 45°C, there would be only about a 2 ns difference in the driver propagation delay times and, from recent data, little or no difference in the receiver propagation delay times. If such a temperature gradient actually existed across a board, it' is likely that skew budgets are not going to be the problem with the equipment!

In summary:

1. The designer should determine the transceiver skew requirements based upon his controller and board design.

2. The current specification and testing of $t_{sk(lim)}$ of the 'LBC976 is, the best compromise for a cost effective solution.
3. We have application information from our experience gained through numerous users with no inter-operability problems detected at the time of writing.

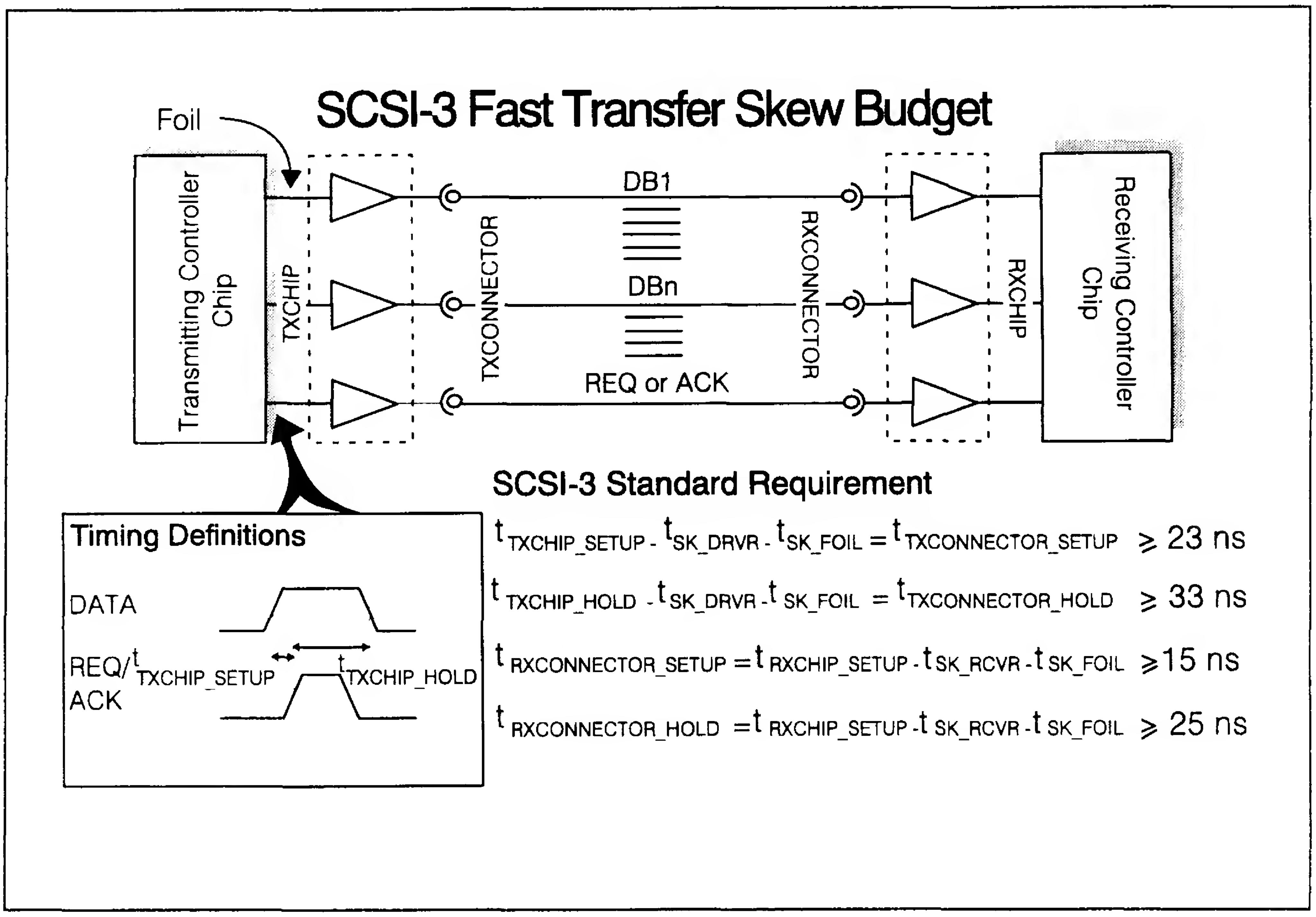

SCSI-3 Fast Transfer Skew Budget
Foil
Transmitting Controller Chip
TXCHIP
TXCONNECTOR
DB1
DBn
REQ or ACK
RXCONNECTOR
RXCHIP
Receiving Controller Chip
Timing Definitions
DATA
REQ/ACK
t_{TXCHIP_SETUP}
t_{TXCHIP_HOLD}
SCSI-3 Standard Requirement
$t_{TXCHIP\_SETUP} - t_{SK\_DRVR} - t_{SK\_FOIL} = t_{TXCONNECTOR\_SETUP} \geqslant 23$ ns
$t_{TXCHIP\_HOLD} - t_{SK\_DRVR} - t_{SK\_FOIL} = t_{TXCONNECTOR\_HOLD} \geqslant 33$ ns
$t_{RXCONNECTOR\_SETUP} = t_{RXCHIP\_SETUP} - t_{SK\_RCVR} - t_{SK\_FOIL} \geqslant 15$ ns
$t_{RXCONNECTOR\_HOLD} = t_{RXCHIP\_SETUP} - t_{SK\_RCVR} - t_{SK\_FOIL} \geqslant 25$ ns

Figure 4.42 - SCSI-3 Fast Transfer Skew Budget

3.5.2 SN75LBC976DL; Two Chip Differential SCSI

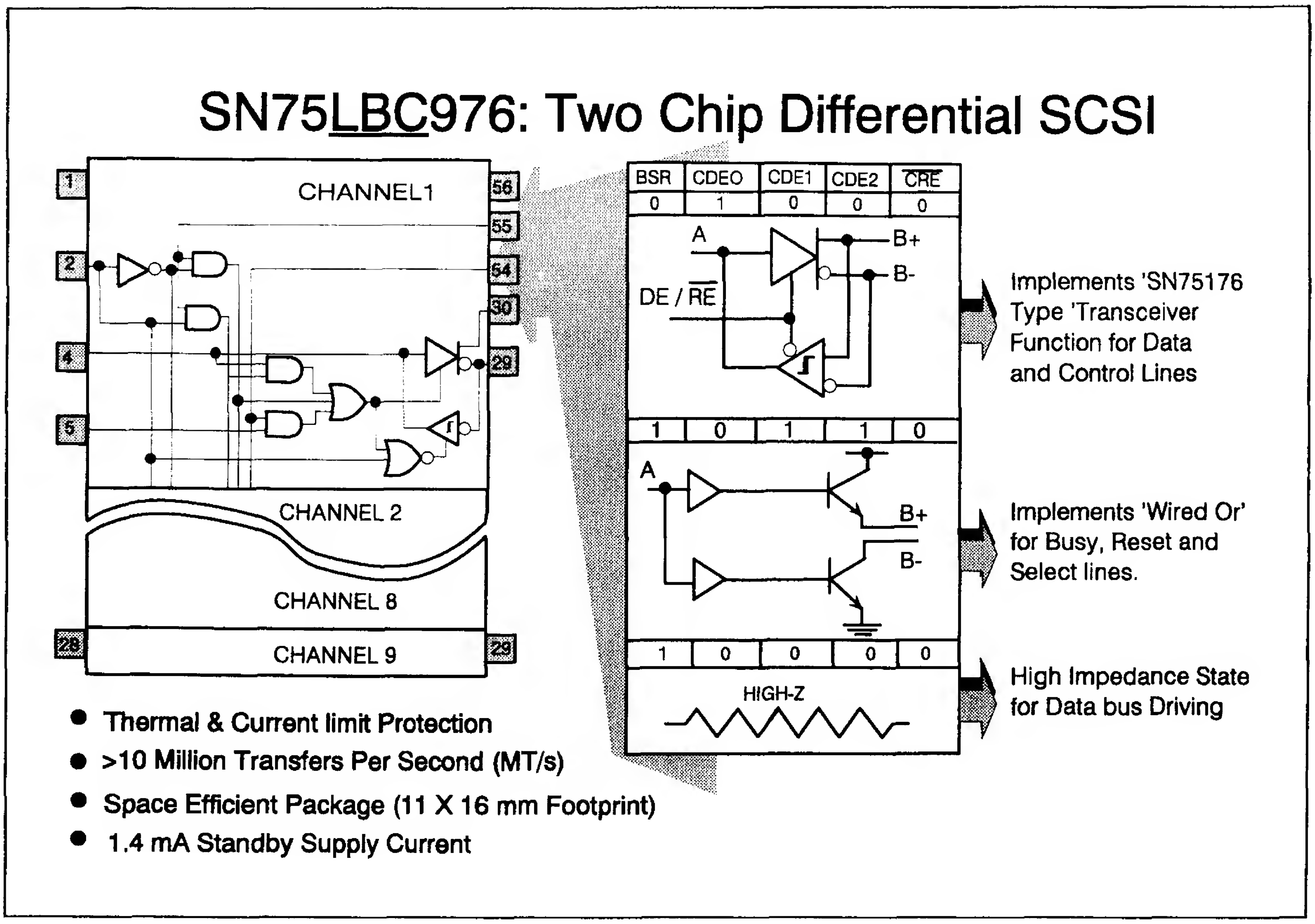
Much debate has taken place on differential versus single ended SCSI for data rates above 5 million transfers per second (MTps). It is clear however, that for data rates approaching 10 MTps and at line lengths in excess of 6 metres, differential SCSI is essential.

As we discussed earlier, the standard 8-bit interface is made up of 8 data lines, one parity bit, and 9 control lines, making 18 channels in total. The only differential transceivers capable of transmitting at 10 MTps data rate have utilised the LS and ALS technologies. Using these technologies and considering the 18 transceivers per interface the power consumption is quite considerable, 2.4 W with all drivers disabled. Turn the drivers on and the power consumption rises to nearly 4 W.

From a designers viewpoint, 2.4 watts is a considerable amount of heat to remove from a system. This is evident in the case of compact hard disk drives where shear equipment size is the limiting element. A further factor is board area, using one discrete transceiver per channel, i.e. 18 8-pin SO packages, is unacceptable for many applications.

From a semiconductor designers viewpoint integrating a number of transceivers is of course possible however the limiting factor once again is power dissipation. The

SN75LBC976 is designed to overcome both the problems of power dissipation and integration. The device incorporates on a single IC, nine RS-485 configurable transceivers each capable of transmitting at 10 MTps. This is made possible using LinBiCMOS™ technology. With all drivers disabled the quiescent power consumption of the 'LBC976 is a mere 1.5 mW, with all drivers enabled the quiescent consumption rises to 45 mW, a considerable saving over LS and ALS parts. The package size has also been reduced to a minimum using the 0.635 mm pitch 56 pin SSOP package which reduces board area significantly compared with alternate packages such as PLCC. The reader should note that irrespective of the device power, there is still the relatively high line current. The SSOP package has been thermally enhanced to handle this level of power dissipation. We will cover this point later as we look at the thermal characteristics of the package.



SN75LBC976: Two Chip Differential SCSI

Implements 'SN75176 Type 'Transceiver Function for Data and Control Lines

Implements 'Wired Or' for Busy, Reset and Select lines.

High Impedance State for Data bus Driving

- Thermal & Current limit Protection
- >10 Million Transfers Per Second (MT/s)
- Space Efficient Package (11 X 16 mm Footprint)
- 1.4 mA Standby Supply Current

Figure 4.42.1. - SN75LBC976: Two Chip Differential SCSI

The SN75LBC976 is fully configurable to facilitate connection to any type of SCSI system arrangement. The 9 channels can be arranged into seven possible channel functions using the BSR, CDE0, CDE1, CDE2, CRE control pins.

The 7 channel configurations are:

1. Transparent, permanently enabled Receiver.
2. Transparent, permanently enabled Driver.
3. Bi-directional transceiver with direction control.
4. Driver with enable control.
5. Open ended driver for Wired OR control lines.

6. Driver with ORed data and enable lines.
7. Permanent high impedance state.

3.5.3 SN75LBC976 Channel Power Dissipation Considerations

Channel Power Dissipation

To understand the SN75LBC976 power dissipation when connected to a SCSI bus and the subsequent heat sinking requirements, we must develop a realistic model for the power consumption under working conditions. We must consider the power dissipation within the silicon. There are three primary sources, the dc quiescent power, the ac or switching power, and the dc or resistive losses in the output drivers.

The current necessary to bias the circuits of a single enabled 'LBC976 differential driver is typically 0.53 mA and a maximum of 1.1 mA. A single enabled receiver circuit requires 3.22 mA typically and 5.00 mA maximum. The typical values have been measured on 94 SN75LBC976DLs from three different wafer lots. The maximums have been verified over temperature on the same samples.

It follows the driver quiescent power consumption, P_{DCC} is:

$$\begin{aligned} P_{DCC} &= I_{CC} \text{ x } V_{CC} \\ &= 0.53 \text{ mA x } 5.00 \text{ V} = 2.65 \text{ mW/Channel average} \\ &= 1.11 \text{ mA x } 5.25 \text{ V} = 5.83 \text{ mW/Channel maximum} \end{aligned}$$

And the receiver quiescent power, P_{RCC} is:

$$\begin{aligned} P_{RCC} &= I_{CC} \text{ x } V_{CC} \\ &= 3.22 \text{ mA x } 5.00 \text{ V} = 16.10 \text{ mW/Channel average} \\ &= 5.00 \text{ mA x } 5.25 \text{ V} = 26.25 \text{ mW/Channel maximum} \end{aligned}$$

The average I_{CC} of a representative sampling of the SN75LBC976 has been measured to be 9.77 mA for nine unloaded drivers switching at 5 MHz (10 Mbps), a 50% duty cycle, and at a V_{CC} of 5 V. Nine receivers at the same frequency and duty cycle and unloaded outputs consumed 36.0 mA average. Since both measurements include P_{DCC} or P_{RCC}, they are subtracted below:

Driver switching losses, P_{DAC}, at 5 MHz:

$$\begin{aligned} P_{DAC} + P_{DCC(average)} &= (I_{CC(average)}/9) \text{ x } V_{CC} \\ P_{DAC} &= (I_{CC(average)}/9) \text{ x } V_{CC} - P_{DCC(average)} \\ &= (97.7/9) \text{ x } 5.0 - 2.65 \\ &= 51.6 \text{ mW/Channel} \end{aligned}$$

Receiver switching losses, P_{RAC}, at 5 MHz:

$$\begin{aligned} P_{RAC} + P_{RCC(average)} &= (I_{CC(average)}/9) \text{ x } V_{CC} \\ P_{RAC} &= (I_{CC\ (average)}/9) \text{ x } V_{CC} - P_{RCC(average)} \\ &= (36.0 \text{ mA}/9) \text{ x } 5.0 \text{ V} - 16.10 \\ &= 3.9 \text{ mW/Channel} \end{aligned}$$

The output stage losses vary with the magnitude of the output voltages or the output transistor saturation voltages and with the load conditions. The following is based upon the solution of the equivalent circuit of a differential SCSI bus and no further proof is included in this analysis.

For the differential driver, the worst case condition is with a driver asserting the line with SCSI bus termination and a differential output voltage of about 2 V. Under these conditions there would be 144 mW dissipated in the output transistors when asserted and 71 mW when negated. The average output voltage of the SN75LBC976 driver is 2 V. As such, the average power dissipated in the output transistors is also a worst case condition.

Driver output dc losses, P_{DOH} is given by:

$$P_{DOH} = 144.0 \text{ mW/Channel}$$

The same circuit but with the line negated:

$$P_{DOL} = 71.0 \text{ mW/Channel}$$

The receiver output stage is rated for sinking 8.0 mA at a maximum low-level output voltage of 0.8 V.

Receiver output dc losses, P_{RO}, is given by:

$$P_{RO} = 8.0 \text{ mA} \times 0.8 \text{ V} = 6.4 \text{ mW/Channel maximum}$$

Since $P_{DCC} + P_{DAC} = P_{DO} >> P_{RCC} + P_{RAC} + P_{RO}$, the worst case power dissipation in a data channel occurs when the driver is enabled and transmitting data. This case will be used to analyse the device power dissipation.

Device Power Dissipation

Assuming the probability that any one bit on the bus is asserted is equal to the probability of being negated, the state of the output is non-deterministic, and the thermal time constant of the device is long with respect to the data transfer period, the mean die temperature will be determined by the mean power dissipation. In the driver output this is the mean of the asserted and negated values:

Mean device output dc losses:

$$\begin{aligned} P_{DO(DEV)} &= (P_{DOH} + P_{DOL})/2 \text{ x } 9 \text{ Channels} \\ &= (144 \text{ mW/Ch} + 71 \text{ mW/Ch})/2 \text{ x } 9 \text{ Channels} \\ &= 967.5 \text{ mW} \end{aligned}$$

From the assumptions above and the probability that the driver output will change state on the next cycle is equal to the probability that it will not, the mean power dissipated due to driver switching is one-half P_{DAC} which was measured with the switching loss occurring every cycle.

Mean device switching losses:

$$\begin{aligned} P_{DAC(DEV)} &= P_{DAC}/2 \text{ x } 9 \text{ Channels} \\ &= (51.6 \text{ mW/Ch})/2 \text{ x } 9 \text{ Channels} \\ &= 232.2 \text{ mW} \end{aligned}$$

Total Device quiescent power:

$$\begin{aligned} P_{DCC(DEV)} &= P_{DCC(average)} \text{ x } 9 \text{ Channels} \\ &= 2.65 \text{ mW/Ch x } 9 \text{ Channels} \\ &= 23.85 \text{ mW} \end{aligned}$$

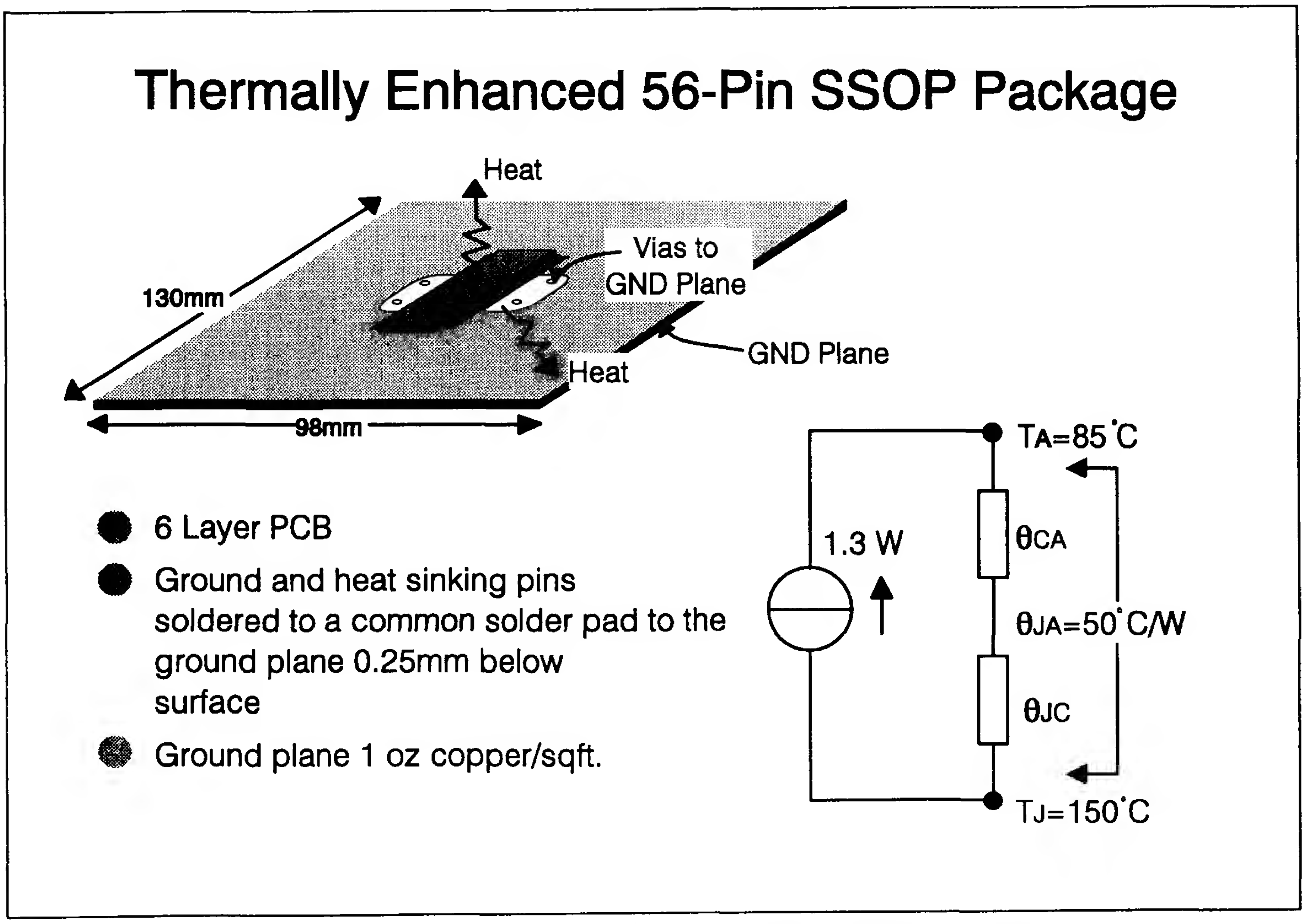
The total mean power dissipated in 9 enabled drivers transmitting over a SCSI bus for several package thermal time constants is then

$$
\begin{aligned}
P_{D(DEV)} &= P_{DO(DEV)} + P_{DAC(DEV)} + P_{DCC(DEV)} \\
&= 967.5 \text{ mW} + 232.2 \text{ mW} + 23.85 \text{ mW} \\
&= 1223.6 \text{ mW}
\end{aligned}
$$

3.5.4 Junction Temperature and Layout Considerations

Measurements of the thermally enhanced 56-pin SSOP package and lead frame used on the SN75LBC976DL were performed on a 130 mm by 98 mm six layer printed circuit board with the ground and heat sinking pins soldered to a common solder pad and connected to a second layer ground plane through one via interconnect, see figure 4.43. The ground plane was 0.254 mm below the surface of the board and was a 1 oz copper layer. The results of two tests resulted in θ_{JA}s of 52.9 and 46.6°C/W with zero air flow.

The mean junction temperature rise above ambient when all drivers are enabled and transmitting data over the SCSI bus for several package thermal time constants can then be calculated.



Thermally Enhanced 56-Pin SSOP Package

- 6 Layer PCB
- Ground and heat sinking pins soldered to a common solder pad to the ground plane 0.25mm below surface
- Ground plane 1 oz copper/sqft.

Figure 4.43 - Thermally Enhanced 56-pin SSOP Package

Junction temperature rise above ambient:

$$
\begin{aligned}
T_J - T_A &= \theta_{JA} \text{ x } P_{D(DEV)} \\
&= (52.9^{\circ}\text{C/W} + 46.6^{2}\text{C/W})/2 \text{ x } 1233.6^{\circ}\text{mW x 1 W/1000 mW} \\
&= 60.8^{\circ}\text{C}
\end{aligned}
$$

Most designs require two junction temperature conditions to be met. The junction operating temperature should not exceed 150°C under worst case operating conditions and the average operating junction temperature should be no more than 110°C.

Since the worst case condition of all nine channels transmitting data was used for analysis, the maximum ambient air temperature, T_A, with no air flow should be:

$$\begin{aligned} T_{A(maximum)} &= 150°C - 60.8°C \\ &= 89.2°C \end{aligned}$$

When evaluating the average operating junction temperature the effects of transmit/receive duty cycle communication port activity must be taken into account.

3.5.6 Driving the 'Wired-Or' SCSI Lines with the SN75LBC976

The control lines of the SCSI bus have three 'Wired-Or' lines, these are BSY (busy), RST (reset), and SEL (select). These lines are wired-or in that the line drivers connected to these lines drive in one direction (assertion) only and are tri-stated (high impedance) when negated. This allows numerous drivers to be active at the same time without affecting the logic state of the line and requires that all drivers be released or off before the logical state can change. When tri-stated the bus termination network passively negates the signal.

The technique used for wired-or operation with differential transceivers is to input the signal into the driver enable pin and connect the driver input to a fixed logic level input. When the input signal to the driver enable is active (high), the driver becomes enabled and the outputs drive the SCSI bus to the state of the driver input. When the input signal at the driver enable pin goes low, the driver turns off and allows the bus termination to negate the signal on the bus after all other drivers on the bus are also shut off.

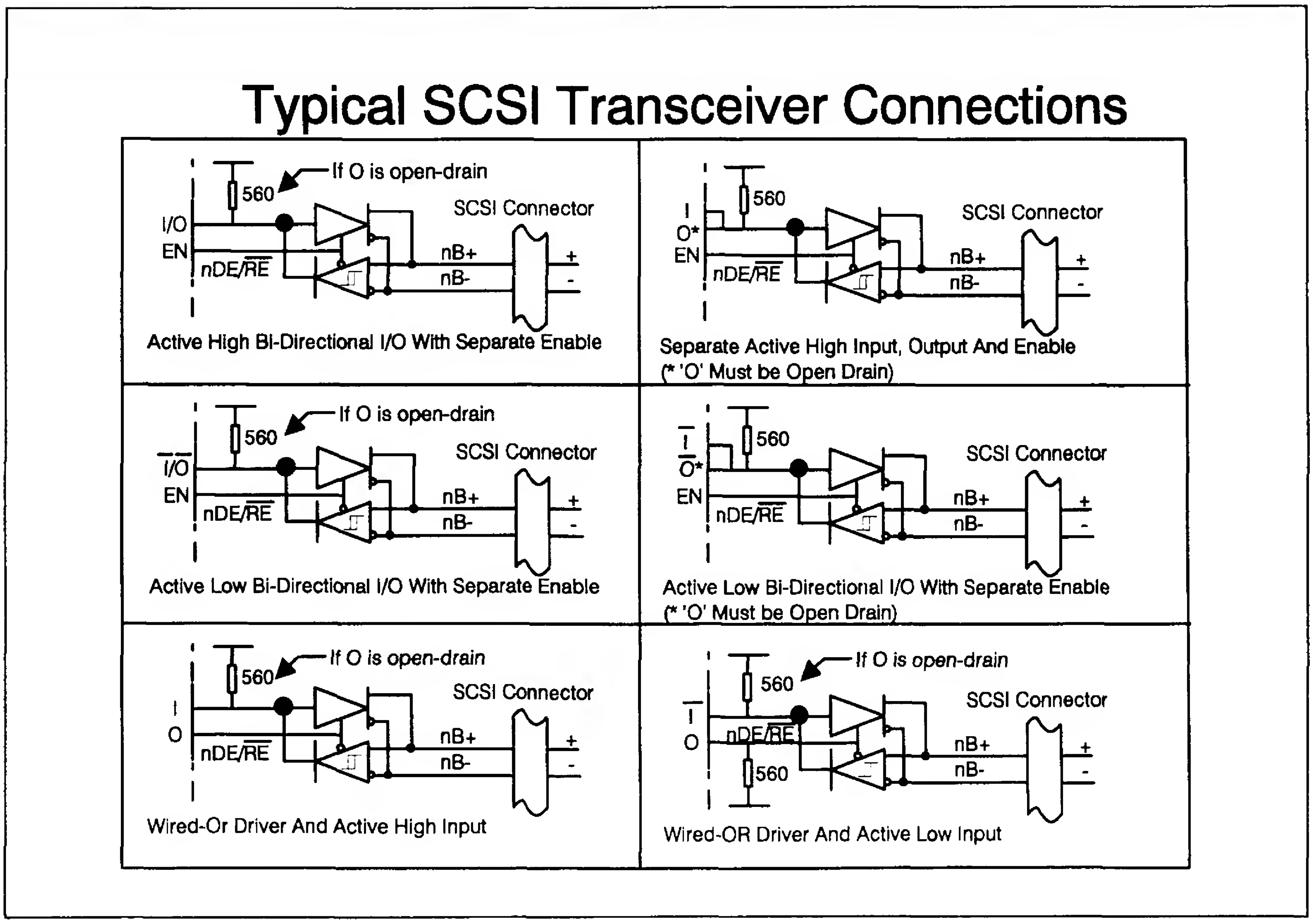

Typical SCSI Transceiver Connections
If O is open-drain
560
I/O
EN
nDE/RE
SCSI Connector
nB+
nB-
+
-
Active High Bi-Directional I/O With Separate Enable
I
O*
EN
Separate Active High Input, Output And Enable
(* 'O' Must be Open Drain)
Active Low Bi-Directional I/O With Separate Enable
Active Low Bi-Directional I/O With Separate Enable
(* 'O' Must be Open Drain)
Wired-Or Driver And Active High Input
Wired-OR Driver And Active Low Input

Figure 4.43.1 - Typical SCSI Transceiver Connections

Many communications controllers used for differential SCSI have separate inputs and outputs for these signals. When used with the SN75176 type RS-485 transceiver, these controller I/Os can be directly connected to separate driver enable inputs or receiver outputs. The SN75LBC976 device does not have a separate driver input and receiver input, these are tied together internally to save pins.

Controllers with separate I/Os can still be used with the 'LBC976 using the connections shown in figure 4.43.1. The controller output will go high and enable the driver and disable the receiver. Upon disabling the receiver, the external pull-up or pull-down resistor will drive pin A of the 'LBC976 to the proper level for bus assertion and the driver will assert the SCSI signal line. When the controller output goes low, the driver disables and allows the termination to negate the bus signal. After a short delay, the receiver outputs are enabled and will reflect the logical state of the bus signal.

3.5.7 Using the WRAP function of the SN75LBC978

Two Chip Differential SCSI with the SN75LBC978

The second 9 Channel Differential Transceiver from Texas Instruments is the SN75LBC978. This device performs the same basic function for differential SCSI as its predecessor the SN75LBC976 of interfacing the RS-485 signals with the logic signals of the SCSI communications controller. The SN75LBC978 differs in the logic used to control the enabling of the drivers and receivers.

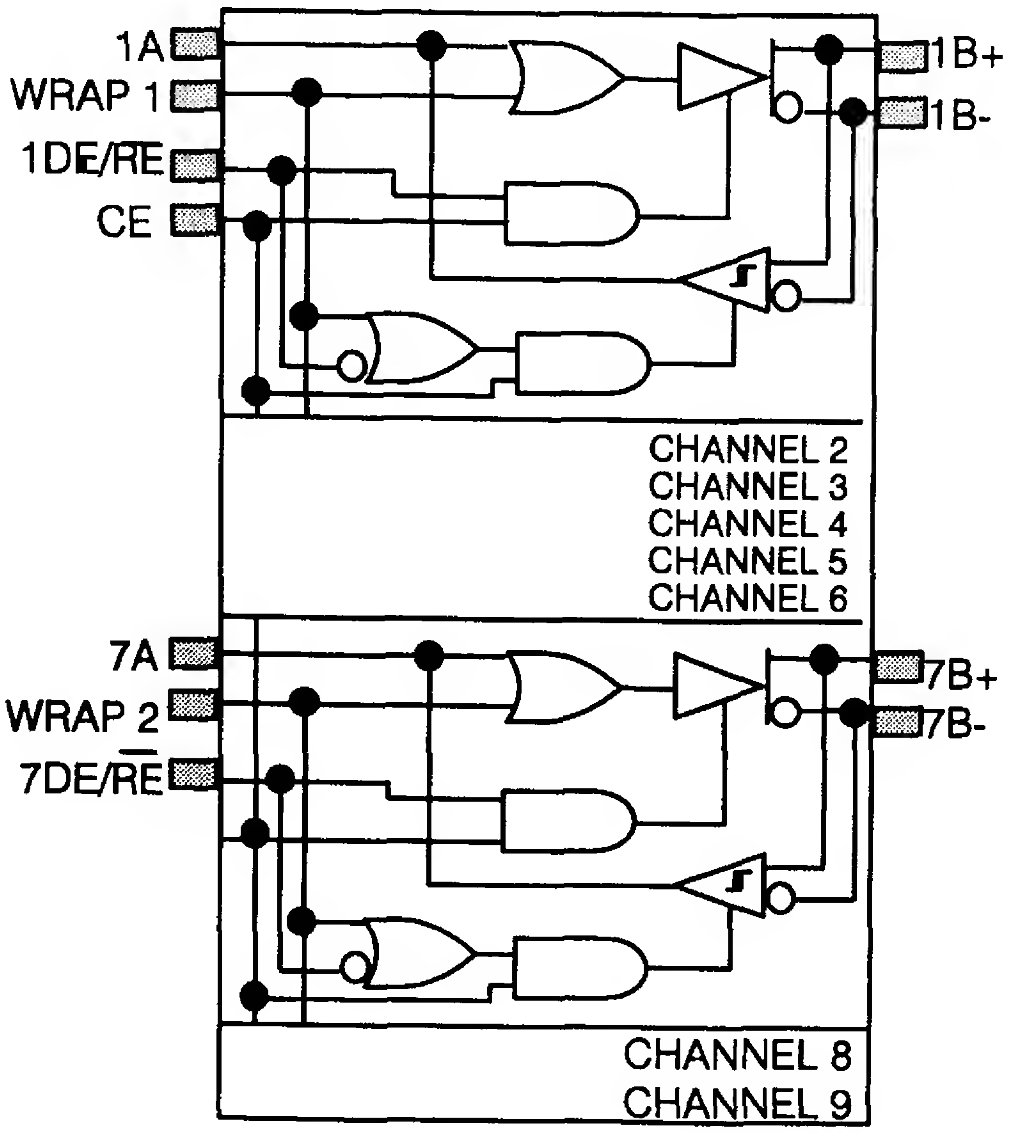
There are three control inputs to each channel of the SN75LBC978 Transceiver, WRAP, CE and DE/RE_N. (Active low signals are denoted by the "_N" symbol.) The CE (Chip

Enable) affects all 9 channels the two WRAP inputs affect groups of six and three channels and the DE/RE_N affects each channel.

As its name implies a high level CE input enables the control of the drivers and receivers through the DE/RE_N and WRAP inputs. CE is usually connected to the DIFFSENS line of the SCSI cable and is intended to disable the drivers should a single ended plug and cable be connected to the differential jack pulling CE to a low level and disabling the drivers. When CE is low the SN75LBC978 is in its lowest quiescent power state. The CE input is internally pulled down when left open.

When CE is at a high level, the basic transceiver function is then controlled by WRAP and DE/RE_N. A low level input to the WRAP pin configures the transceiver as shown in figure 4.44. This is the basic function for most SCSI signals with a single direction control and a bi-directional input and output at A.

SN75LBC978: Two Chip Differential SCSI



- Each Transceiver meets EIA RS-485 and ISO 8482 : 1987 (E) Standards
- Designed to operate at 10 Million transfers per second
- Low disabled supply current 1.4mA typ
- Thermally enhanced 56 pin SSOP Package
- Transceiver configuration: SCSI signals DB(n),REQ,ACK etc

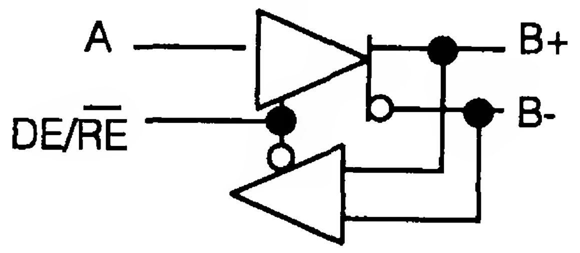
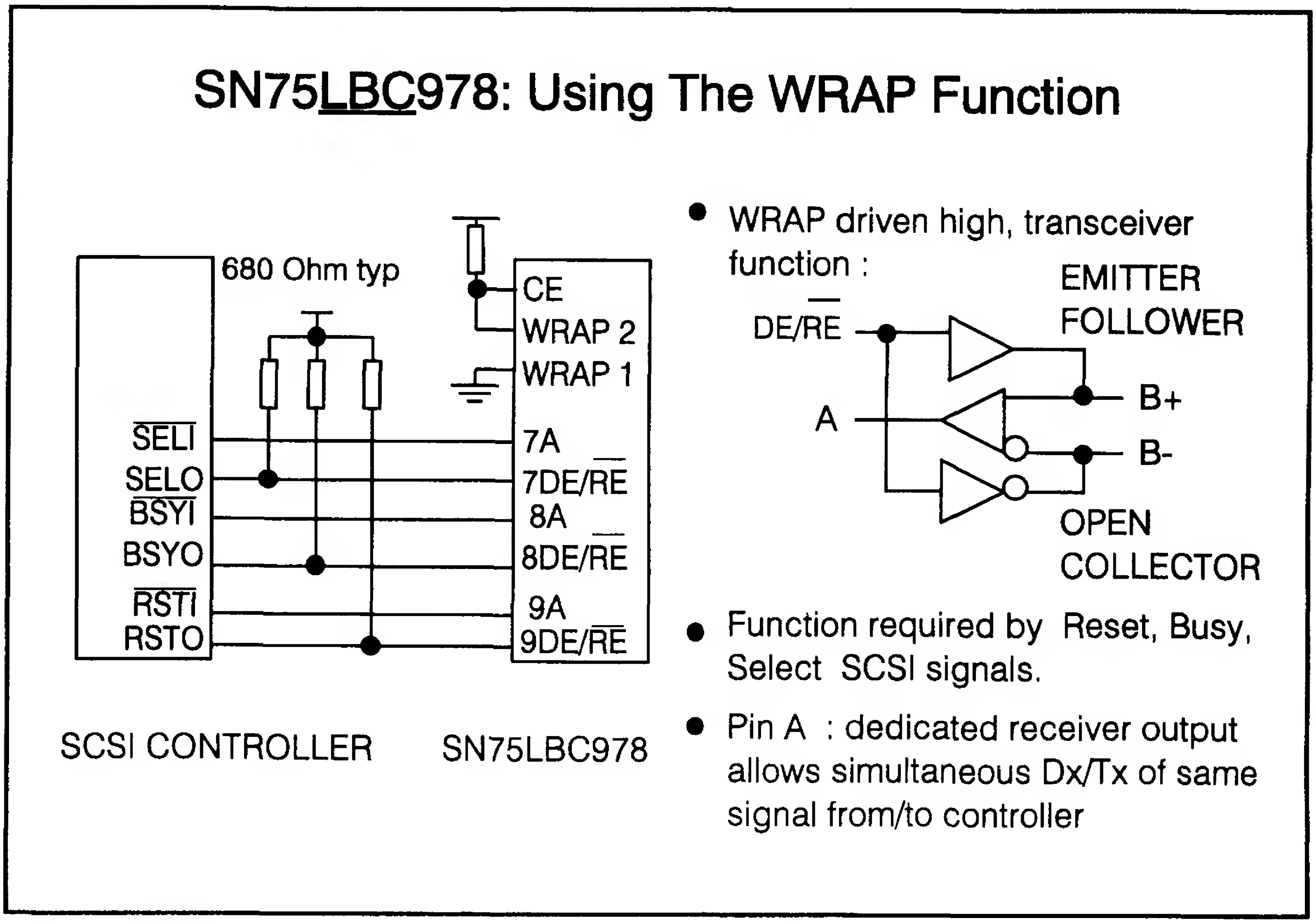


Figure 4.44 - Two Chip Differential SCSI

The unique feature of the SN75LBC978 is the WRAP function. When WRAP is driven to a high level, the transceiver function becomes that shown on figure 4.45. This function is useful for SCSI and its wired or signals RST, BST and SEL. although these signals can be driven with the transceiver configured as in figure 4.44, the WRAP function frees A pin for a dedicated receiver output to the controller rather than sharing this pin with the driver input. This effectively allows simultaneous driving and receiving of the same signal from and to the controller and eliminates the need for an external pull up or pull down resistor for the non - WRAP transceiver.

In addition to the Wired-or signals, a test routine can be devised to test the integrity of the SCSI port circuitry at the connector. Attaching the SCSI termination to the bus pins will put approximately -1V (referenced to B-) and be translated by the receiver as a low level output at pin A. As DE/RE_N is driven high, the bus is driven by the driver to the opposite polarity of about 2V and in turn changes the receiver output to a corresponding high-level output. In performing this sequence, the electrical continuity and transceiver function of the SCSI port can be verified.



SN75LBC978: Using The WRAP Function

- WRAP driven high, transceiver function :
- Function required by Reset, Busy, Select SCSI signals.
- Pin A : dedicated receiver output allows simultaneous Dx/Tx of same signal from/to controller

Figure 4.45 - Using the WRAP function

Typical connection of the SN75LBC978 to a SCSI controller's Wired-Or pins

Figure 4.45 shows how the SN75LBC978 can be connected to a controller with separated I/Os for the Wired-Or signals. Since only three lines are needed, WRAP2 is connected to Vcc through a pull up resistor configuring channels 7,8 and 9 as the wired-or lines. Since A pin of the SN75LBC978 is a dedicated output with WRAP enabled, no external resistors are required.

The other SCSI signal lines use the non WRAP'ed function and their connection to the control varies depending upon the controller's electrical characteristics. The reader is referred to the datasheet for the SN75LBC978 or the SN75LBC976 for further information on these connections.

3.5.8 The SCSI Signals

The SCSI signals are :

ACK (Acknowledge)	The initiator asserts this line to acknowledge that it has accepted or supplied data in response to the REQ signal (which is asserted by the target). All asynchronous data transfers over the SCSI bus use the same REQ/ACK handshake sequence.
ATN (Attention)	A host asserts this signal to let a controller know that it has a message for it. The controller can then ask for the message using the MESSAGE OUT bus.
BSY (Busy)	The signal is asserted by one or both of the parties to a transaction to indicate the bus is in use.
C/D (Control/Data)	The signal is controlled by the target during the transaction and it indicates whether control information or data is on the bus.
Data lines(DB0, DB7 and DB(P))	These lines form bi-directional data bus with optional parity. In addition they carry SCSI IDs of devices when they contend for the bus and when they establish (or re-establish) connections with other devices. (Each ID corresponds to one line on the bus being active.)
DIFFSENS (Differential Sense)	This line which is found only on differential SCSI buses enables differential drivers.
I/O (Input/Output)	This signal indicates the direction of a data transfer relative to the initiator (host). It is driven by the target and also distinguishes between the Selection (done by the initiator) and Reselection (done by the target) bus phases.
MSG (Message)	This signal which is controlled by the target indicates which message is on the bus.
REQ (Request)	The target asserts this signal to begin an asynchronous bus transfer using the REQ/ACK handshake sequence.
RST (Reset)	This signal resets the bus. Any device can assert it; it is not normally used only at power up time or when a selected device is not responding.
SEL (Select)	A host uses this signal to specify the controller that it wishes to talk to and vice versa. (The ID of the device being selected appears on the data lines.)
TERMPWR (Terminator power)	This line provides to the terminator resistor networks at either end of the bus.

3.6 Meter-Bus Concept

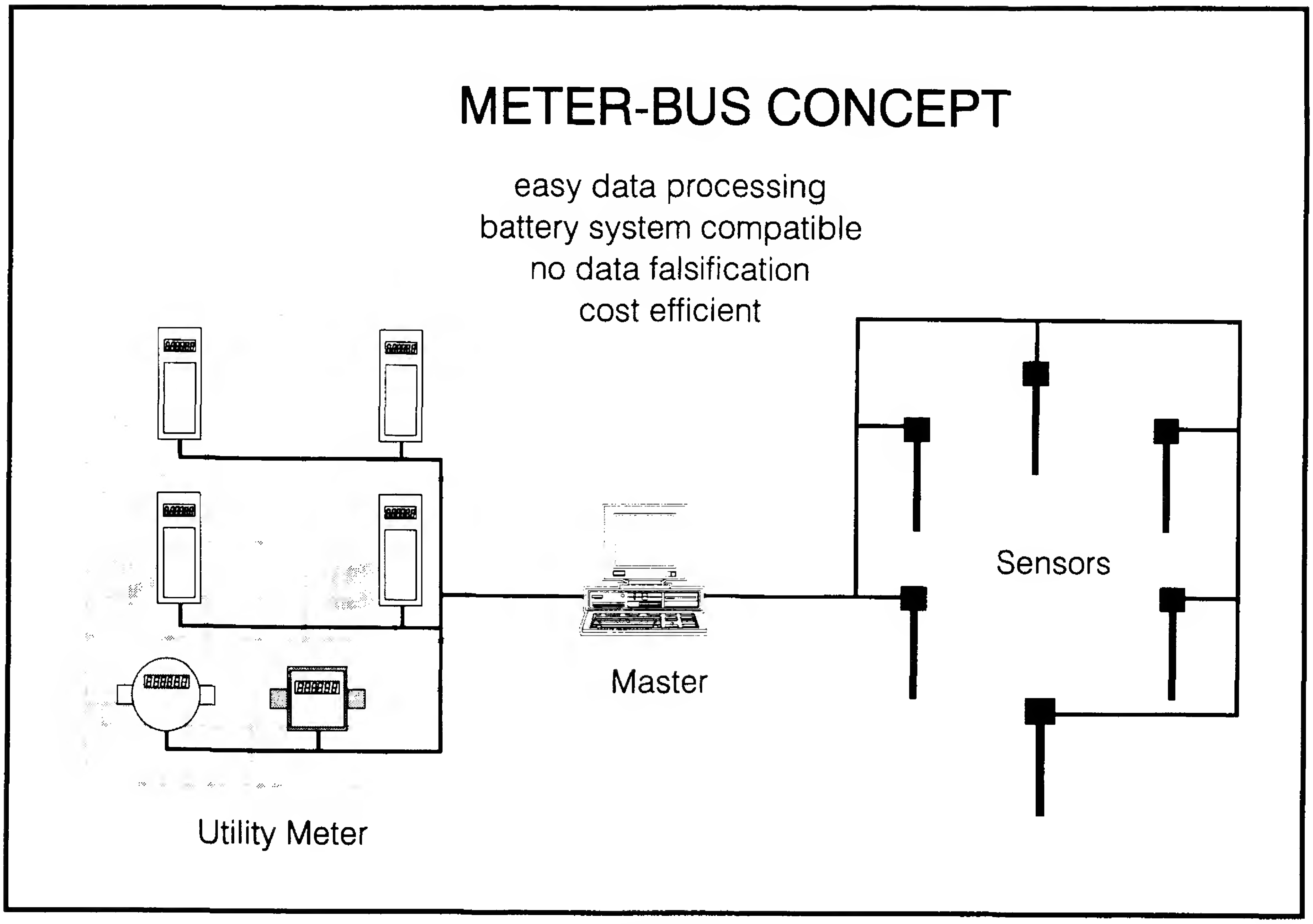


Figure 4.46 - Meter-Bus Concept

In applications like Utility Meters or remote measurement in the field the usage of battery powered sensor systems is rapidly increasing. The operation for many years with one set of battery is a basic requirement and therefore these systems are designed for very low current consumption, down to a few mircoamps.

Once electronic Utility Meters are installed in private and commercial buildings the need for a bus system is very clear. A bus system for electronic meters offer a lot of advantages. Data processing can be done very easily. Computer systems can exchange information as often as necessary and erroneous read-outs are minimised. If all meters are read-out fully automatically privacy and a maximum of security are guarantied for the end-user. No meter-man has to access private homes which is also a major cost reduction.

The bus system can connect the meters with a central Master Unit where read-out data are collected and stored and from which they can be transmitted via modem and telephone lines over long distances.

Such a bus systems used to link these meters or sensor systems and connect them to a central Master Unit have very special requirements:

- long transmission distances
- safe data transmission
- a maximum of slave count

- compatibility to other Utility meters
- no impact to the sensor system lifetime, i.e. remote power supply
- standard wiring material
- polarity independent

The Meter-Bus has been developed by a team of Utility meter manufacturers, the University of Paderborn and TI in the CEN working group TC176 in order to meat these requirements. A CEN standard for the Meter-Bus is expected for the end of 1994.

3.6.1 Physical Layer

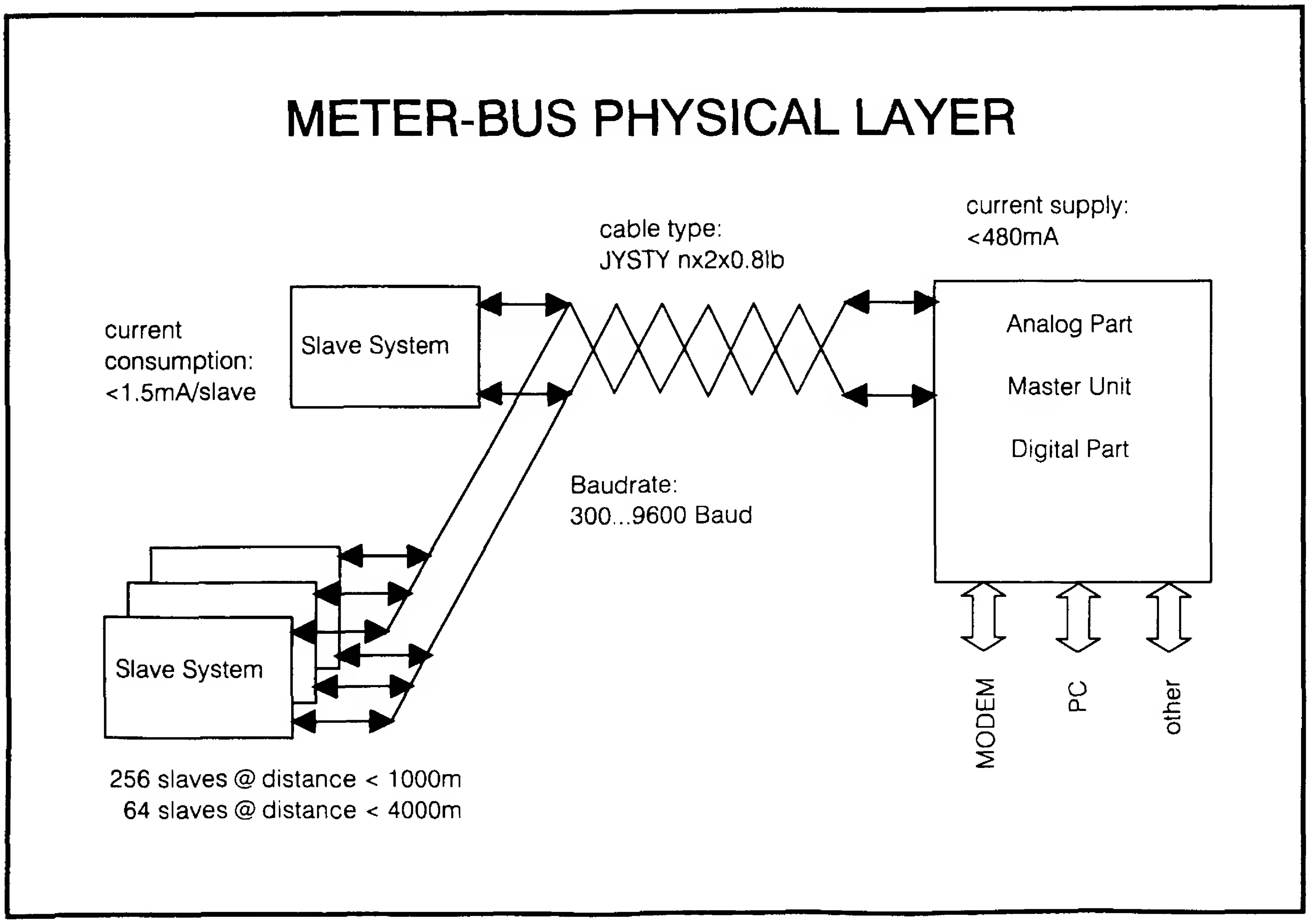

METER-BUS PHYSICAL LAYER
cable type:
JYSTY nx2x0.8lb
current supply:
<480mA
current
consumption:
<1.5mA/slave
Slave System
Analog Part
Master Unit
Digital Part
Baudrate:
300...9600 Baud
Slave System
MODEM
PC
other
256 slaves @ distance < 1000m
64 slaves @ distance < 4000m

Figure 4.47 - Physical Layer

The Meter-Bus uses a Master Unit that controls the protocol on the bus as well as supplying the power for the data transmission. It consists of an analog part that is modulating the bus and detecting information sent from the slave systems.

The slaves, which are typically Meters are connected via a bus-driver unit to ordinary twisted pair telephone wiring material (called JYSTY nx2n0.8lb). For the connection the bus-driver TSS721 is used. Up to 256 slaves can be connected to one Master Unit over a maximum line length of 1000 m. This distance can even be expanded to 4000 m if not more than 64 slaves will be connected.

Each slave is identified by its unique address. The communication is bi-directional. The transmission rate is defined with 300 to 9600 Baud. The power supply for the TSS721 is provided via the bus lines. Some of the energy supplied on the bus lines (1.5 mA/slave) can be used to provide remote powering to a connected slave.

The digital part of the Master Unit controls the level on the analog part, which is handling the bus signals. It is also controlling the bus protocol and is handling data collision. The Master Unit can hold any kind of processor.

The protocol used, which is not at all defined by the Meter-Bus, defines the hardware requirements of the digital part. A Master Unit typically is equipped with an interface to other data processing or transmitting systems (like PC, Modem, Handhold Terminal, other Bus Systems).

3.6.2 Modulation

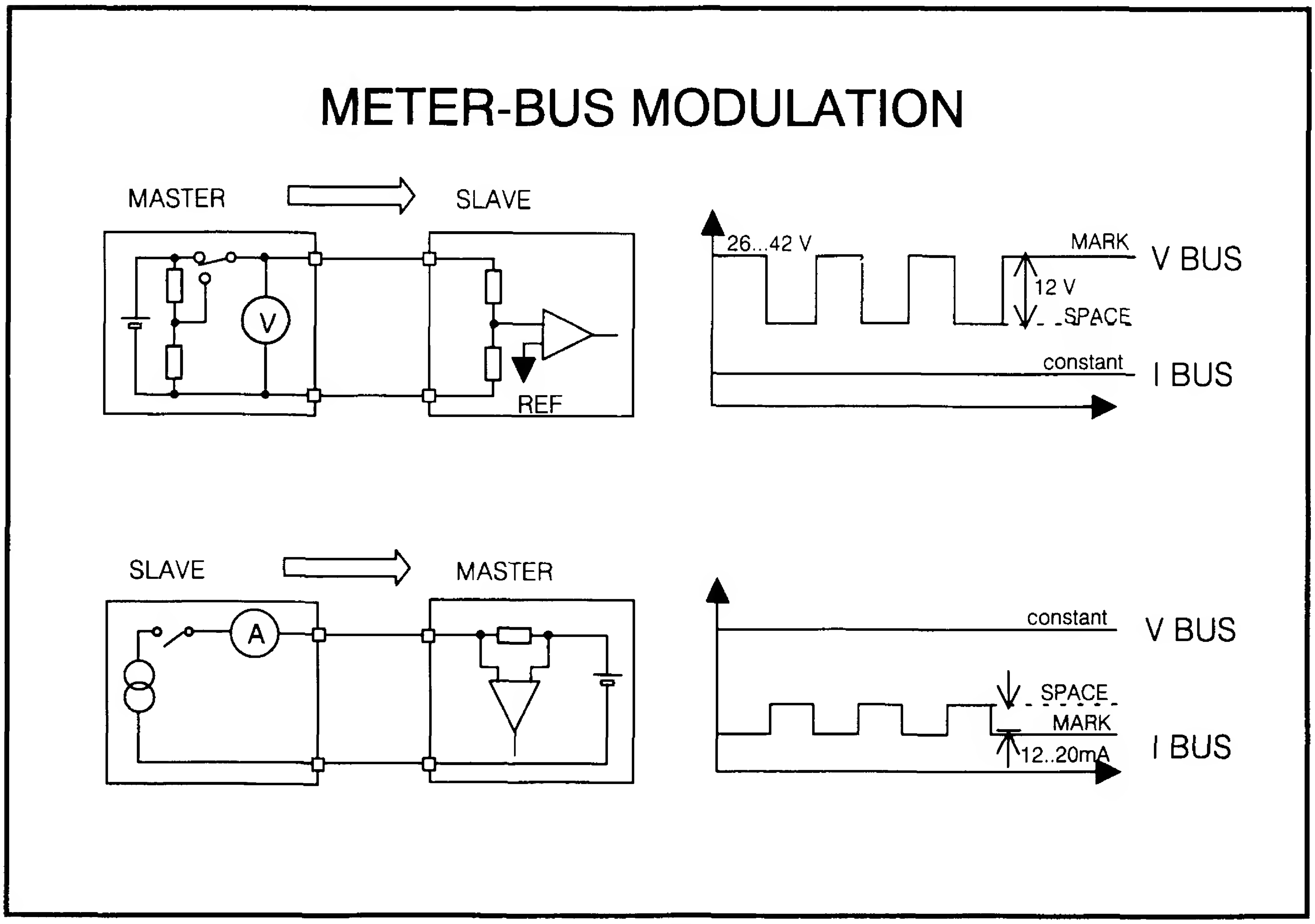


Figure4.48 - Modulation

Since the Master Unit needs to supply the power for the driver unit as well as for the driving of information a current loop seems to be ideal. A typical current loop works with 20 mA levels. However 256 systems connected to a bus each working on 20 mA is too much power on an ordinary telephone cable type. A pure voltage modulation would require a lot of power from the slave supply system to drive the information through the lines to the Master. A remote supply would be impossible.

The Meter-Bus uses both versions. The communication from the Master to the slave is done using different voltage levels. The communication from the slave to the Master is done by different current levels.

Master to Slave

Depending on the number of slaves connected to the system and depending on how much power is used for remote power supply a certain idle current level is defined.

The idle mode, the mark state, is defined by a voltage level between 24 V and 42 V. A space state is defined by a voltage drop of 12 V. Whatever the mark state is in the given window, the space state is less 12 V down to 0 V. 0 V is an invalid state since the power supply on the bus would break down. The idle current remains almost unchanged during this modulation.

Slave to Master

Any slave is sending data to the Master Unit by modulating the current on the bus. Only one slave system can send at one time. Bus collision must be handled by the protocol and the Master Unit. The TSS721 driver unit activates a built-in current sink to modulate the current on the bus lines. The idle mode, mark state, is 0 mA to 1.5 mA signal level. The space state is a maximum 20 mA signal level. The signal level is defined as the current flowing without idle current used to supply the TSS721 units and the remote powered slaves. The mark level voltage remains unchanged during this data transmission.

Since the TSS721 is configured for half duplex only, the current modulation from RX or RXI is concurrently repeated as ECHO on the outputs TX and TXI. In case a slave as well as the Master is trying to send information via the bus the added signals are appearing at the outputs TX and TXI which indicates the data collision to the slave.

Because the bus is always powered during normal run mode a connected slave can send requests at any time the bus is unused and the remote power feature can be used to supply connected slaves without their own power

3.6.3 Master Unit and Repeater

As already described one Master Unit can handle up to 256 TSS721 units for a maximum cable length of 1000 meters. Whenever more than 256 units are connected to the bus or the cable length is longer than 1000 meters, Repeaters are necessary. A Meter-Bus Master Unit supplies all connected slaves with power for the Driver units as well as power for the communication and, if used, with remote powering for the micro-controller system.

Each Repeater can handle maximum of 256 slave units for a bus line length of 1000 m. As many Repeaters as necessary can be used in a Meter-Bus system. A Repeater serves a segment. Up to 256 segments can be connected to one Master Unit via 256 Repeaters, and even that can be expanded if necessary. In each segment 256 slaves can be attached to the bus lines. A Repeater works similar to a Master Unit for the served segment. The input works as an input in a slave system. It detects different voltage levels and transmits these voltage levels to the connected slaves. To a Master Unit a Repeater simulates one slave load. A Repeater uses its own power supply to provide the slave systems in its segment with power and information.

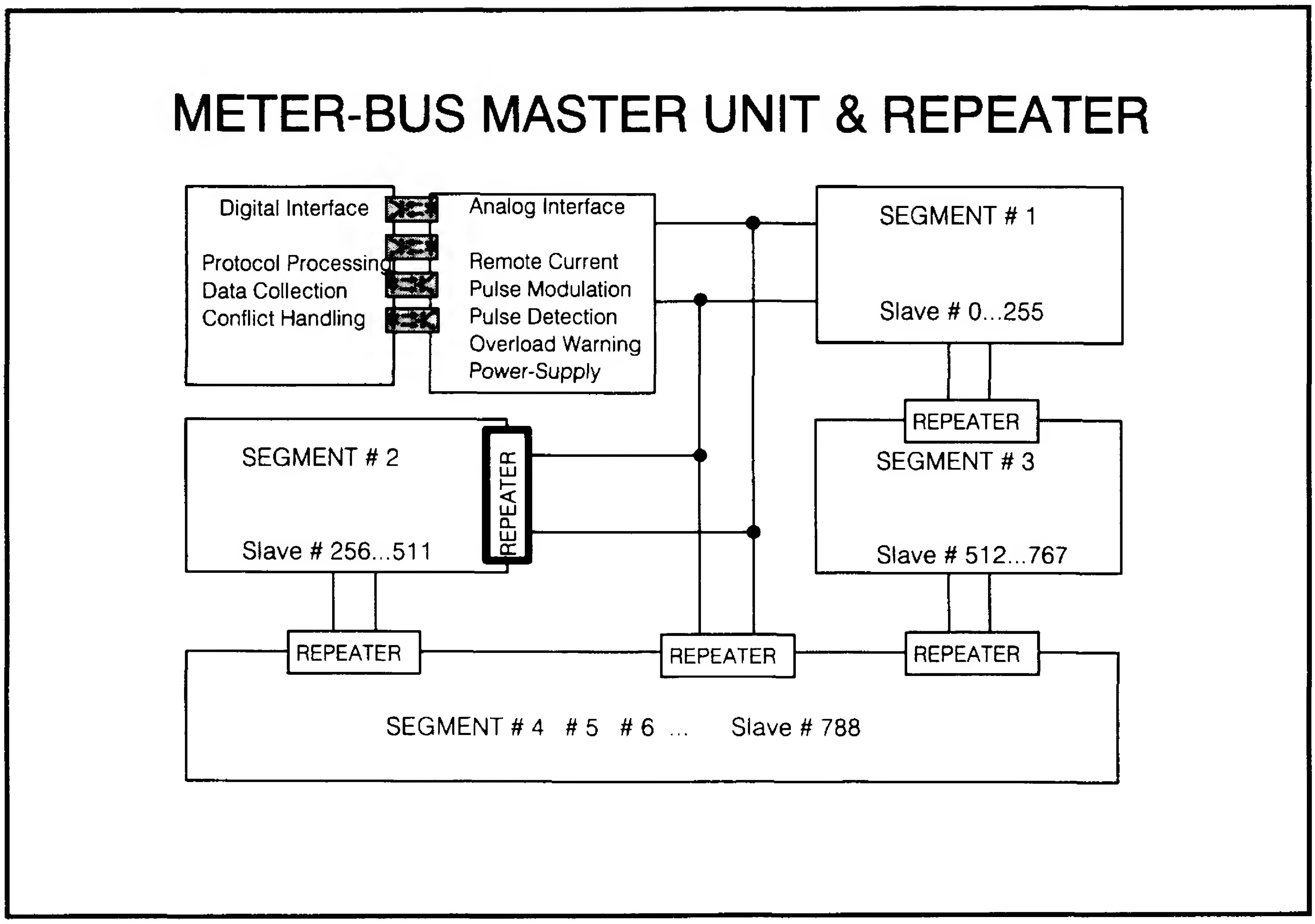

METER-BUS MASTER UNIT & REPEATER
Digital Interface
Protocol Processing
Data Collection
Conflict Handling
Analog Interface
Remote Current
Pulse Modulation
Pulse Detection
Overload Warning
Power-Supply
SEGMENT # 1
Slave # 0...255
REPEATER
SEGMENT # 2
Slave # 256...511
REPEATER
SEGMENT # 3
Slave # 512...767
REPEATER
REPEATER
REPEATER
SEGMENT # 4 # 5 # 6 ... Slave # 788

Figure 4.49 - Master Unit & Repeater

A current signal on the bus lines in a segment is transferred by the Repeater to the main-bus lines connected to the Master Unit. Similar to the TSS721 driver unit the Repeater uses a current-sink to transmit information via different current levels. For the Master Unit a Repeater with its connected slaves is one slave load only.

The protocol is transparent to all connected slaves. This means for example a transmitted address is read by all connected slaves regardless to which segment they are connected. This also means that an address system must be able to address more than 256 slaves. There is no need to connect slave addresses in sequential order to one segment. Repeater and slave systems can be connected to the Master Unit in parallel as long as the maximum number of slaves and Repeaters does not exceed 256 and the maximum line length of 1000 meters is not exceeded.

TI developed an Analog Part of a Master Unit for evaluation purpose. Since the Digital Part of a Master is basically defined by the protocol used on the bus lines, the unit is defined with an interface for any digital processing unit. Any customer will define its own Master Unit and Repeaters but all will show similar features in the Analog Part.

The TI Analog Master Unit expects a processor system that is controlling the data communication in a half-duplex mode. It is this processor system's task to include check-sums to the protocol, check data collision, store data in RAM, EPROM or other media, and control the different run modes of the connected slaves. This processor is not included in the TI evaluation unit. For an evaluation a PC might be used to install a prototype system.

The master Unit must be equipped with an isolated power supply that can supply the power for the slaves. The system must have a galvanic isolation from ground to guarantee a ground-free bus system. 256 slaves must be supplied with a maximum of 1.5 mA per slave plus additional 20 % security for short-circuits in a slave or at data collision.

Data transmission from slaves must be identified. Since all connected driver units and remote power slaves are bus-powered, this power consumption level must be identified as idle state. Only fast current changes after the bus system is powered-up are considered as data information and must be transmitted to the Digital Part. When a Master Unit can adapt to the idle current consumption of a bus, a calibration cycle is not necessary when the bus system or slave number and type are changed.

Overload and short-circuit conditions are checked to avoid the destruction of slaves systems and measurement data.

3.6.4 TSS721 Transceiver

One of the major requirements for the realization of a cost efficient Bus concept is to reduce the number of electronic parts and costs for the driver interface, because the driver interface is a high volume product. The major objective of the TSS721 development was therefore the integration of all necessary functions in one IC with a minimized number of external parts.

TSS721 Features:

-receiver/transmitter logic according to the Meter-Bus specification with dynamic level

recognition

-adjustable constant current sink via external resistor (nominal 20 mA according to

DIN standard 66258 and 66348)

-polarity independent

-power-fail functions

-backup supply functions

-remote powering

Analog Part

The bus lines are connected to the pins BUSL1 and BUSL2. The rectifier bridge rectifies the bus voltage and makes the device polarity independent. The signal is then available at the pins VB and GND. If the chosen bus voltage is very low and the internal voltage drop can not be accepted, the bus voltage can be supplied to the driver via pins VB and GND. The voltage drop in the Schottky rectifier diodes is then eliminated, but the bus lines are no longer polarity independent.

The bus voltage supplies several constant current sources. These constant current sources are the power supply of the entire TSS721 as well as for the connected module which is remote powered. The concept to take all power supply out of the constant current source, is required by the Meter-Bus. Request is a constant quiescent current from the bus. A current variation in each connected module would be added up and cause erroneous transmission.

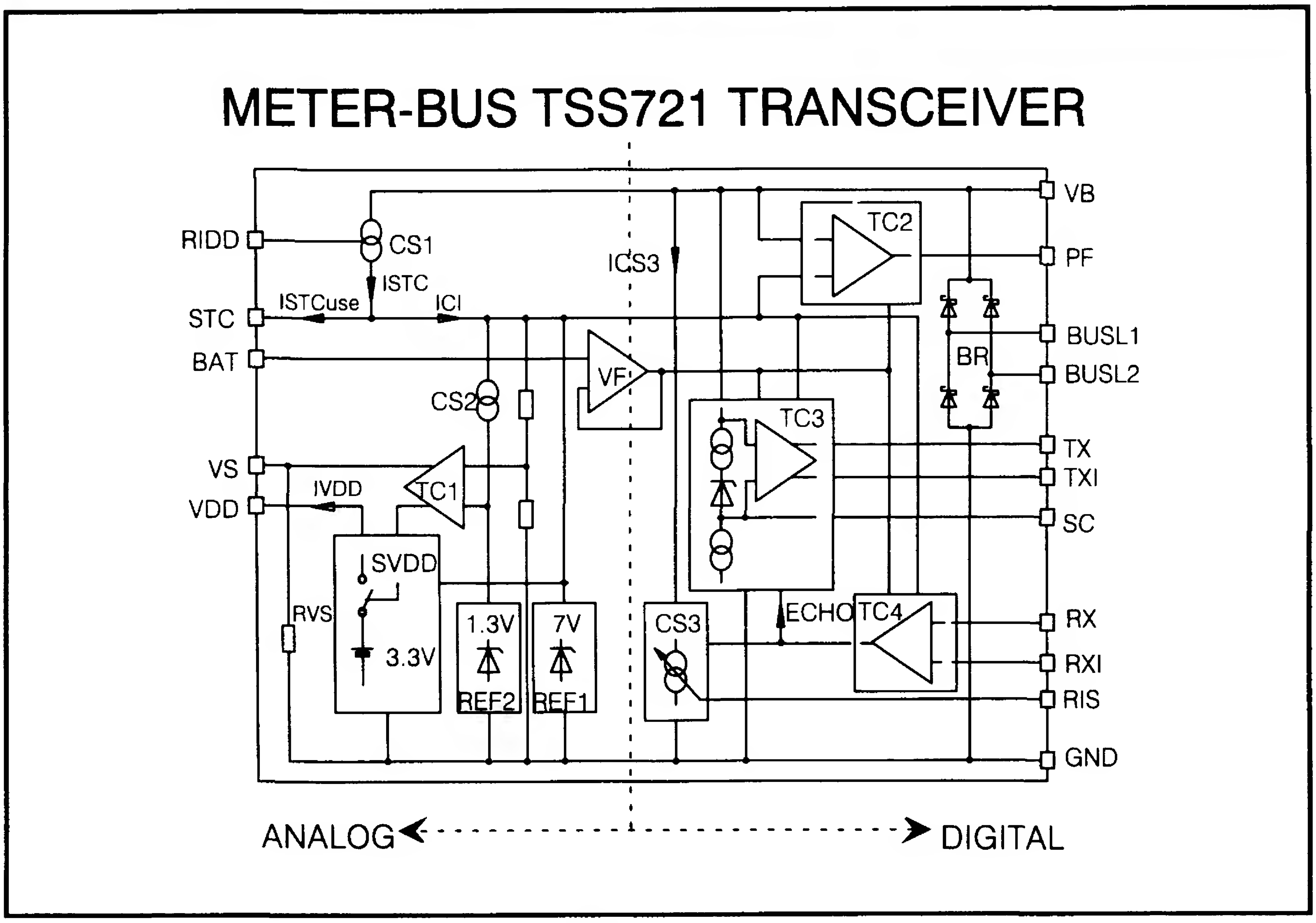

METER-BUS TSS721 TRANSCEIVER
RIDD
STC
BAT
VS
VDD
CS1
ISTC
ISTCuse
ICI
CS2
IVDD
TC1
SVDD
RVS
3.3V
1.3V
REF2
7V
REF1
ICS3
VF
TC2
TC3
BR
CS3
ECHO
TC4
VB
PF
BUSL1
BUSL2
TX
TXI
SC
RX
RXI
RIS
GND
ANALOG
DIGITAL

Figure4.50 - TSS721 Transceiver

The constant current source CS1 is the main power supply and can be programmed by an external resistor typically in the range of 400 µA to 960 µA. The resistor connected to the RIDD pin and the current I_{STC} are calculated by the following formula:

$$I_{STC} = \frac{V_{RIDD}}{R_{IDD}}$$

I_{STC} = constant current of CS1

V_{RIDD} = reference voltage on pin RIDD (typ. 1.26 V)

R_{IDD} = 13 kΩ...80 kΩ

The current I_{STC} splits into the current for the device supply and the charge current for a support capacitor. The support capacitor provides current for a connected module at current peaks and in case the bus power fails. The capacitor is connected to pin SC.

When the bus voltage is switched on and the TSS721 is powered a certain time is required to charge the support capacitor. Since the load current is limited it may, in some cases, take up to one minute until the TSS721 starts the initialisation routine. REF1 tracks a capacitor voltage of typical 7.0 V and activates a Zener diode to take additional current. As already described a constant load on the bus is mandatory.

TC2 tracks the bus voltage and in case of a power-fail pin PF is activated. This pin may be used to detect a power failure and initiate a safe shutdown of the micro-controller system. During the shutdown, power can be supplied by the support capacitor. In case the capacitor voltage falls below 7.0 V the comparator TC1 switches off SVDD since it is not possible to regulate the voltage on VDD to a constant level of 3.3 Volts any longer. Than the low-active pin VS can be used to control a FET-switch which may activate a support battery.

Digital Part

The signal TX and TXI, the inverted output, generate a digital output depending on the voltage levels on the bus. A mark state generates a high level that is defined by the BAT input, the supply voltage of the slave system. The RX pin, or the inverted input, activate the current sink in case the slave system needs to send a logical high. The level acknowledgement is again controlled via the input BAT. RIS is a control input and must be always connected to ground, via a resistor.

3.6.5 Slave System Supply Modes

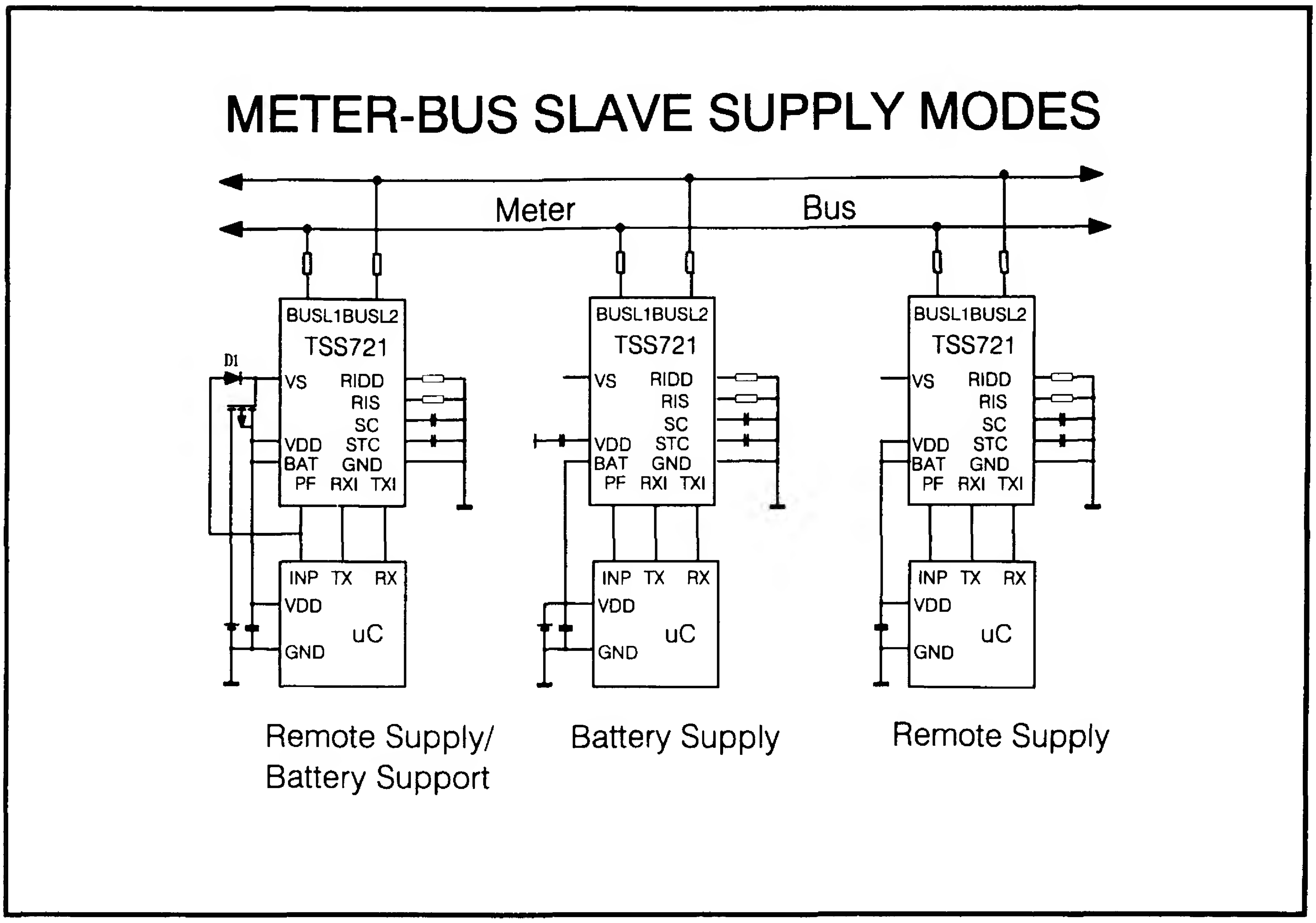

METER-BUS SLAVE SUPPLY MODES
Meter
Bus
D1
BUSL1BUSL2
TSS721
VS
RIDD
RIS
SC
VDD
STC
BAT
GND
PF
RXI
TXI
INP
TX
RX
VDD
uC
GND
Remote Supply/
Battery Support
Battery Supply
Remote Supply

Figure4.51 - Slave System Supply Modes

The TSS721 utilize three different energy supply modes for the connected slave systems. The three modes are:

-Local Supply: energy for slave supplied locally, i.e. by battery

-Remote Supply: energy for slave supplied by the bus

-Mix Mode: energy for slave supplied by bus, in case of power-failure a backup battery is activated

When power for the slave is supplied locally, normally by a battery, the TSS721 is working as a pure driver device only. The information on the bus is supplied in the right voltage format to the slave system. The communication initiated by the slave microcontroller system is transferred into current modulations. For security reasons it is advisable to add resistors (430 Ω) between the bus lines and each driver device. Using resistors has the additional feature that in case of a short circuit the additional power consumption can be tracked by the Master Unit that can initiate an alarm.

Even though the defective unit can not be addressed any longer, all other devices connected to the bus can still be accessed.

The TSS721 allows the remote power supply for the slaves. The driver unit performs the data transmission and the module is fully powered by the bus. In case of a voltage breakdown on the bus the power-fail signal is activated. This enables the processor to save important data and initiate a safe shutdown. The power for this is delivered by the support capacitor.

In the mix-mode the slave system is supplied by the bus lines as long as power is available. A power failure is also indicated by the power-fail pin PF. Additional to this a backup battery is activated by a FET-switch, controlled by the VS pin. The backup battery is active during the bus-off time only so the power supply for the slave system is guaranteed. Since the power-fail pin is still usable for the application to track the power failure, a low power consumption mode can be started. Thereby the capacity of the backup battery may be minimized.

In all three supply modes the TSS721 is powered by the bus lines as long as no power-fail occurs and it does not use any slave system battery capacity.

4 Summary and Further Information

4.1 EIA Standards

For copies of the EIA standards please contact the Electronic Industries Association. For details and a copy of the Catalog of EIA & Jedec Standards & Engineering Publications contact the EIA Standard Sales office at the following address and telephone number:

EIA Standard Sales Office
2001 Pennsylvania Avenue, N.W.
Washington, D.C. 20006
United States
Telephone Number + 1 (202) 457-4966

4.2 SCSI specification

The SCSI specification is available from the

American National Standards Institute,

1430 Broadway,

New York

N.Y. 10018 .

Telephone Number + 1 (212) 642- 4900

4.3 References

The following books were invaluable in producing the Section on data transmission:

1. **Digital, Analog, and Data Communication** - William Sinnema & Tom McGovern - Prentice-Hall International - ISBN 0-835-91313-9.
2. **Data Transmission** - D. Tugal and O. Tugal - McGraw Hill - 1980

4.4 Texas Instruments - Completing the Picture

The range of products discussed throughout this section demonstrate the commitment made by Texas Instruments to the field of peripheral interfacing. Use of leadership technologies has enabled the production of high performance, reliable line drive/receive functions and highly integrated controllers.

Obviously in a seminar this short it is impossible to cover all Texas Instruments' data transmission products. The reader is encouraged to contact a TI representative to obtain the latest data books on transmission ICs. As a minimum the designer should posses a copy of the Data Transmission Circuits Data Book.

Finally, although we have discussed the older standards such as EIA-232 and RS-485 TI is continuing to work and participate in the various standard definition committees to ensure new and emerging standards gain the full support of Texas Instruments' semiconductor experience. Testimony to this fact has been the SN75LBC978 RS-485 transceiver, the specifications for which were closely aligned with the outcome of the work done by the SCSI-3 standards group.

Over the next 12 months TI will be releasing products in support of Futurebus+, and is actively supporting the P1394 high speed serial bus Working Group among others.

Section 5
Power+™ Products

Section Contributions by:

David Cotton Julie Holland Mick Maytum
Ben Mullett Charles Wray

TEXAS INSTRUMENTS

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1 Introduction

1.1 Power+ Spectrum

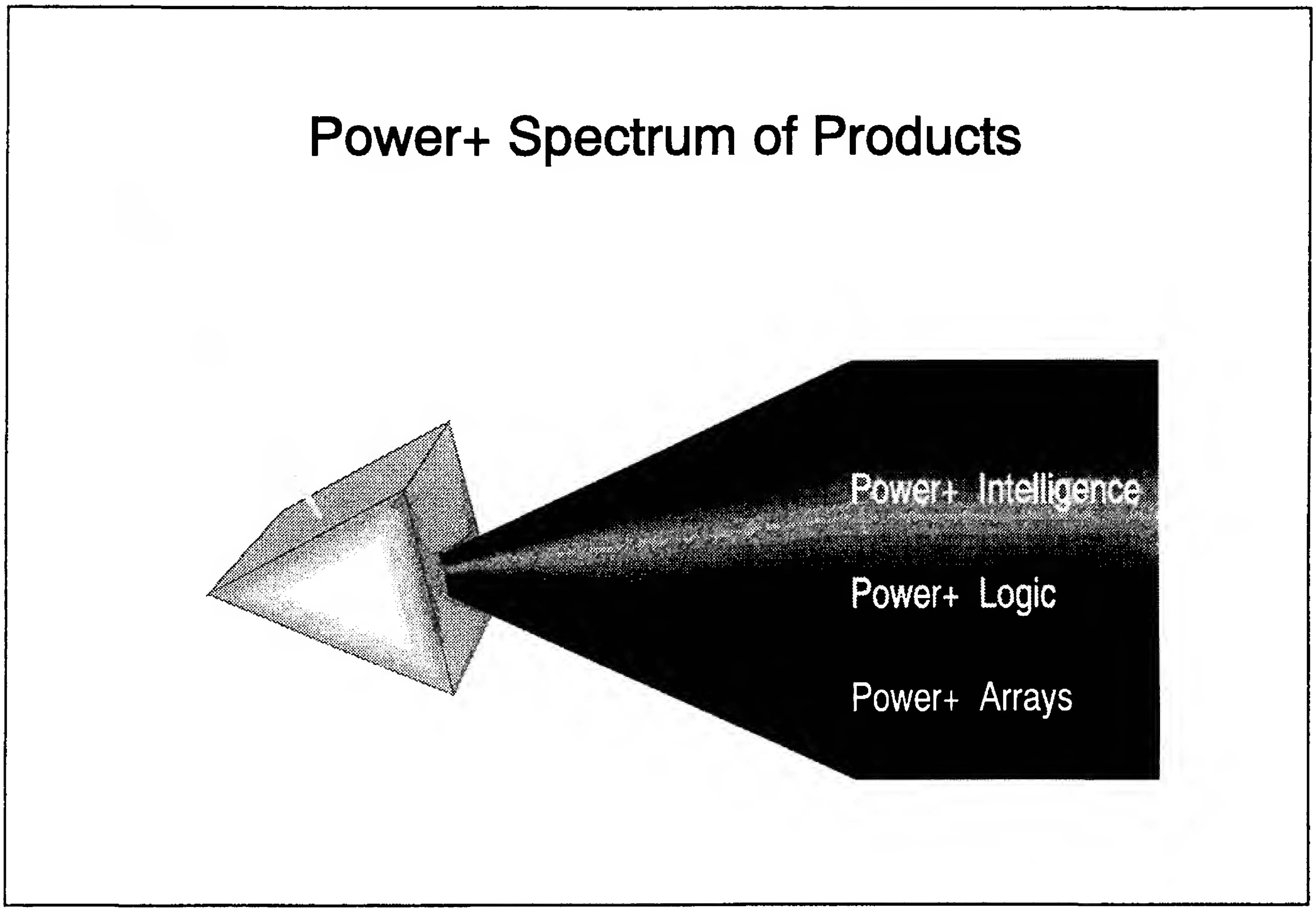

Power+ Spectrum of Products
Power+ Intelligence
Power+ Logic
Power+ Arrays

Figure 5.1.1 - Power+™ Spectrum of Products

Texas Instruments Power+ Products are the latest in a series of power devices introduced by T.I. since the 1970s. The future growth path reflects the major strides made in recent months by our process engineers, and leads us to examine the process used in more detail.

1.2 Lateral DMOS

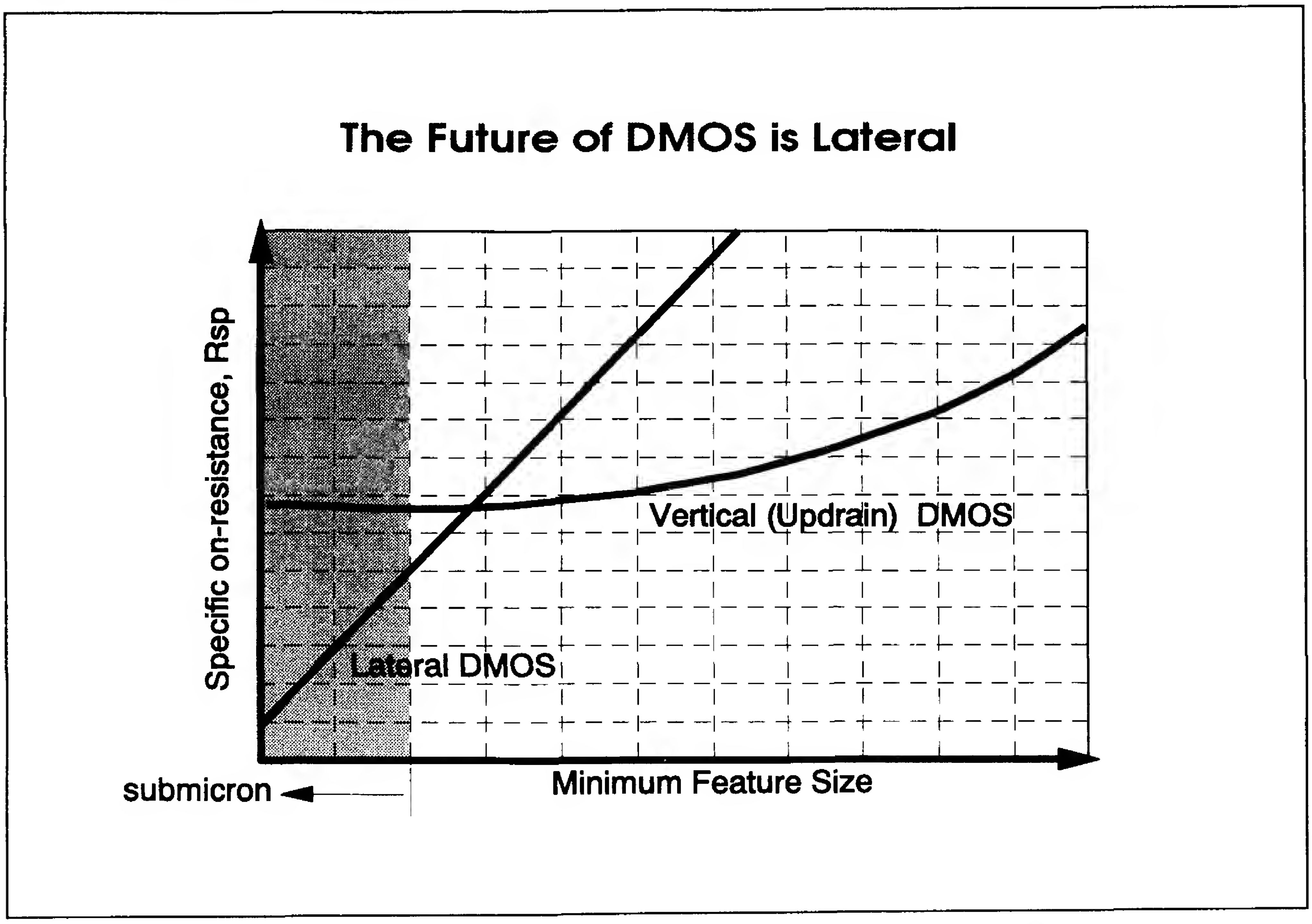


Figure 5.1.2 - Lateral DMOS performance vs Vertical DMOS

The graph shows clearly the increasing perfomance advantage of Lateral DMOS (LDMOS) over conventional structures as feature size reduces. The graph is purposely vague in its terms, since processes vary. What is clear is that process-for-process, LDMOS is superior in the submicron region, which is where all manufacturers are headed, if they wish to remain cost-competitive. The impact of this technology advantage is only just starting to be felt, and will start to make its mark later this year.

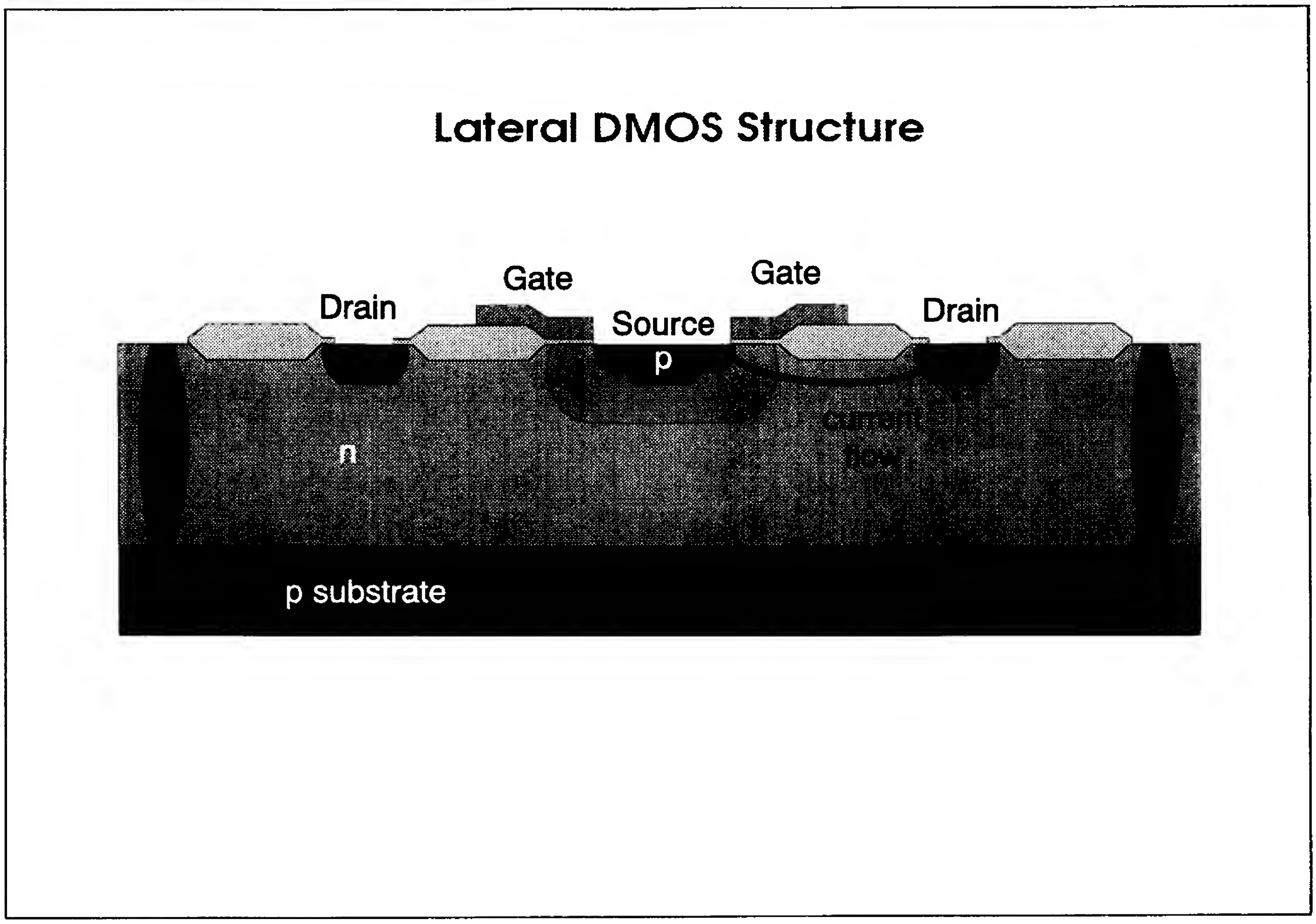

Lateral DMOS Structure
Gate
Gate
Drain
Source
Drain
p
n
current flow
p substrate

Figure 5.1.3 - Lateral DMOS Cross Section

This section through an LDMOS FET shows the directness of the lateral current path compared with vertical or updrain DMOS. The design is also compact, which reduces the size of a given device, and thus reduces the cost of a given switch performance.

As feature sizes reduce with development, so the directness of the lateral current path improves, and the performance of the switch improves proportionally. With vertical or updrain DMOS, the vertical path(s) dominates the overall path length. This does not scale with feature size.

1.3 PRISM Methodology

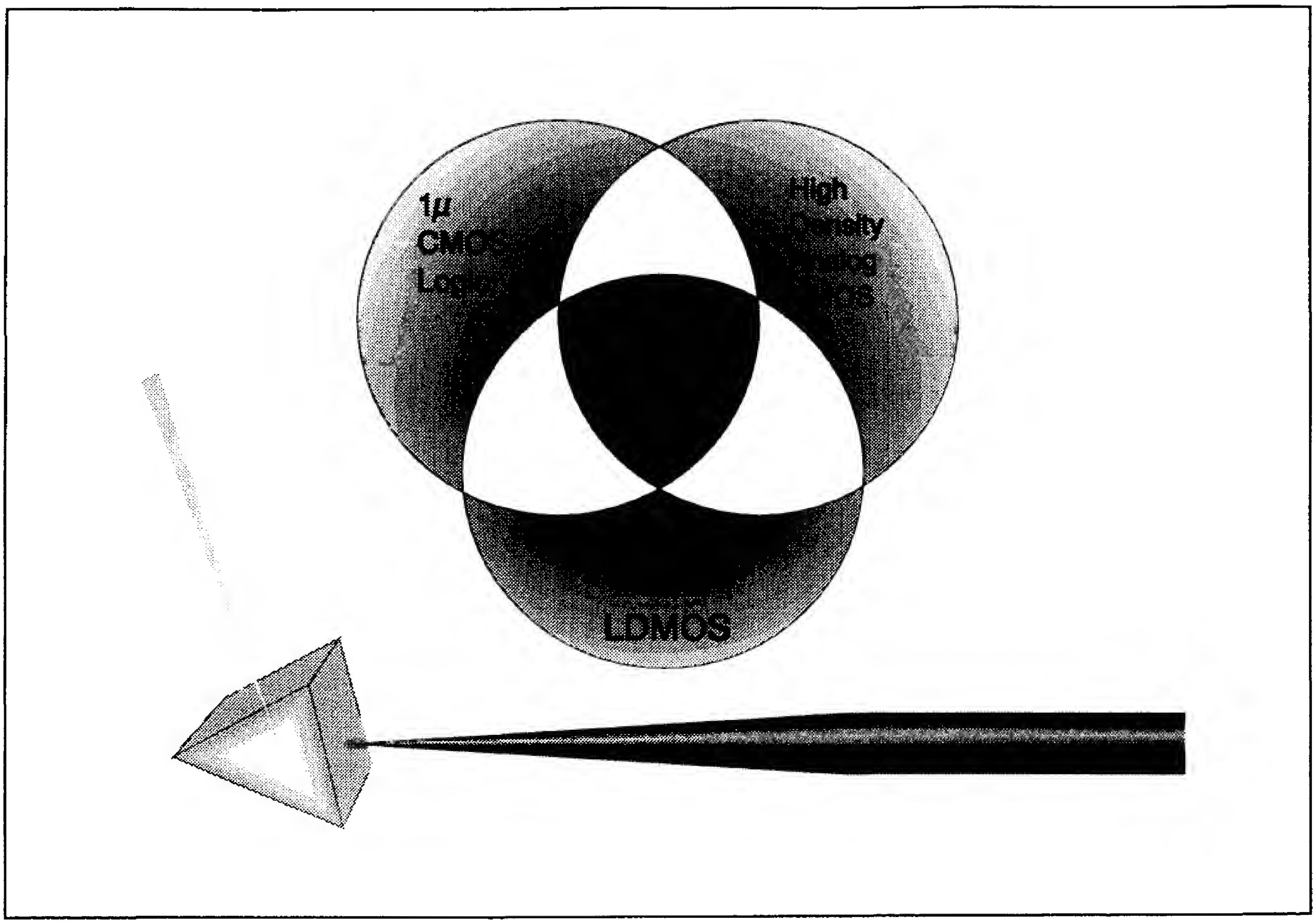


Figure 5.1.4 - PRISM

PRISM is a mixed power, linear and logic process methodology that includes a Cell-based library for rapid design turnaround, analog and VLSI CMOS, EPROM and EEPROM, with LDMOS power capability.

The spread of process modules available ensures that the highest levels of integration are possible, and the specialisation ensures that there is minimum performance compromise. Examples are the EEPROM process in PRISM that can be combined with LDMOS power devices, logic and linear to build an EE-programmable power product.

The logic might comprise a microprocessor, a state machine or random logic, dependant on the application. The linear elements might involve Op-amps, comparators, charge pumps, regulators and FET drivers. Many of these functions are to be found inside the TPIC family of products.

1.4 Technology trends

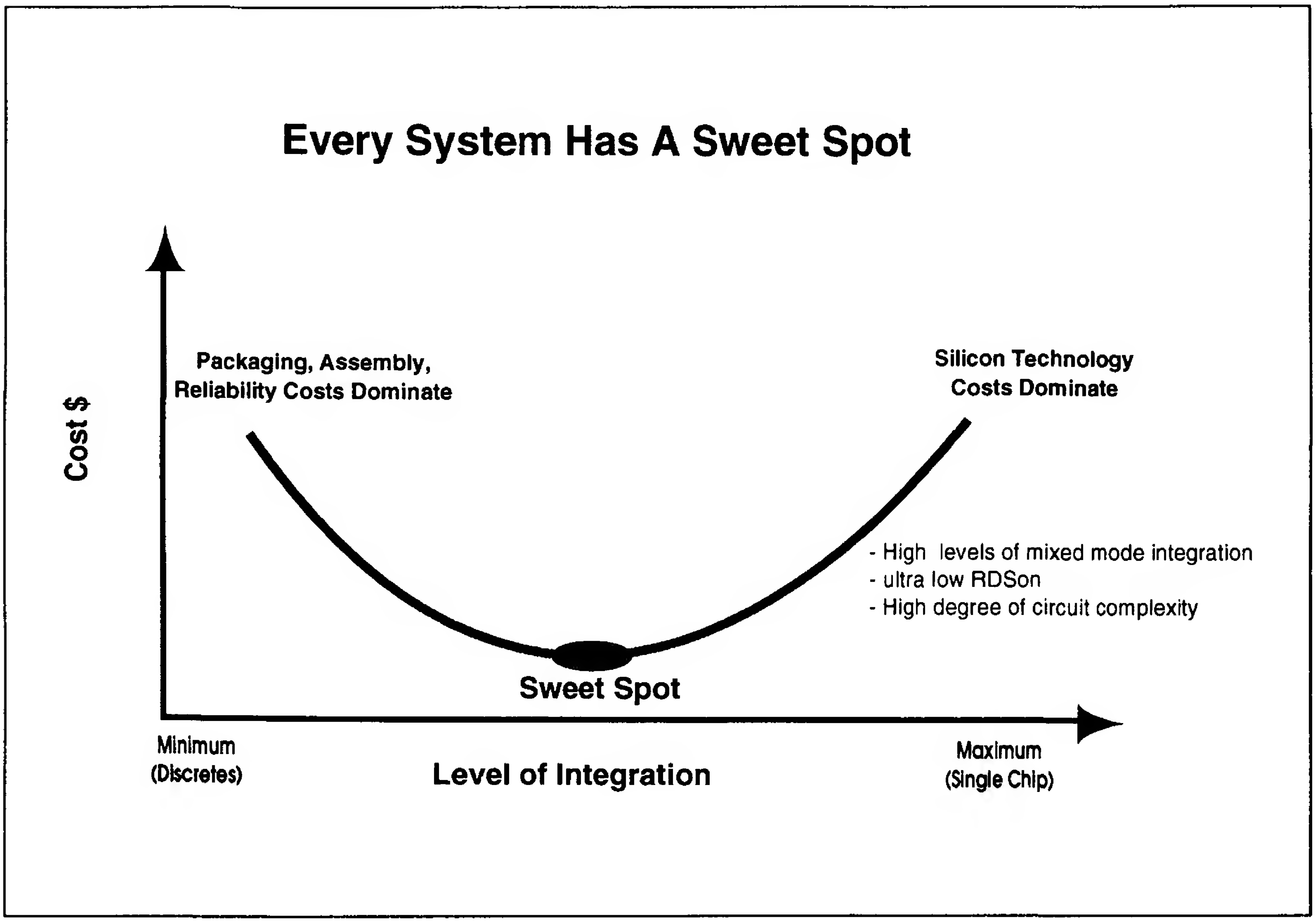

Every System Has A Sweet Spot
Cost $
Packaging, Assembly, Reliability Costs Dominate
Silicon Technology Costs Dominate
- High levels of mixed mode integration
- ultra low RDSon
- High degree of circuit complexity
Sweet Spot
Minimum (Discretes)
Level of Integration
Maximum (Single Chip)

Figure 5.1.5 - Finding the sweet spot

Often solutions to system problems cluster around a "sweet spot" where the trade-offs balance out to provide a good general solution. This is often the case with power and intelligent power ICs.

Successful power ICs tend to have output capabilities that are usually less than an amp or two, with the occasional exception. Higher currents are possible, and become more possible with time, but they rarely appear on highly integrated devices.

At the high integration end of the scale, discrete solutions can cost less than highly integrated ones which require complex fabrication processing. An example would be a 32-bit micro with an array of 20-Amp switches, EEPROM, an ADC, DAC, etc. All this is possible in PRISM, but it is probably cheaper today if the large switches are in an off-chip array.

At the low end of the integration scale, costs start to rise again as package count increases. To take an extreme example, no-one expects to build a standard op-amp or NAND gate from discrete transistors. Another example would be an 8-pin opamp being replaced by a large number of 3-pin transistors, plus passives. This increases the interconnections and affects reliability adversely.

The most important point to be made here is that the "sweet Spot" is NOT fixed. It moves with new developments, and with the acceptance of new solutions. In general silicon technology improvements result in smaller physical size, and this will in time favour higher integration.

As a result of recent process innovations, the "Sweet Spot" for Power+(tm) ICs is moving away from the traditional 1 or 2 Amp products with minimal integration, and it is moving in two directions.

The first direction is the obvious one - higher current, higher integration and lower on-resistance are continuing goals - but the way they have been achieved brings lower specific on-resistance to all devices.

Thus the size and dissipation of smaller devices is reduced proportionally. They become better able to be associated with greater amounts of logic, and to be available in smaller packages - eg surface mount, and specifically SO packages. This means that new product families will be appearing at both ends of the power spectrum.

1.5 Power+ Products

Power+ Arrays

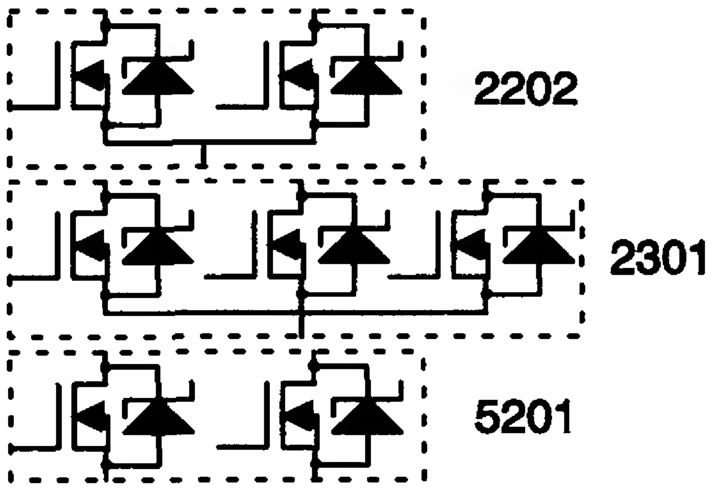
- TO220 Arrays:-

  60V, 7.5/15A, 90mOhm, 120 mJ

  TPIC2202KC - Dual Mosfets

  TPIC2301KV - Triple Mosfets

  TPIC5201KV - Dual (separate)



- DIL Sept Array (7)

  60V, 0.5/2.5A, 0.5 Ohm, 22 mJ

  Pinout is identical to ULN 2001/2/3/4

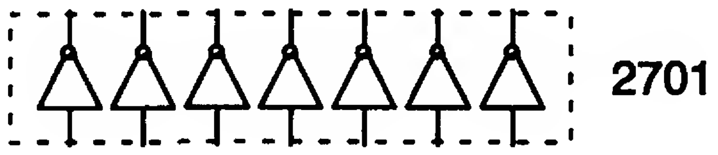


Figure 5.1.6 - Power+ Arrays

1.5.1 Power+ Arrays

Here the Power+ Array family is shown in brief. These devices are monolithic configurations of LDMOS switches in single packages.

The TO220 arrays offer 90 mOhm switching at the voltages and currents shown. The two Dual devices, the TPIC 2202 (common-source) and the TPIC 5201 (separate devices) offer a choice when (eg) building H-bridge configurations. These are shown later in the applications sections. The TPIC 2301 is a Triple common-source device in the same 7-lead TO220 package as the TPIC 5201.

The TPIC 2701 is a Sept (7 FETs) device with common sources and an output clamp pin. Its performance is less dramatic than the TO220 arrays, but it is considerably more capable than the ULN200x series with which it is pin compatible. It offers higher current capability over the same temperature range, better dissipation, and a specification that extends to 125 deg C as opposed to 85 deg C.

The avalanche energy value (22 mJoules) encourages its use in inductor driver design due to its guaranteed switch-off capability. This can help prevent the type of mysterious occasional failures experienced with bipolar arrays when used without adequate snubbing networks, or reduce snubbing network costs.

Power+ Logic

- TPIC 6xxx series - 0.25A, 1.5A pk, 45V, 1.3 Ohm, 75 mJ, 20 pin DIL or 20-pin SO package.

  TPIC 6259 - 8-bit addressable latch
  TPIC 6273 - Octal D-type latch
  TPIC 6595 - Octal SIPO (shift register)

- TPIC 6Axxx series - 0.35A, 1.1A limit, 50v, 1 Ohm, 75 mJ, in a 20-pin DIL

  TPIC6A259 - 8-bit addressable latch
  TPIC6A595 - Octal SIPO (shift register)

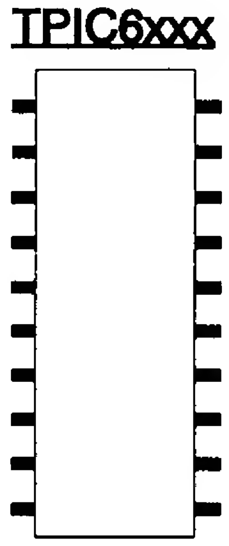


Figure 5.1.7 - Power+ Logic

1.5.2 Power+ Logic

The Power+ Logic family contains multiple power switches with high speed logic drivers. The nomenclature borrows from standard 74 series logic families. The input logic is as the part number suffix suggests, and the outputs are LDMOS FETs. There is current limiting on the enhanced 6Axxx parts, as well as the improved specification shown in figure 5.1.7.

With their high speed CMOS input logic, the serial parts are particularly effective in driving large arrays for display purposes; the shift register architecture minimises interconnects when driving large banks of LEDs, lamps or mechanical flippers in (eg) airport departure/arrival display systems. The 6Axxx parts are particularly useful when driving incandescent lamps, since their current limiting extends the life of the lamps as well as protecting the device against short circuits.

Power+ Intelligence

- TPIC 2404 - Quad LSS (Low Side Switch) with diagnostics & Fault O/P.

  45V, 1A, 1.5A limit, 0.8V Sat, 40 mJ, in a 15-pin ZIP (Zigzag inline)
  Output diode clamps are provided, with overvoltage, thermal, and over-current shutdown.
  This part is featured in "Stepper motor Applications" SLDTE01

- TPIC 2802 - Octal SIPO (Shift Register) with diagnostics and PISO.

  35V, 1A, 1.8A limit, 1.4V Sat, 40 mJ, in a 15-pin ZIP
  45V transient clamps on-chip, 20 mW standby power,
  PWM and absolute value current limit.
  This part replaces TPIC2801, which is featured in
  the application report SLDA002

Figure 5.1.8 - Power+ Intelligence

1.5.3 Power+ Intelligence

The Intelligence part of the "Power+ Intelligence" family reflects the ability of the device to sense the state of its power outputs, report faults, and feed data back to the controlling micro, logic system, or ASIC. This can save large amounts of external circuitry.

The TPIC 2404 is a useful output device with logic level inputs, and individual current and thermal limits on the outputs that turn off the drivers and signal a fault. Exceeding the overvoltage limit will also turn off the outputs and enable the fault output, as will open load/short to ground. Using the truth table on the data sheet, full output diagnostics can be carried out by toggling the inputs and reading the data output.

The TPIC 2802 replaces the popular TPIC 2801, its darlington outputs giving improved gain, and reducing current consumption as a result. The SIPO (Serial In Parallel Out) architecture is extended to allow PISO output readback from the serial out pin; this enables the output states to be interrogated remotely. Output protection includes a current limit with both PWM and absolute peak limits, and out-of-saturation voltage protection.

2 Output System Design

2.1 Selecting a load device

This involves defining the type of output energy needed and selecting the correct size and class of load.

The next step is evaluation of the input requirements that address the voltage and current requirements during normal operation. Normal operation includes load switching (turn on, turn off and accompanying transients).

Often the behaviour of a load during switching is not adequately specified by the maker and must be characterized for the specific application. This implies evaluating the system under operating conditions, examining the load behaviour, and then redesigning if necessary.

It cannot be stressed too highly that the approximations and rules of thumb that work for small signal devices do not always work in a power system. Current can be found flowing the "Wrong" way - especially in inductive circuits. Inductive portions can be found in many nominally resistive power circuits. This is due to the high currents, or high dI/dT appearing in (eg) the ground leads, generating unwanted ground offsets. It is recommended strongly that an oscilloscope be used to view the dynamic conditions of both voltage and current through the switch, and that this be used to inform any redesign.

2.1.1 Resistive loads, Capacitive loads, and Inductive loads

Resistive loads are simplest, since sizing is largely a question of examining the current and voltage specification, estimating dissipation, making allowance for duty cycle, then allowing margins for safety. It is always worth checking the load for unsuspected inductive and capacitive components.

Incandescent lamps however, have a rapid initial current surge that reduces with time. These loads need care to ensure that the peak current is less than the switch limit - or a switch that provides its own current limit.

Current Limit can be more economical in many cases than just using an "overkill" device, since an incandescent lamp bulb may peak at 4A, before settling to 1A nominal. A 4A MOSFET is likely to be 4 times the area of a 1A MOSFET, with consequent cost increase, when a protected 1A device is adequate to the task, substantially smaller and therefore cheaper to make, and increases the life of the bulb.

Capacitive loads are comparatively rare - often stray capacitance is the only capacitive element in an otherwise resistive load. Where they are encountered, the principal danger arises from the high initial current into the (initially → Ø Ohms) load, which must be limited in some way if the switch is not to suffer - a switch with current limit is ideal.

Inductive loads can be complex to deal with, and energy can be passed from switch to load and back again to the switch. This energy must then be dissipated without damage, and a well-specified avalanche energy value for the switch device is helpful here.

Inductive loads usually have a significant resistive (and a small capacitive) component as well. Care must be taken to ensure that the energy return is fully understood and dealt with at the design (or re-design) phase. It is therefore important when driving inductive loads to use devices whose avalanche energy is fully specified, or to use other methods of protection such as snubbers, diode or zener diode clamps.

In the latter case, it can be beneficial to clamp to a voltage higher than the supply voltage, but lower than the specified device voltage; the higher voltage spike is usually of shorter duration, and therefore has less energy to dissipate, which means cooler running.

Load Categories

- Resistive - Imax, Vmax, dissipation and duty cycle predominate. Lamps exhibit a high initial current surge.
- Capacitive is usually in combination with resistive/inductive.
- Inductive loads can be complex in a number of ways..... The energy storage and return is the most critical to understand and control, and to do this, the MOSFET avalanche energy needs to be specified clearly.

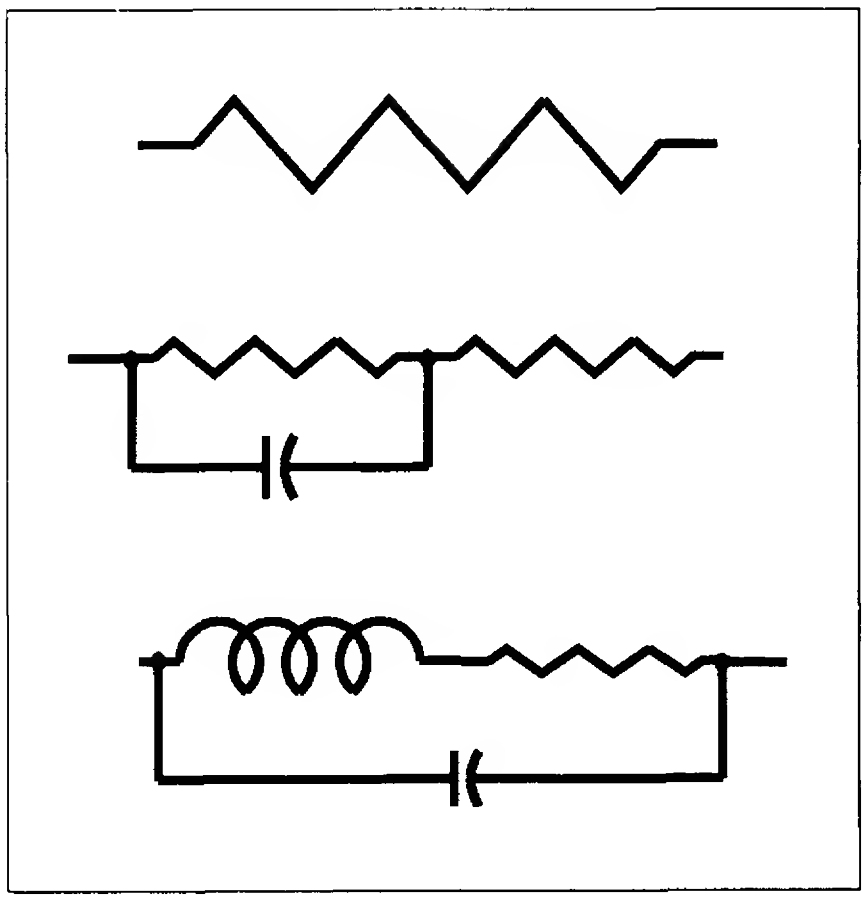


Figure 5.2.1 - Categories of Load

2.2 Interface Circuit Requirements

If we assume that the interface circuit is a switch then what do we need to know in order to select the right switch?

Motors, solenoids, lamps and other assorted loads are generally specified by operating voltage and current. The information provided is sufficient for operating at continuous duty. However, in most applications the load is being switched on and off. When switching loads the operating requirements as well as transient conditions must be considered. The power requirements are often further influenced by dynamic operating conditions.

Inductive Load Switch Requirements

Inductive Load

- Current
  - Continuous
  - Turn On
  - Turn Off
- Operating Voltage
- Energy
  - Mechanical Output
  - Loss
  - Returned Energy

LDMOS switch

- Current
  - Continuous
  - Pulsed
- Dissipation
- Drain-Source volts
- Avalanche Energy
- Drain-Source Ohms

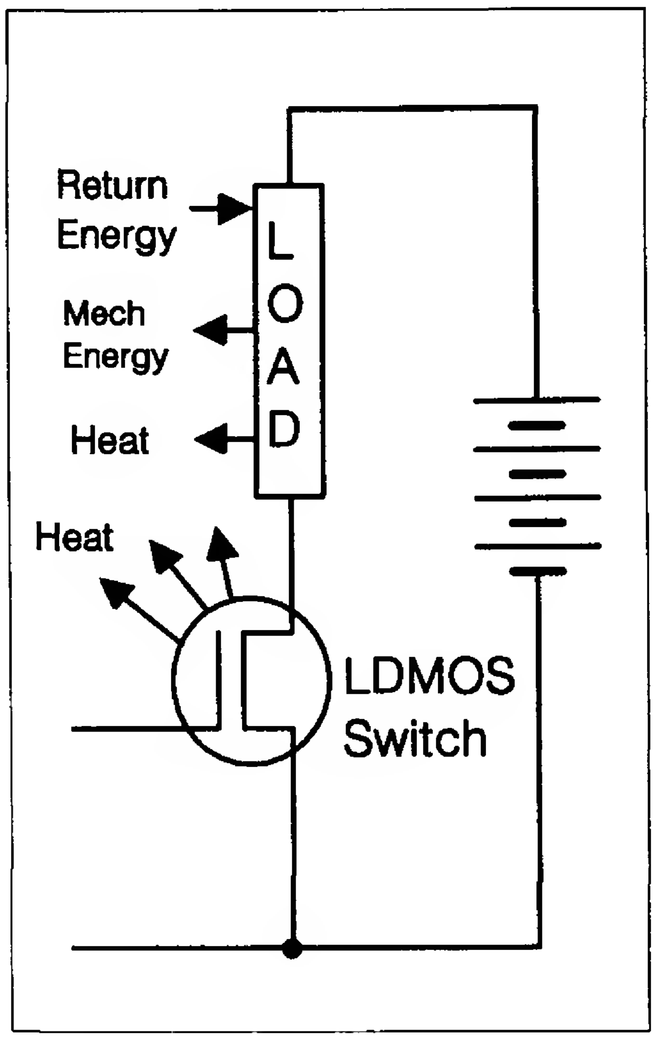


Figure 5.2.2 - Inductive Load Switch Requirements

The easiest way to look at load requirements is to consider the example in Figure 5.2.2, of a load operating from a battery and controlled by a low side switch. What is needed to design the switch and evaluate the system?

The system power supply and load choice will determine:

- Current drawn from the battery, including transients when the switch is turned on and off.
- Battery terminal voltage. (V)
- Energy output from the load (motion, sound, etc.)
- Energy dissipated from the load in the form of heat. (IR loss, magnetic loss, friction)
- Energy returned to system (inductive, regeneration, cross coupling)

These system load requirements must then be used to determine the switch requirements:

- Continuous source-drain current
- Pulsed drain current
- Continuous power dissipation @ $T_A = 25\ ^{o}C$
- Single-pulse avalanche energy (energy returned to the switch from back e.m.f.)

- Drain-source voltage (V_{DS})
- Drain- source on-state resistance ($R_{DS(on)}$)

Selecting or designing a switch is a three step process:

- Determine the total energy, current and voltage required
- Select a switching device which will accommodate the energy
- Evaluate the system power dissipation to determine any heat sinking requirements.

2.3 Determining the Total Energy

This begins with evaluating the load current during operation and during switching.

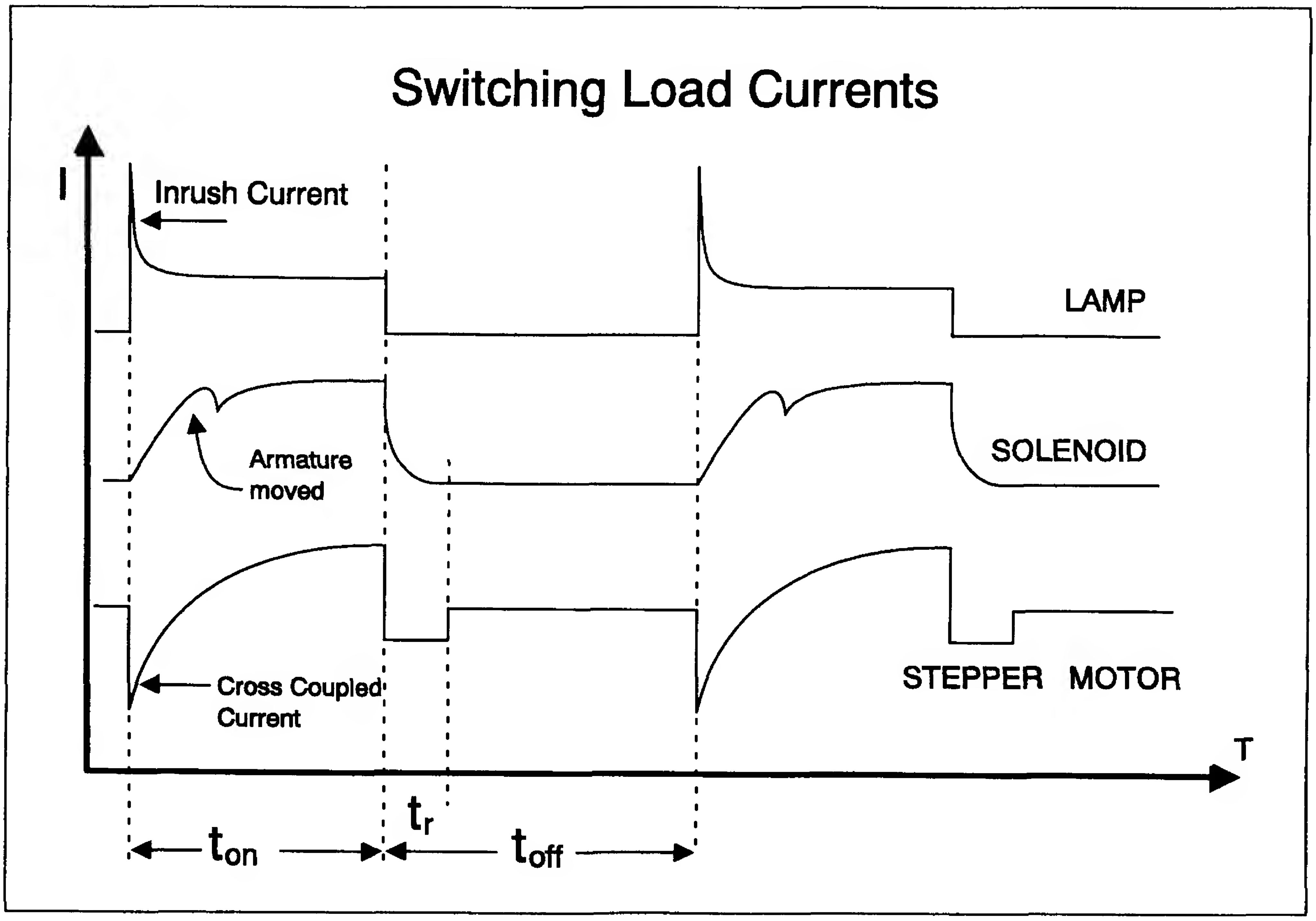


Figure 5.2.3 - Switching Load Currents

Figure 5.2.3 shows the current waveforms for an incandescent lamp, a solenoid and a stepper motor. This diagram depicts steady state and switching conditions which must be considered in controlling a load.

The incandescent lamp current shows a high inrush value at turn on, (t_{on}) due to the difference in filament resistance when cold and hot, decreasing to a steady current value until turn off (t_{off}), and then a clean turn off with no current flowing after t_{off}.

A lamp control switch will need to withstand high peak currents or limit the current until the lamp filament warms up. The latter approach is preferable, since it extends the life of the filament.

The solenoid current starts at t_{on}, increases until t_{off}, and continues to flow until t_R. The change in current slope between t_{on} and t_{off} is caused by the solenoid armature moving closer to the coil and increasing the coil inductance. The current flow between t_{off} and t_R is a result of the magnetic field in the solenoid collapsing and returning energy to the system.

A solenoid switch must be capable of conducting the coil operating current and the system must provide a method for accommodating the energy returned to the system at turn off. Several methods are employed to deal with the returned energy, which when it is dissipated in the switch is referred to as avalanche energy.

The stepper motor exhibits a exponential current increase characteristic of an inductive load. Return energy is a factor in stepper motor control. Additionally stepper motor windings can produce currents as a result of cross coupling from adjacent motor windings; this is particularly true for unipolar stepper motors. A control circuit for a stepper motor such as depicted in Figure 5.2.3 must accommodate the transient energy at turn on and the returned energy at turn off.

Once the load characteristics are determined energy calculations can proceed.

Energy and Power Calculations for an Inductive Load

- Power-on time MOSFET dissipation

$$P_{on} = \frac{1}{3}(I_p^2)\, r_{DS(on)}\, d \qquad \text{For } \frac{R}{L} >> t_{on}$$

- Back emf energy

$$E_T = \frac{3\, L\, I_p^2\, V_{CL}}{6\,(V_{CL} - V_{SS}) + 4 R_L I_{DM}}$$

- Power off dissipation

$$P_{off} = E_T f$$

- Total average switch power dissipation

$$P_T = (P_{on} + P_{off})n + P_{(quies)}$$

L = Load Inductance
I_p = Peak Drain Current
V_{CL} = Max O/P Clamp Voltage
V_{SS} = Load Supply voltage
R_L = Inductor Resistance
f = Switching frequency
d = Duty Cycle
$r_{DS(on)}$ = Drain to Source Resistance
n = Number of switches Operating
$P_{(quies)}$ = Quiescent Disipation of Switch
t_{on} = Switch On Time

Figure 5.2.4 - Energy and Power Calculations for Inductive Loads

The energy calculations for an inductive load are presented in Figure 5.2.4. The intent is to calculate the total power dissipated in the transistor switch.

Power dissipated during switch "on" time is calculated as follows:

During the power-on time the inductor's current approximates to a linear ramp, assuming the inductors L/R_L time constant is much greater than the turn on time (t_{on}). This results in a mean square drain current of $1/3\ I_P^2$ with I_P equal to the peak drain current. Therefore the average power dissipated in the output MOSFET, P_{on}, is equal to:

$$P_{on(av)} = 1/3\ (I_P^2)*r_{DS(on)} * d$$

This assumption would be applicable to the stepper motor waveform in figure 5.2.3, but would not work for the solenoid. The solenoid time constant L/R_L is less than t_{on}, therefore P_{on} will be greater than that calculated above.

Power dissipated during switch off time is calculated as follows:

When the output MOSFET is turned off, the back e.m.f. generated by the inductor raises the drain voltage, which must be clamped either externally or internally. External clamping is normally accomplished with a snubber diode. Internal clamping is also accomplished with a zener diode; the clamp voltage V_{CL} is also called the avalanche voltage.

The equation to define avalanche energy is:

$$E_T = (3 * L_H * I_P^2 * V_{CL})/(6 * (V_{CL} - V_{SS}) + 4 * R_L * I_P) \quad \text{.. JEDEC Standard No. 10;}$$

This equation assumes a linear decay of the current in the inductor. A more accurate calculation of E_T can be derived by integrating the inductor current and clamp voltage in the load from turn off until the inductor current decays to zero as follows:

$$E_T = \int_0^{t1} V_{CL} * I_L * dt;$$

$$I_L = (I_P + (V_{CL} - V_{SS})/R_L)\ e^{-(R_L/L)t} - (V_{CL} - V_{SS})/R_L\,;$$

$$I_P = V_{SS}/R_L\ (1 - e^{-(R_L/L_H * d/f)})\,;$$

$$t_1 = L/R_L * \ln[1 + (I_P * R_L/(V_{CL} - V_{SS}))]$$

$$E_T = V_{CL} * L_H/R_L * (I_P - (V_{CL} - V_{SS})/R_L * \ln(1 + (I_P * R_L)/(V_{CL} - V_{SS}))$$

The power dissipated during the turn-off period, P_{off}, can be equated to the product of E_T and the frequency of switching

$$P_{off} = E_T * f$$

Hence the total power, P_T, dissipated in an integrated switch with multiple output sections is:

$$P_{T(av)} = (P_{off} + P_{on}) * n + P_{(quies)}$$

This is the average power dissipation for multiple sections whose duty cycles have a fixed time relationship to each other. For multiple outputs with variable duty cycles the power calculation becomes more difficult.

Where,

E_T = Total turn-off transient energy absorbed
f = Switching frequency
d = Duty cycle
L = Load Inductance
I_P = Peak output load current
n = Number of output switches operating
P_{off} = Turn-off power dissipation in each switch
P_o = On-state power dissipation each switch
$P_{(quies)}$ = Interface device bias power dissipation
$P_{T(av.)}$ = Average total power dissipation
R_L = Resistance of inductor
V_{CL} = Clamp voltage
V_{SS} = Load supply voltage

2.4 Thermal Considerations

With the device total power dissipation calculated now a thermal evaluation can proceed. The objective is to determine if external heat sinking will be required.

Thermal Considerations for Power Switches

Typical Heat Sink Performance:-

- Max Power Dissipation :-

$P_{MAX} = (T_{J(MAX)} - T_A) / \theta_{JA}$

- Thermal Resistance :-

$\theta_{SA} = \frac{T_J - T_A}{P_{T(AV)}} - \left|(\theta_{JC} + \theta_{CS})\right|$

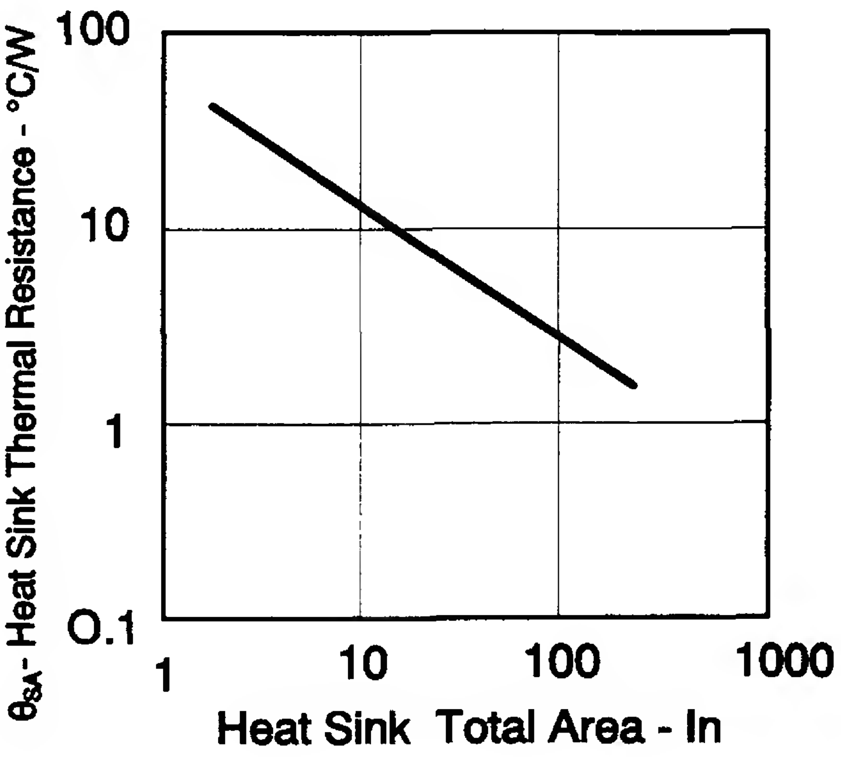


Figure 5.2.5 - Thermal Considerations For Power Switches

The requirement for external heat sinking is calculated based on the device's total average power dissipation, maximum junction temperature, and ambient operating temperature. The maximum power which can be dissipated in a device (P_D) can be determined as follows:

$$P_D = (T_J - T_A) / (R_{\theta JA})$$

Where: T_J = Maximum device junction operating temp.

T_A = Maximum ambient operating temp.

$R_{\theta JA} = \theta_{JA}$ = Junction to ambient thermal resistance, °C/W

T_J and $R_{\theta JA}$ are taken from the device specification and TA is determined by the application environment.

Is a heat sink required?

If the total power dissipated in the device P_T exceeds the maximum power dissipation P_D then either a heat sink must be used or a different device must be selected.

A heat sink size can be determined by first calculating the required heat sink to ambient thermal resistance $R_{\theta SA}$ as follows:

$$R_{\theta SA} \quad = [(T_J - T_A)/P_{T(AV)}] - [R_{\theta JC} + R_{\theta CS}] \qquad (\theta_{SA})$$

Where:

$R_{\theta JC}$ = device junction to case thermal resistance (θ_{JC})

$R_{\theta CS}$ = case to heat sink thermal resistance, °C/W (θ_{CS})

= 0.5 /W typical with thermal joint compound

$P_{T\,(AV)}$ = total average power dissipation, W

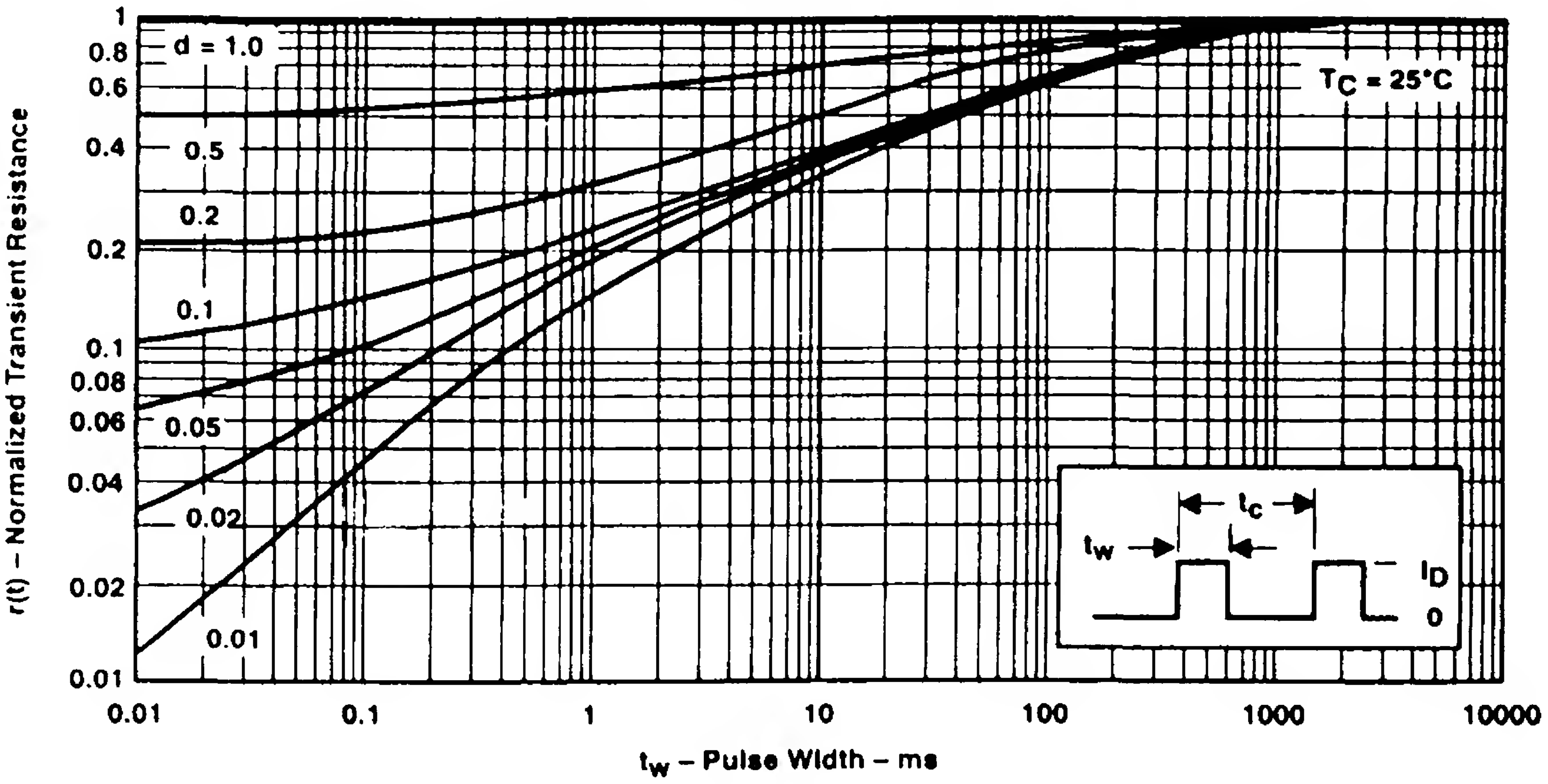
T_J = junction operating temperature, °C (from data sheet)

T_A = operating ambient temperature, °C

The $R_{\theta SA}$ required can now be compared to heat sink design specifications to determine the design type and size required.

THERMAL INFORMATION

NORMALIZED TRANSIENT THERMAL IMPEDANCE
vs
SQUARE-WAVE PULSE WIDTH



NOTES: $Z_{\theta JC}(t) = r(t)\,R_{\theta JC}$
t_w = pulse width
t_c = period
d = duty cycle = t_w/t_c

Figure 5.2.6 - Power+ Arrays Thermal Impedance Characteristics

The preceding thermal calculations were based on the assumption that the device average power was duty cycle dependent. This is true if the pulse widths are short in relation to the device thermal time constant. An example would be a switch that is "on" for one hour in every twenty four hours. the actual duty cycle is low but your system must be designed to accommodate 100% on time for the switch. The graph in Figure 5.2.6 gives the times associated with the TO-220 Power+ Arrays.

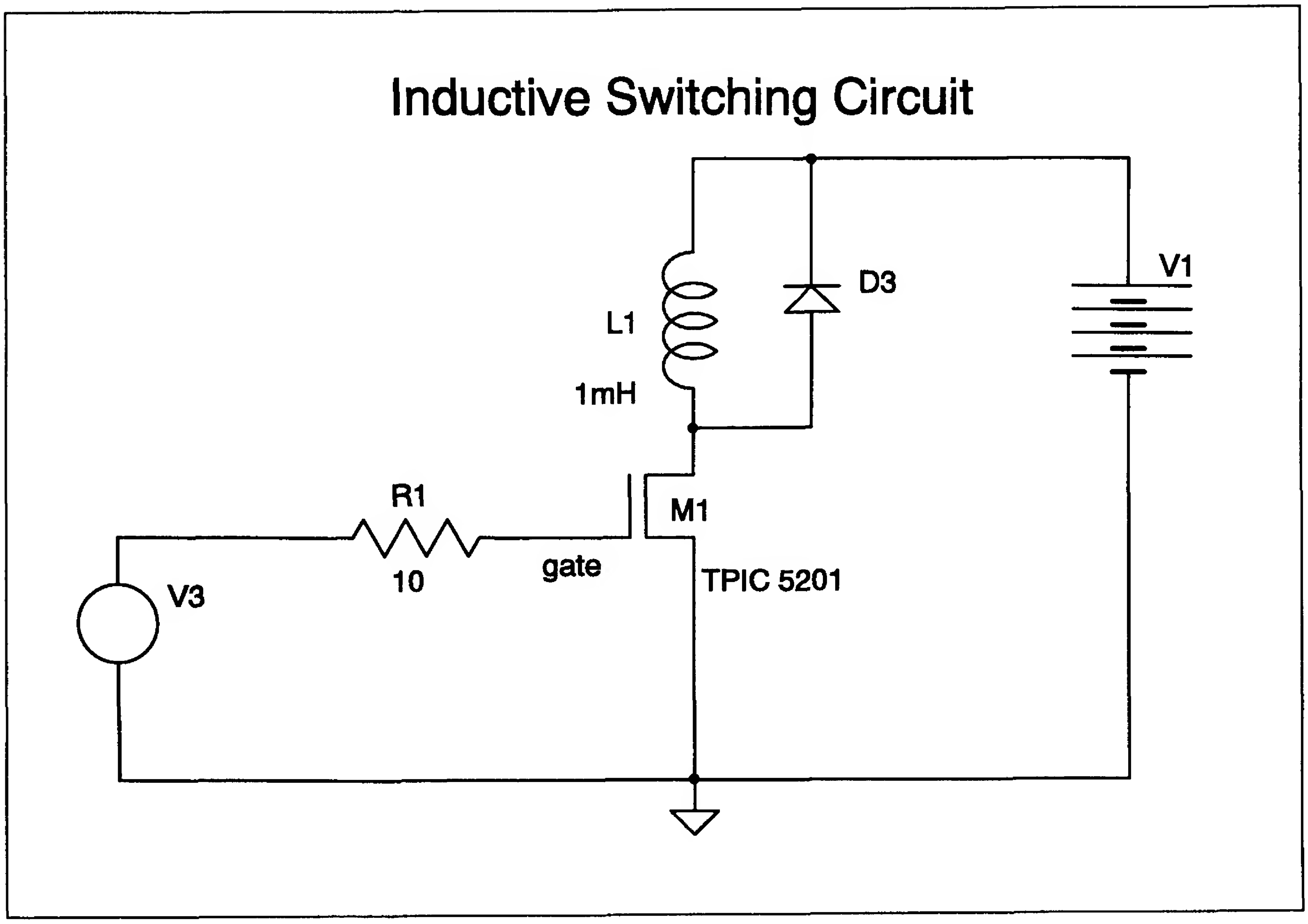


Figure 5.2.7 - Inductive switching circuit

2.5 Switching Speed

The delay and transition times that occur during the switching transients of the device can easily be determined with the aid of characterisation data given within the data sheet. Consider the simplified circuit diagram and associated waveforms shown in figures 5.2.7 and 5.2.8 in which is shown a typical inductive load whose recirculation current is being controlled by transistor M1.

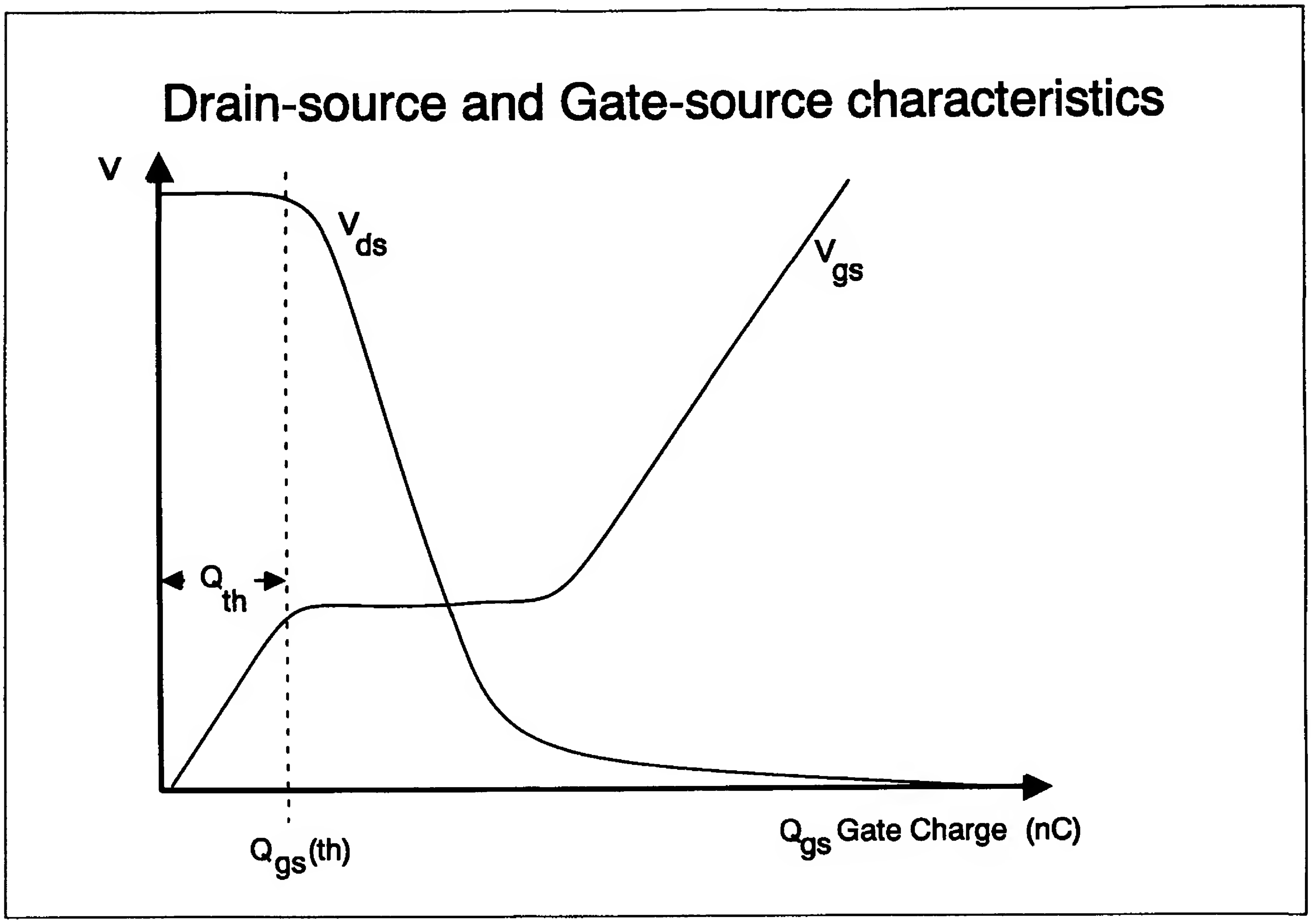


Figure 5.2.8 - Associated gate-source and gate-drain waveforms

In Figure 5.2.8, a useful mnemonic for the gate charge/time relationship is that a nano-Coulomb (nC) of charge is equivalent to 1 µs.. Thus the horizontal axis may be read directly in microseconds of delay, if the charging current is a constant 1 mA, or scaled to the current available.

The drain current of the mosfet is controlled by the gate source voltage. This relationship is shown in figure 8 of the TPIC5201 data sheet, and is elaborated below in figures 5.2.9 and 5.2.10.

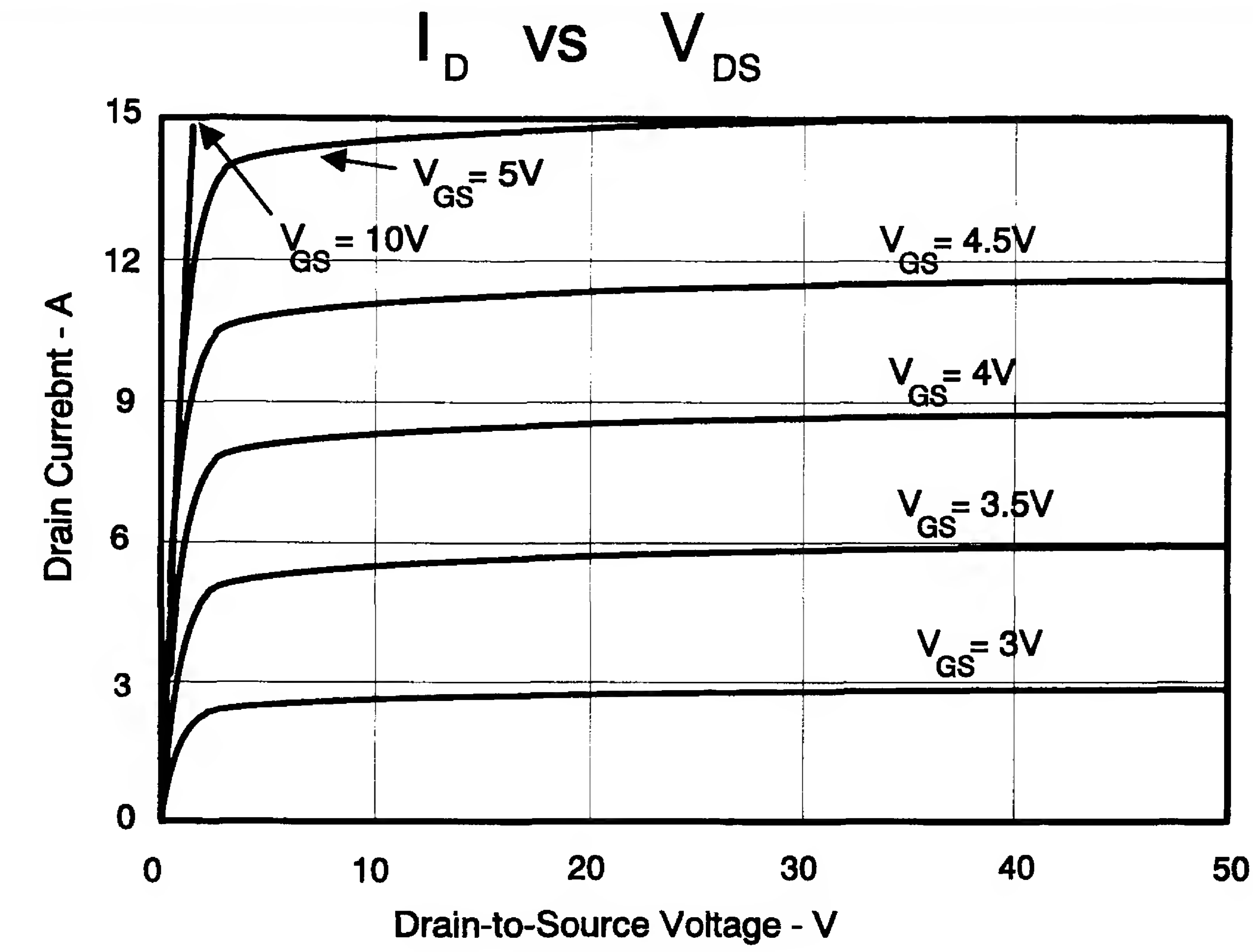


Figure 5.2.9 - TPIC5201 transfer characteristics

Careful study of figure 5.2.10 indicates three distinct regions of operation. Firstly, at low gate voltages, below the threshold voltage, V_{th}, the mosfet is in the off-state and no drain current flows. The threshold voltage is specified in the data sheet at 1mA as typically 1.75V. Above the threshold voltage the drain current is linearly related to the gate voltage by

$$I_d = g_{fs}(V_{gs} - V_{th}) \qquad \text{.................................(1)}$$

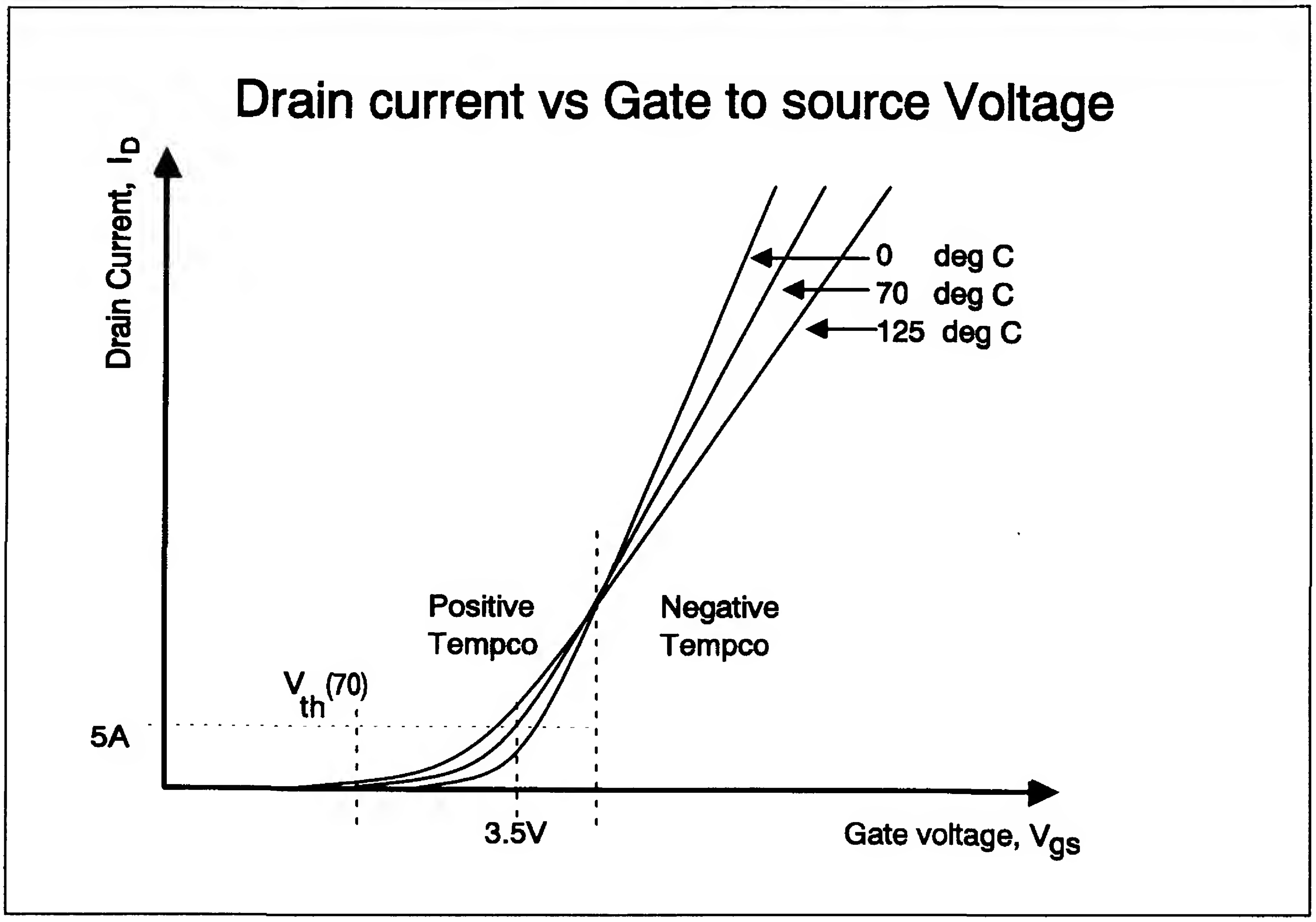


Figure 5.2.10 - Effect of Temperature on transfer characteristics

The data sheet specifies the magnitude of g_{fs} at 5A as typically 4.7 Siemens. The second region in figure 5.2.10 occurs between the threshold voltage and the point where the drain current exhibits a positive temperature coefficient with respect to the gate voltage. The third region occurs at gate voltages greater than this, where a negative temperature relationship exits between drain current and gate voltage.

Essentially, the dynamic input characteristics of the power mosfet may be regarded as capacitive, however, due to the physical construction of the device the terminal capacitances are a function of the applied voltage. Consequently, the dynamic relationship between actual gate voltage and the applied drive signal are best described by the use of charge transfer.

In figure 5.2.11 below is the gate charge waveform of a typical array device. In this figure, three regions may also be distinguished.

The first region is described by Qgs(th) and represents the charge required to raise the gate-source capacitance voltage to that necessary for control of the drain current. Fig 11 on the data sheet suggests a Qgs(th) at a drain current of 2.5A of typically 1.5nC.

The V_{gs} required to maintain a drain current of 5A may be obtained with the aid of the data sheet or figure 5.2.9 or 5.2.10 above as nominally 3.5V. An input capacitance may be associated with this region of low gate-source voltage, V_{gs} and is calculated as follows:

since, $Q = CV$ ....(2)

$$C_{in} = \frac{Q}{V} = \frac{1.5nC}{3.5V} \quad \text{.................................(3)}$$

=430 pF

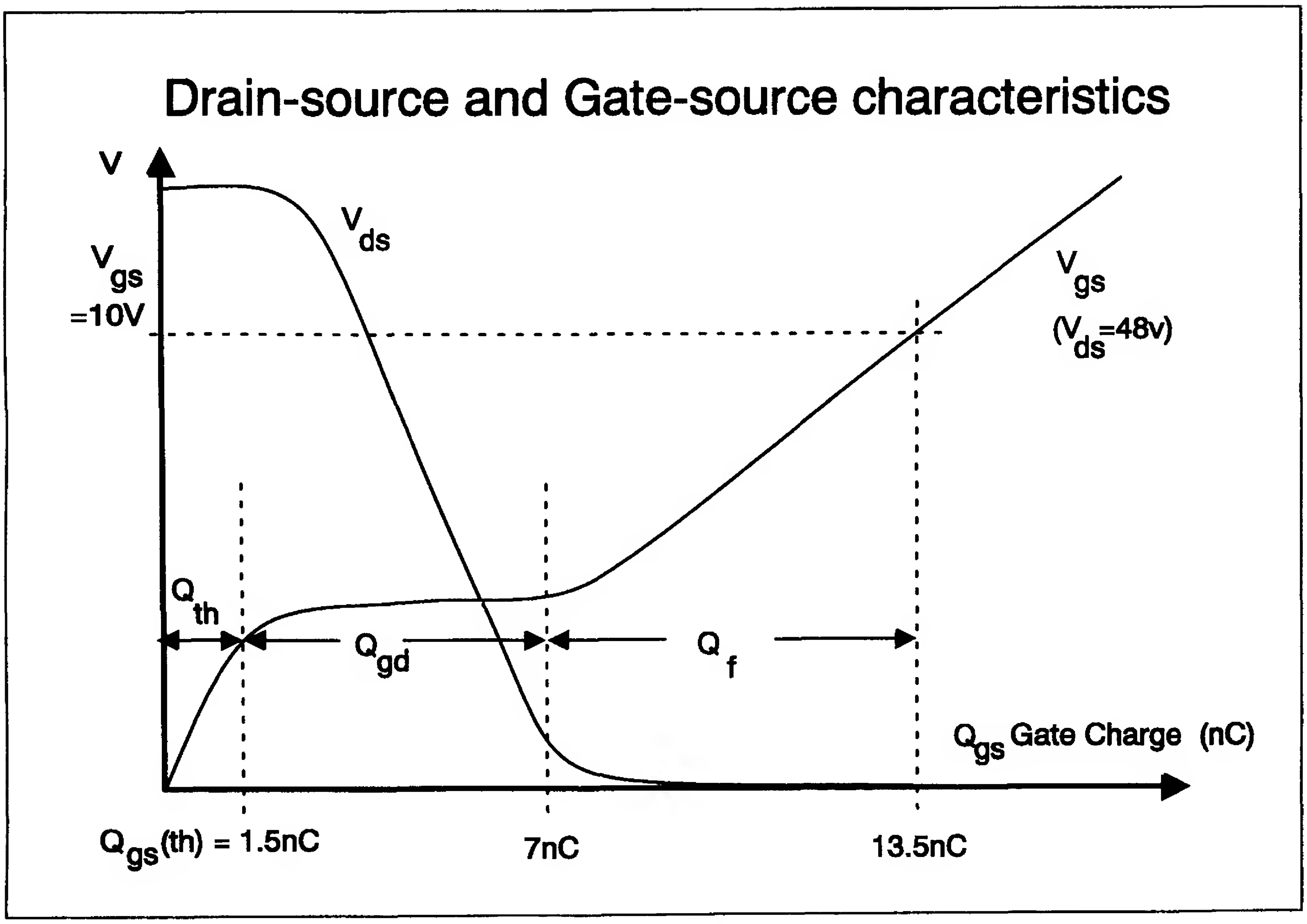


Figure 5.2.11 - gate charge waveforms

The second region, referred to as Qgd in figure 5.2.11 above, is the charge required to fully charge the gate drain capacitance, which is a function of the source-drain voltage.

Assuming the device is switching from a 48 volt rail, the magnitude of this charge is may be obtain from figure 5.2.11 above as:

$$7\text{nC} - 1.5\text{nC} = 5.5 \text{ nC}$$

The third region given by: $Q_g - Q_{gd} - Q_{gs(th)}$ is the charge required to charge the input capacitance to the input drive voltage, and has no impact on the actual drain current. The difference between the initial and final slope of the V_{gs} vs. Q_g curve may be attributed to the difference in value of the drain-gate capacitance.

From a drive circuit perspective, it should be noted that the effective input capacitance, C_{in} does not have the same magnitude when the device is being turned on as when turned off. At turn on, the drain source voltage will be high, and a C_{rss} value at high V_{ds} and C_{gs} value at low V_{gs} would be appropriate, and at turn off capacitance values at low V_{ds} and high V_{gs} would apply.

The value of the appropriate input capacitance may also be obtained from the slope of the gate charge curve for high and low values of V_{gs}.

2.6 Calculation of Switching speeds

2.6.1 Turn-on

The rise and fall times of the drain during switching may be limited by a number of factors relating to both the gate and drain circuits. It is assumed in the following analysis that the drain inductance and capacitance have a time constant that does not limit the drain slew rate and that the response of the device is controlled by the gate drive circuit.

The gate resistance seen by the device, R_g, is the sum of the intrinsic gate resistance and that of the drive circuit; 0.25 ohms is a typical value for gate input resistance. When the drive signal is initially applied, the gate capacitance, C_{in}, charges through the input resistance until the threshold voltage occurs: at this point, the drain starts to conduct current, and the input capacitance continues to charge to a voltage level that will sustain the drain current. The time taken for the gate RC network to reach the threshold voltage gives rise to a delay time, t_{delay}, which is given by:

$$t_{delay} = C_{in} R_g \ln\left(1 - \frac{V_{th}}{V_{gg}}\right)^{-1} \quad \text{..............................(4)}$$

where V_{gg} is the magnitude of the drive signal.

The gate voltage required to support the drain current is obtained from the transfer characteristics of equation (1) as:

$$V_{gs(active)} = \frac{I_d}{g_{fs}} + V_{th} \quad \text{.................................(5)}$$

Therefore, given a supply voltage ,V_{gg}, the rise time of the current to reach a value I_d is given by the time required for the input R_gC_{in} network to charge from an initial voltage of V_{th} to $V_{gs(active)}$. During this period , the drain current is given by:

$$I_d = g_{fs}\left\{ V_{gg}\left(1-\exp\left(\frac{-t}{C_{in}R_g}\right)\right)-V_{th} \right\} \quad \text{..........................(6)}$$

The sum of the rise time and delay time may be obtained from the equation(6) above by setting I_d equal to the load current, I_l, being switched.

$$\therefore t_{ri} + t_{don} = R_g C_{in} \ln\left(\frac{V_{gg}g_{fs}}{V_{gg}g_{fs} - I_l - V_{th}g_{fs}}\right) \quad \text{.....................(6a)}$$

Once the load current is established in the device , the drain voltage is free to fall from the supply voltage to its on-state voltage. In doing so, the gate-drain capacitance, C_{gd} must be charged; this charge will be supplied from the gate drive circuit. Since the drain current does not vary during this period, the gate-source voltage will be constant and the input gate current is given by:

$$I_g = \left(\frac{V_{gg} - V_{gs(active)}}{R_g}\right) \quad \text{..................................(7)}$$

Where the magnitude of $V_{gs(active)}$ is given by equation (5)

The rate of change of drain voltage is given by:

$$\frac{dv_{gd}}{dt} = \frac{I_g}{C_{gd}} \qquad \text{.......................................(8)}$$

Therefore, given a load supply V_{dd}, the fall time is given by:

$$t_{fv} = \frac{V_{dd} C_{gd}}{I_g} \qquad \text{.......................................(9)}$$

In practice, equation 9 is difficult to apply since the magnitude of C_{gd} is a strong function of gate-drain voltage. At low voltages the magnitude of C_{rss} ($C_{rss}=C_{gd}$) tends to increase significantly. Further, the magnitude of C_{rss} increases above this value for negative values of gate-drain voltage, which occur when the device is fully switched on. An alternative approach to calculating the fall time is possible by associating the plateau region of the gate charge curve with the charge necessary to fully charge the gate-drain capacitance.

The gate charge curves show that the total needed to fully charge the gate-drain capacitance is approximately 7nC (V_{ds}=48V), and therefore the charge required by the gate-drain capacitance is given by:

$$GateCharge = 7nC - Q_{gs(th)} \text{..............................(10)}$$

$$\therefore t_{fv} = \left(\frac{5.5nC}{I_g} \right) \text{.......................................(11)}$$

where I_g is given by equation 7 above.

2.6.2 Turn-off

During turn-off the gate source capacitance is discharged through the gate resistance R_g. However, due to the asymmetry of the gate charge curve, the turn-off and turn-on periods will be different.

It should be noted that the input capacitance, C_{in} does not have the same value as in the case of turn-on, since the gate-drain capacitance increases in magnitude as the source-drain voltage is reduced. The value of the appropriate capacitance may be obtained from the slope of the gate charge curve for high values of V_{gs}.

Initially, the gate capacitance discharges from the supply, V_{gg}, to $V_{gs(active)}$. Thus, by combining the RC discharge rate with the gate transfer function, the delay time is obtained:

$$V_{gs} = V_{gg} \exp\left(\frac{-t}{R_g C_{in}} \right) \text{..............................(12).}$$

$$t_{d(off)} = R_g C_{in} \left(\frac{V_{gg}}{V_{th} + \frac{I_l}{g_{fs}}} \right) \text{..............................(13)}$$

Once the gate voltage has fallen to $V_{gs(active)}$, the drain voltage is free to rise towards the supply voltage. As in the turn-on case, the gate-drain capacitance, C_{dg}, must be charged, and the voltage rise time is given by:

$$t_{rv} = \frac{C_{gd} V_{dd}}{I_g} \text{......................................(14)}$$

As previously noted, the plateau region of the gate charge curve is associated with the rise in drain voltage and may be used to derive an equation similar to equation (11).

When the drain voltage reaches the supply rail, the clamping diode is free to turn on and the gate voltage will discharge through the gate resistance and be given by:

$$V_{gs} = \left(V_{th} + \frac{I_l}{g_{fs}} \right) \exp\left(\frac{-t}{R_g C_{in}} \right) \text{..............................(15)}$$

Equation (15) may be used in conjunction with equation (1)to give the resulting drain current:

$$I_d = \left(I_l + g_{fs} V_{th} \right) \exp\left(\frac{-t}{R_g C_{in}} \right) - g_{fs} V_{th} \text{......................(16)}$$

The fall time is obtained by setting I_d=0 or by using the discharge rate of the gate resistance/capacitance combination i.e.

$$t_{fi} = R_g C_{in} \ln\left(1 + \frac{I_l}{g_{fs} V_{th}}\right) \text{.................................(17)}$$

2.7 Worked example:

Consider the case of switching the TPIC5201 with the following parameters:

R_g = 100, V_{gg} = 10, L = 10mH, I_l = 5A and V_{dd} = 48V.

The data sheet may be used to obtain the following:

1/ From the transfer curves, $V_{gs(active)}$ = 3.5V

2/ $Q_{gs(th)}$ = 1.5 nC

3/ V_{th} = 1.75 V

4/ g_{fs} = 4.7 S

The input capacitance for low V_{gs} values is

C_{in} = 1.5nC/3.5V = 430pF

The input capacitance for high Vgs is

$$C_{in} = \frac{Q_{gs}(10V) - Q_{gs}(3.5)}{10 - 3.5} = \frac{13.5 - 7}{10 - 3.5} = 1000 \text{ pF}$$

2.7.1 Switch-on

The delay time, t_{don} is given by application of equation (4) :-

$$t_{don} = C_{in} R_g \ln\left(1 - \frac{V_{th}}{V_{gg}}\right)^{-1}$$

$$t_{don} = 430 \times 10^{-12} \times 100 \times \ln\left(1 - \frac{1.75}{10}\right)^{-1}$$

$$=8.3\text{ns}$$

Equation (6) is used to obtain the rise time as follows:

$$t_{ri} + t_{don} = R_g C_{in} \ln\left(\frac{V_{gg} g_{fs}}{V_{gg} g_{fs} - I_l - V_{th} g_{fs}}\right)$$

$$t_{ri} + t_{don} = R_g C_{in} \ln\left(\frac{10 * 4.7}{10 * 4.7 - 5 - 1.75 * 4.7}\right)$$

$$\therefore t_{ri} = 100 \times 430 \times 10^{-12} \times 0.33 - 8.3ns$$

$$= 5.9 \text{ ns}$$

The voltage fall time is calculated by first calculating the gate current and using the charge transfer curve:

$$I_g = \frac{V_{gg} - V_{gs(active)}}{R_g}$$

$$I_g = \left(\frac{10-3.5}{100}\right) = 65mA$$

$$t_{rv} = \frac{7nC - 1.5nC}{65mA} = 84ns$$

2.7.2 Switch-off

the delay time is obtained from equation (13):

$$t_{doff} = R_g C_{in}\left(\frac{V_{gg}}{V_{th} + \frac{I_l}{g_{fs}}}\right)$$

$$t_{doff} = 100 \times 1000pF \times \frac{10}{1.75 + \frac{5}{4.7}}$$

$$t_{doff} = 355ns$$

the voltage rise time, t_{rv} is given by:

$$t_{rv} = {}^{\Delta Q_{gs}}\!/\!_{I_g} = {}^{(7nC - 1.5nC)}\!/\!_{35mA} = 157ns$$

$$\text{(where } Ig = \frac{0 - V_{gs(active)}}{R_g} = \frac{-3.5}{100} = \text{-35 mA)}$$

and the fall time is given by equation (17) as:

$$t_{fi} = R_g C_{in} \ln\left(1 + \frac{I_l}{g_{fs} V_{th}}\right) = 100 * 430pF * \ln\left(1 + \frac{5}{4.7 * 1.75}\right)$$

$$= 20 \text{ ns}$$

2.8 Conclusion

Defining the system output requirements leads to selection of a load, based on load output specifications.

From the load characteristics, system energy can then be calculated, and the load input specifications derived along with some switch assumptions.

A switch device can then be selected on peak and average power and energy calculations. Load analysis will then indicate whether external circuitry for back e.m.f. energy dissipation is needed.

For array devices, examination of the data sheet charge characteristic and gate drive available will give an estimate of the switching time of the output.

A thermal analysis based on the selected device thermal specifications will determine if additional heat sinking will be required.

The design of the switch section will be completed when actual measurements from the system are used to verify the design. These measurements must include dynamic measurements using an oscilloscope or similar method to view the current and voltage waveforms, verifying that they agree with the design assumptions.

This is the single most critical element of the design flow - testing and evaluating the prototype, and if in doubt, redesigning to add greater margins of safety, and then re-testing to confirm.

3 Applications - Stepper Motors

Stepper Motor Application

- Control Signal Interface:
  Serial link from logic or Micro
  CMOS Logic Levels
- Load definition:
  Unipolar Stepper Motor
  1A peak per winding
- Design Considerations:
  Peak Current
  Peak Voltage
  Recirculating Current
  Power dissipation

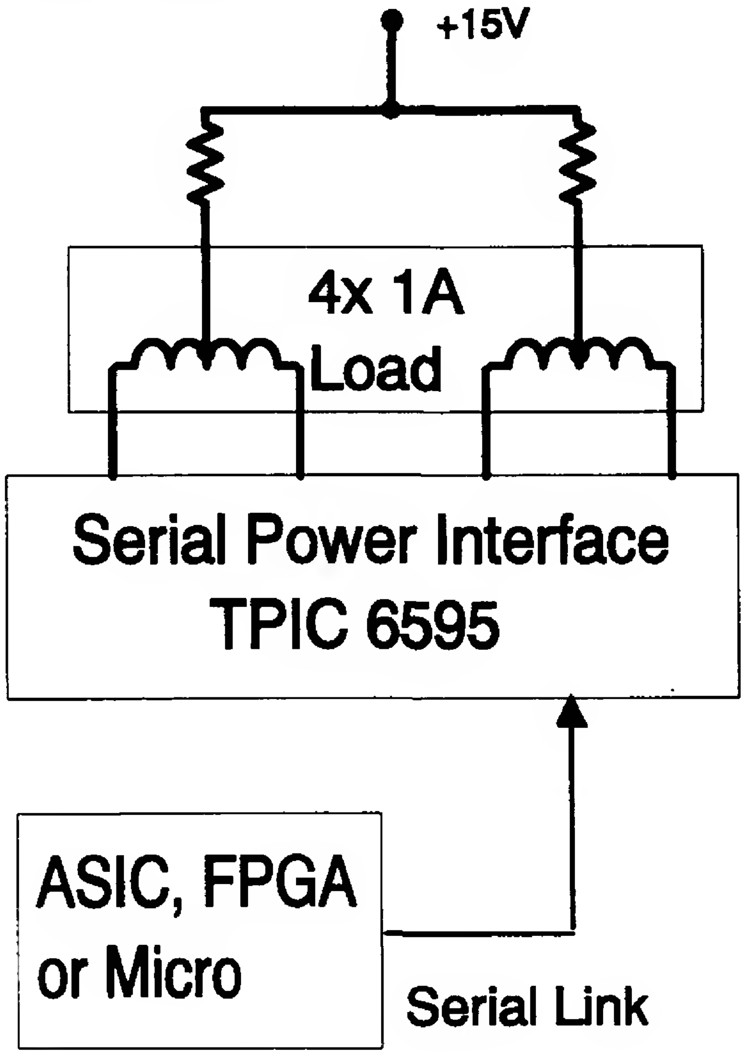


Figure 5.3.1 - One Amp Stepper Motor Application

3.1 One Amp Stepper Motor Application with serial interface

Stepper motors are often chosen to provide incremental rotating motion. Some typical applications are printers, copiers, and industrial robots. They are increasingly found in automotive systems, as more in-car functions are automated. Stepper motors present a multiple phase inductive load to the output circuit.

Figure 5.3.1 shows a block diagram of the application. The motor chosen has unipolar windings which require a peak current of 1A.

3.1.1 Load Description:

The first consideration in designing this application is to consider the load which in this case is a one amp unipolar stepper motor. The permanent magnet rotor stepping motor has two forms of stator winding. The bipolar stepping motor has a single winding on each stator pole and uses a full bridge to drive each phase winding. In the unipolar stepping motor, the flux reversal is accomplished by individually driving a bifilar winding on each pole.

The windings are phased such that when current is passed through one winding, a given flux direction is generated. By passing current through the other winding, the opposite flux polarity is produced. Thus, the overall magnetic effect is the same as the bipolar motor, but the phase windings can be more economically driven by interface devices with open-drain outputs.

The motor chosen for this application has unipolar windings. Due to the manner in which the windings are constructed a back e.m.f. voltage will be induced both in a winding that was turned off and in the other bifilar winding.

3.1.2 Energy Calculations

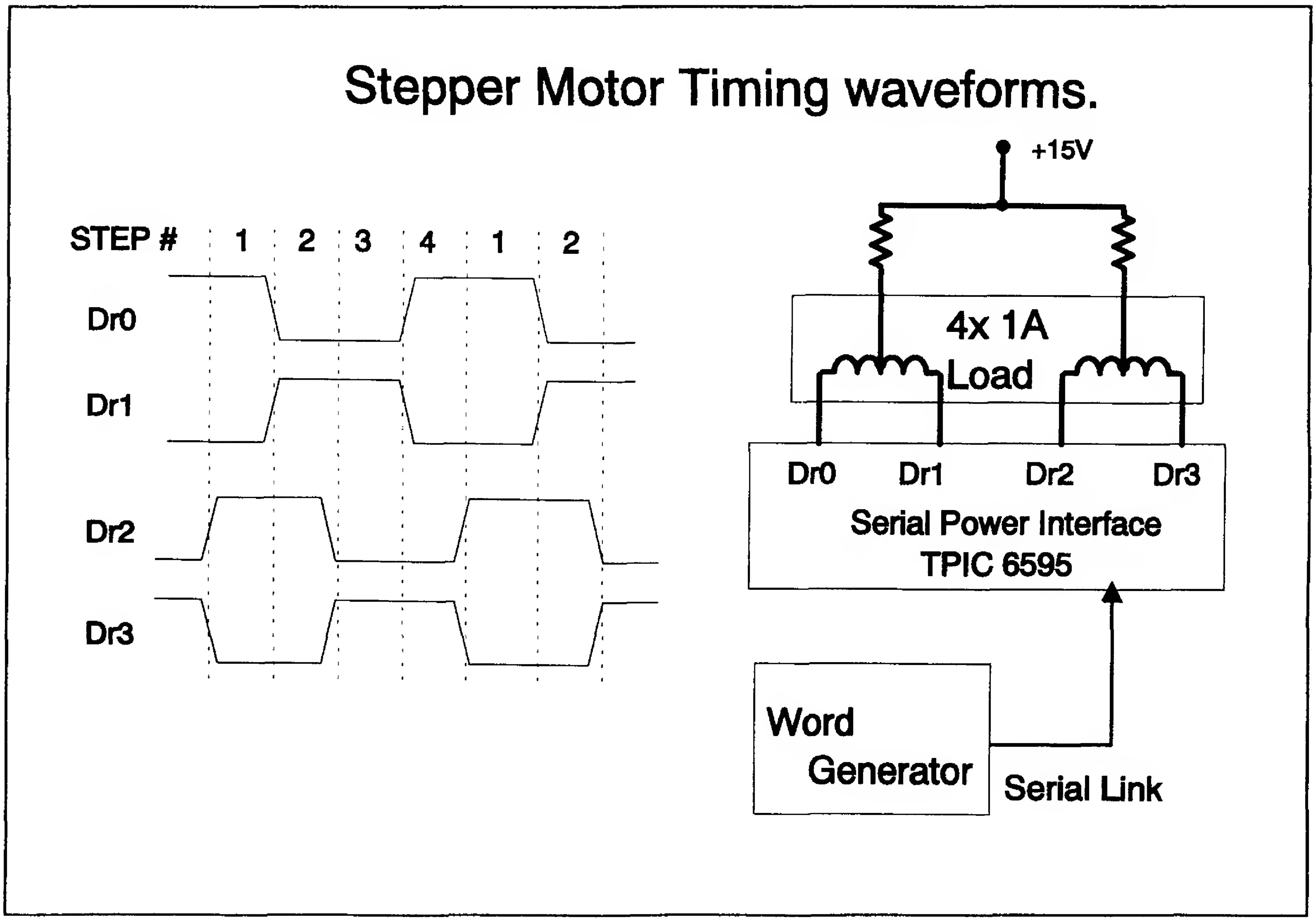


Figure 5.3.2 - Stepper Motor Timing Waveforms

Figure 5.3.2 shows a timing waveform of the stepping motor. The table in the lower right section shows the winding switching sequence. Additionally we can see that at any step two windings will be energized. With the knowledge that the windings are driven two at a time and by observation of the current waveform we can begin energy calculations. The value of back e.m.f. energy will remain the same as if it were all returned to one winding.

Observation of the timing diagram indicates t_{on} = 5 ms and that the winding current approximates a linear ramp (L/R >> t_{on}). This indicates that the simplified formula will be a good approximation.

Therefore:

$$P_{on} = 1/3\,(I_P^2)*r_{DS(on)}*d$$

Where d = 0.5 (each winding conducts twice in the four step cycle)

Note that in this example if the motor is stopped the current through each winding will be a steady 1 A. This brings up an important point. The power calculations are based on an assumed operating frequency. If the motor is stopped the individual drive currents may exceed the maximum continuous current rating of the switches. When calculating energy and power, worst-case assumptions must be considered.

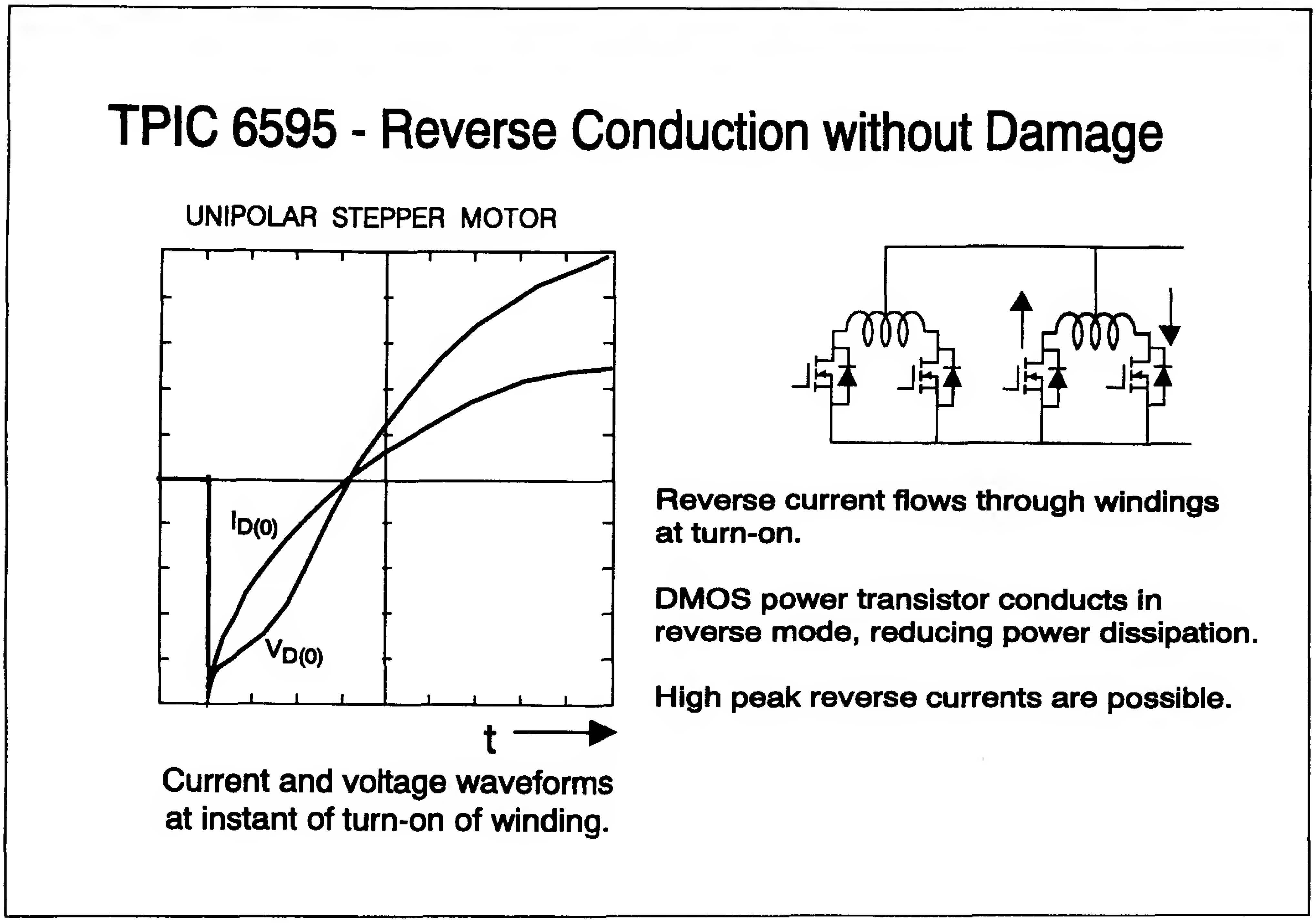
3.1.3 Choosing an Interface Circuit

Figure 5.3.2 shows a TPIC6595 that has been chosen for this application because it can meet the power requirements, can drive all four 1 Amp windings from a single integrated circuit, and includes interface logic.

The same figure also shows the TPIC6595 driving the stepper motor at its rated 1 amp by operating two output DMOS transistors in parallel. Drain 0 (Dr 0) is representative of output transistors 1 and 5 in parallel. Similarly, Dr 1 is representative of output transistors 2 and 6, etc. Anti-parallel source-drain diodes are omitted for clarity.

In this example, the input data which would normally be provided by the system's microprocessor, random logic, FPGA etc was provided by a Hewlett Packard HP8180A data generator.

The antiparallel diodes are used to recirculate the current that is induced in the winding when the current through the previously activated winding on the pole is terminated. Hence, during each motor revolution both positive and negative current flows through the power switches which control the winding. Fig 5.3.3 illustrates the voltage and current flows for Drain 0.



TPIC 6595 - Reverse Conduction without Damage

Current and voltage waveforms at instant of turn-on of winding.

Reverse current flows through windings at turn-on.

DMOS power transistor conducts in reverse mode, reducing power dissipation.

High peak reverse currents are possible.

Figure 5.3.3 - TPIC6595 Stepper motor turn-on waveforms

Two features of the Power+ Logic DMOS output structure enhance the performance of the outputs when switching inductive loads as in the previous stepper motor example. Figure 5.3.3 shows an expansion of the wave forms of the negative current region of the winding pulse from the stepper motor application.

As previously mentioned, the anti-parallel diodes of the DMOS output allow the recirculation of current at winding turn-on. It is the anti-parallel diode which allows the DMOS output to withstand high peak reverse currents. In contrast, a power bipolar structure does not benefit from an inherent anti-parallel diode; one must be physically added, either to the integrated circuit design, or externally at the board level.

If negative currents are required of a bipolar power switch which does not include such as diode, parasitic isolation diodes in the bipolar structure will conduct which may cause system malfunction. It is for this reason that a DMOS solution is often the most practical and economical for motor drive applications.

Returning to the stepper motor example, as the winding turns on, the voltage drop across the output decreases. Once the voltage drop across the output ceases to be at least 0.7V , the body drain diode no longer conducts. At this point, the DMOS power transistor turns on in the reverse direction, allowing continued negative current flow to the inductor.

Once reverse conduction through the DMOS becomes the vehicle for negative current flow to the inductor, the power dissipation is given by the product of $r_{DS(on)}$ and the square of the drain current. Reverse conduction continues through the DMOS transistor until the current reaches zero.

Why choose a Power+ Logic device for an application:

The DMOS output structure is power efficient, reducing system dissipation and heat- sinking.

TPIC6Axxx parts have current limited output protection

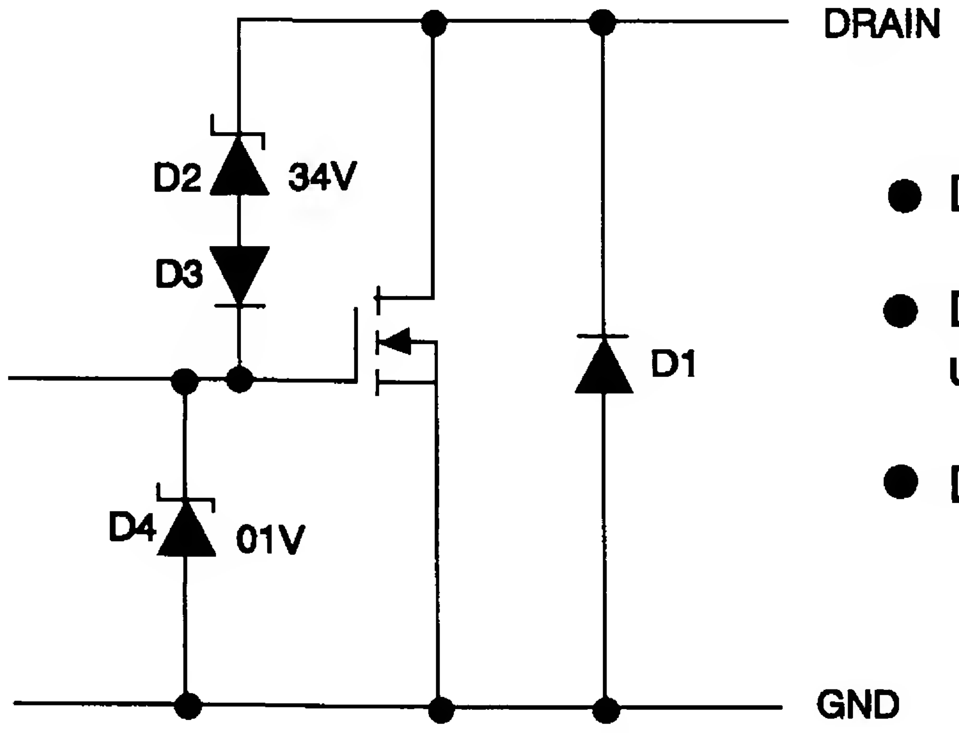
The output structure is fully specified to withstand high avalanche energy.

System design is simpler than with discrete DMOS or bipolar transistors.

The PCB layout is substantially more compact due to the integration of power and logic, and the lack of external protection passives in most systems.

Power+ Logic Output Structure

Typical Schematic - All Drain Outputs



- **D1 is an integrated body drain diode**
- **D2 and D3 are added to provide improved unclamped energy capability**
- **D4 is added to prevent gate oxide damage**

Figure 5.3.4 - Power+ Logic Output Structure

The TPIC6595 device has 8 power DMOS outputs with built-in 45V voltage clamps for enhanced inductive energy switching capability. When switching inductive loads, high voltage transients are seen at the device output when the output is placed in a high impedance state. The voltage generated by the inductive transient is limited by the breakdown mechanism of the output structure.

For the TPIC6xxx Power+ Logic devices, the internal dynamic 45V clamp circuit will eventually conduct during switching of an unclamped inductive load, allowing current to charge up the gate of the DMOS.

Once the DMOS gate voltage exceeds the threshold voltage of the device, the DMOS turns back on, completely dissipating the energy from the inductor. Thus, the entire active area of the DMOS transistor is used in the forward bias mode to absorb energy from the inductive load.

Without the internal clamp circuitry, the device output would be driven into avalanche breakdown, and would operate in the much lower energy capability reverse bias mode. The built-in voltage clamps of the Power+ Logic devices allow the user to switch up to 75 mJ of avalanche energy without the use of external snubber circuitry.

Each DMOS output of the TPIC6595 can provide 250 mA of continuous current with all outputs turned on. Individually, the outputs can be pulsed to provide up to 1.5 A of current. Or, multiple outputs can be parallelled for increased current drive of up to 6A of pulsed total load current. This rating is sufficient to drive the stepper motor when operating at the described duty cycle.

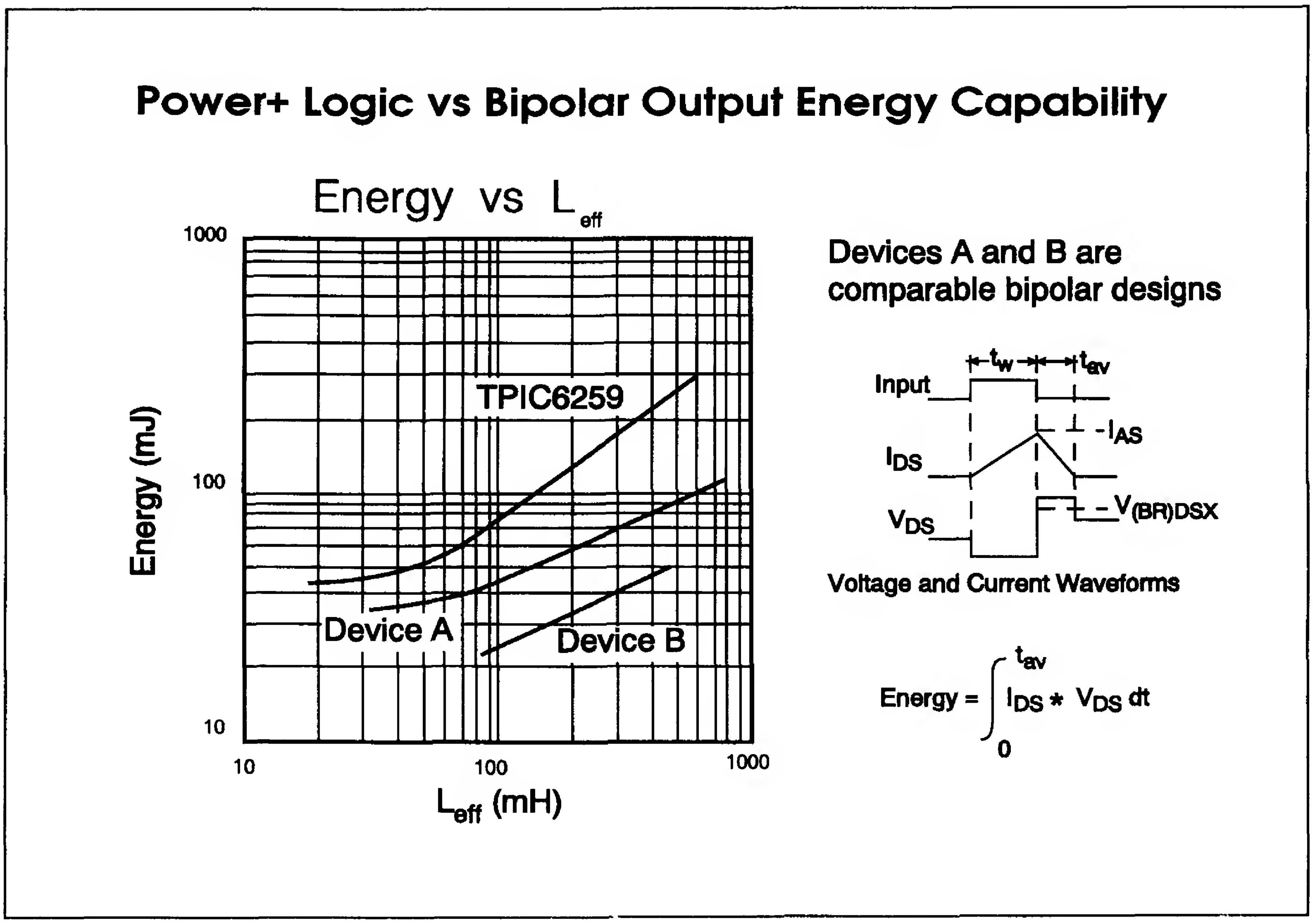


Figure 5.3.5 - Power Logic Vs Bipolar Output Energy

In describing the ruggedness of any power output, a key parameter is the avalanche energy capability. When the maximum energy capability is determined by thermal limitations of the silicon, the energy that can be dissipated during avalanche is not a constant, but varies with peak switching current and load inductance. Some power structures, however, may be prematurely limited by secondary breakdown and will have a constant energy rating. For an inductive switching pulse within the energy capability of the device, the energy dissipated in the output is proportional to the product of the current and voltage wave forms.

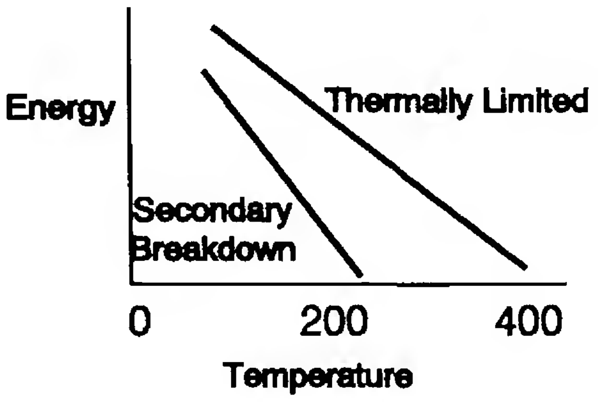
Figure 5.3.5 benchmarks the ruggedness of the Power+ Logic devices against two low side bipolar devices having comparable voltage capability. Device A has a breakdown voltage of 37V, while device B has a breakdown voltage of 50V. Each bipolar device has approximately twice the output active area as the Power+ Logic devices. The data in the figure reflects the last point of output survival just prior to its destruction.

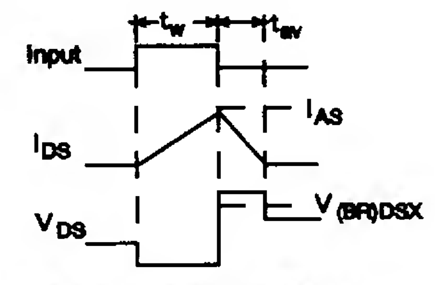
It is evident that the Power+ Logic DMOS device is much more rugged that either of the bipolar structures. While switching a 350 mH inductor, the TPIC6259 dissipates 200 mJ prior to destruction, more than twice the energy of the bipolar devices. Note that while the energy capability of the Power+ Logic devices decrease to 45 mJ while switching a 30 mH load, this is still significantly more than comparable bipolar devices. This implies substantially improved safety margins when using Power+ Logic solutions.

Unclamped Inductive Switching Test Data

Maximum Energy Capability Prior to Device Destruction
T_j = Starting Junction Temperature = 25 °C

Device Type	I_{AS} (A)	t_{av} (ms)	V (V)	V (V)	L_{eff} (mH)	L (mH)	E (mj)	P_O (W)	K	T_m Deg C	T_{jpk} Deg C
DMOS TPIC6259	2.1	0.8	50	15.1	19	13.2	42.2	105.5	269.0	378	403
	1.7	1.4	50	15.1	42	29.4	58.1	83	269.0	394	419
Bipolar Device A	1.3	1.5	37	9.0	41	30.7	35.4	48.8	139.5	122	147
	0.9	2.6	37	12.8	101	66.3	43.9	34.4	139.5	114	139
	0.8	5.0	37	19.0	247	120.0	69.4	27.8	139.5	129	154
Bipolar Device B	0.8	1.3	50	11.6	80	61.4	25.6	40.0	139.5	94	119
	0.7	1.8	50	9.5	125	101.0	30.6	35.0	139.5	96	121
	0.5	3.4	50	15.0	335	335.0	41.9	25.0	139.5	95	120





Voltage and Current Waveforms

$$\text{Energy} = \int_0^{t_{av}} I_{DS} * V_{DS}\,dt$$

Figure 5.3.6 - Unclamped Inductive Switching Test Data

In addition to peak switching current and load inductance, the energy capability of a power device varies with temperature. As the junction temperature of the device increases, energy capability decreases. This temperature-energy relationship was exploited to further understand the avalanche energy capabilities of the Power+ Logic devices.

Unclamped inductive switching tests were performed on the Power+ Logic devices in which the junction temperature of the DMOS output was gradually raised by forcing the device to dissipate increasingly large amounts of energy. The virtual junction temperature of the device immediately prior to destruction was calculated.

Note that for the purposes of these tests, the 150 °C maximum junction temperature specification of the Power+ Logic devices was violated; these tests do **not** reflect recommended operation of the Power+ Logic devices.

Assuming mechanical limitations of the package are disregarded, the maximum avalanche energy capability of a power device operating in the forward bias mode is limited by the thermal capabilities of silicon. However, the actual avalanche energy dissipated by a given power structure may be prematurely limited by a secondary breakdown mechanism.

In the case of the Power+ Logic outputs, the absence of forward secondary breakdown can be shown. The calculated virtual junction temperature of the Power+ Logic output structure at the point of device destruction was greater than 400 °C. Since silicon is thermally limited at approximately 400 °C, silicon thermal limitations were the probable cause of device destruction.

For comparison, similar tests were performed on the bipolar devices A and B. Bipolar device B (50V clamp) had a calculated maximum virtual temperature of approximately 120 °C immediately prior to destruction, clearly illustrating a secondary breakdown limitation. Bipolar device A (37V clamp) had improved characteristics, but still clearly experienced secondary breakdown limitations with destruction temperatures ranging from approximately 140 °C to 150 °C.

The following terms and definitions apply to figure 5.3.6:

I_{as} = Peak current reached during device avalanche

t_{av} = Time duration of device in avalanche

L = Load inductance

L_{eff} = Effective load inductance; accounts for supply voltage

E = Energy absorbed by device under test $L_{eff} \times I_{as}^2/2$

V_{dd} = Output supply voltage

V_{dsx} = Effective device avalanche voltage

T_c = Case temperature

T_M = Maximum junction rise which occurs in inductive switching

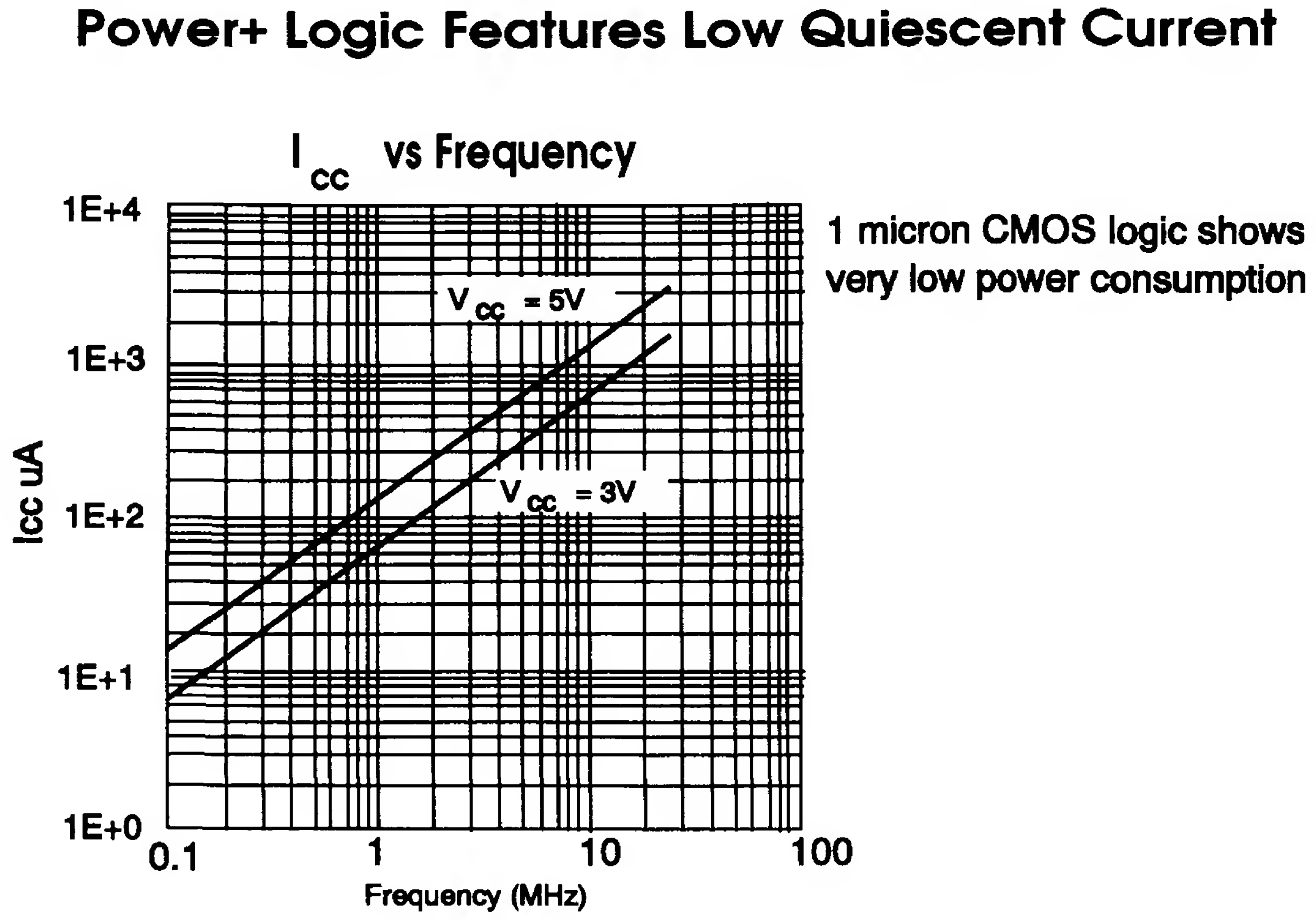
P_o = Power = $I_{as} \times V_{dsx}$

K = 139.5 = A thermal constant where the area of active silicon = 1k mils square.

K = $2/(A(p\ kc)^{1/2})$ where A = Area of power gen. silicon
p = density of silicon
k = thermal conductivity of silicon
c = thermal capacity of silicon

T_M = $(2^{0.5})/3\ Po\ k(tav)^{0.5}$

T_{JPK} = Peak junction temperature at point of destruction = $T_M + T_c$



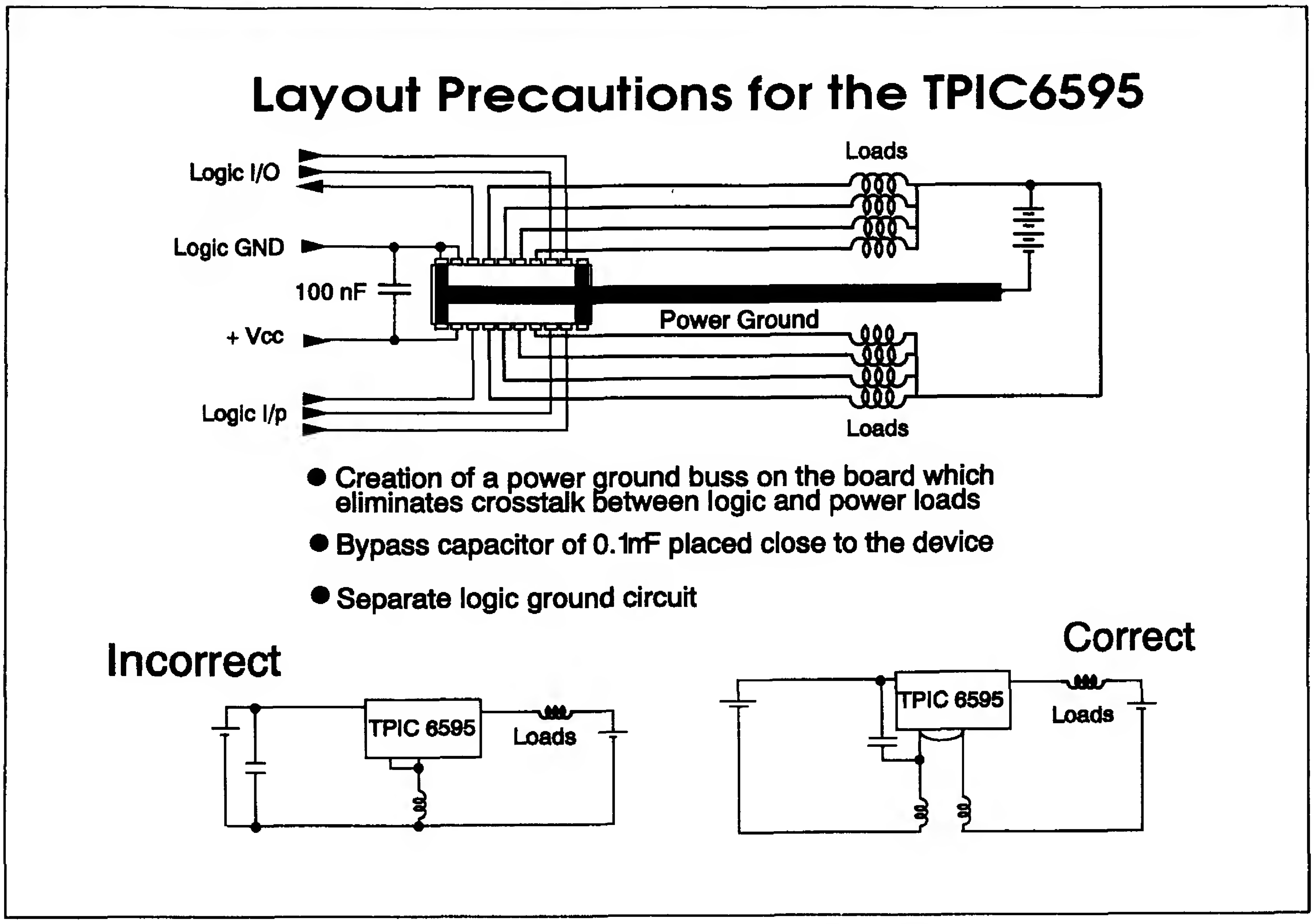
Power+ Logic Features Low Quiescent Current

1 micron CMOS logic shows very low power consumption

Figure 5.3.7 - Power+ Logic Features Low Quiescent Current

The Power+ Logic devices integrate performance power output structures with high-density sub micron CMOS logic. Figure 5.3.7 shows Icc versus SRCK frequency for the TPIC6595 with the outputs static and an alternating bit pattern on the SER IN pin. This example demonstrates the high logic frequency capability of the Power+ Logic devices, as well as the low Vcc power consumption. A high logic speed capability allows the information to be transferred from the µP, FPGA or ASIC interface very quickly even though the switch and load operation occurs at a much slower repetition rate. This would especially be important when cascading several devices for a large number of outputs all controlled be a single serial interface, as in LED (or incandescent lamp) video arrays.

The power described in this graph is the term P_{quies} used in calculating the total average power dissipated in a device.



Layout Precautions for the TPIC6595

- Creation of a power ground buss on the board which eliminates crosstalk between logic and power loads
- Bypass capacitor of 0.1nF placed close to the device
- Separate logic ground circuit

Incorrect

Correct

Figure 5.3.8 - Layout Precautions for the TPIC6595

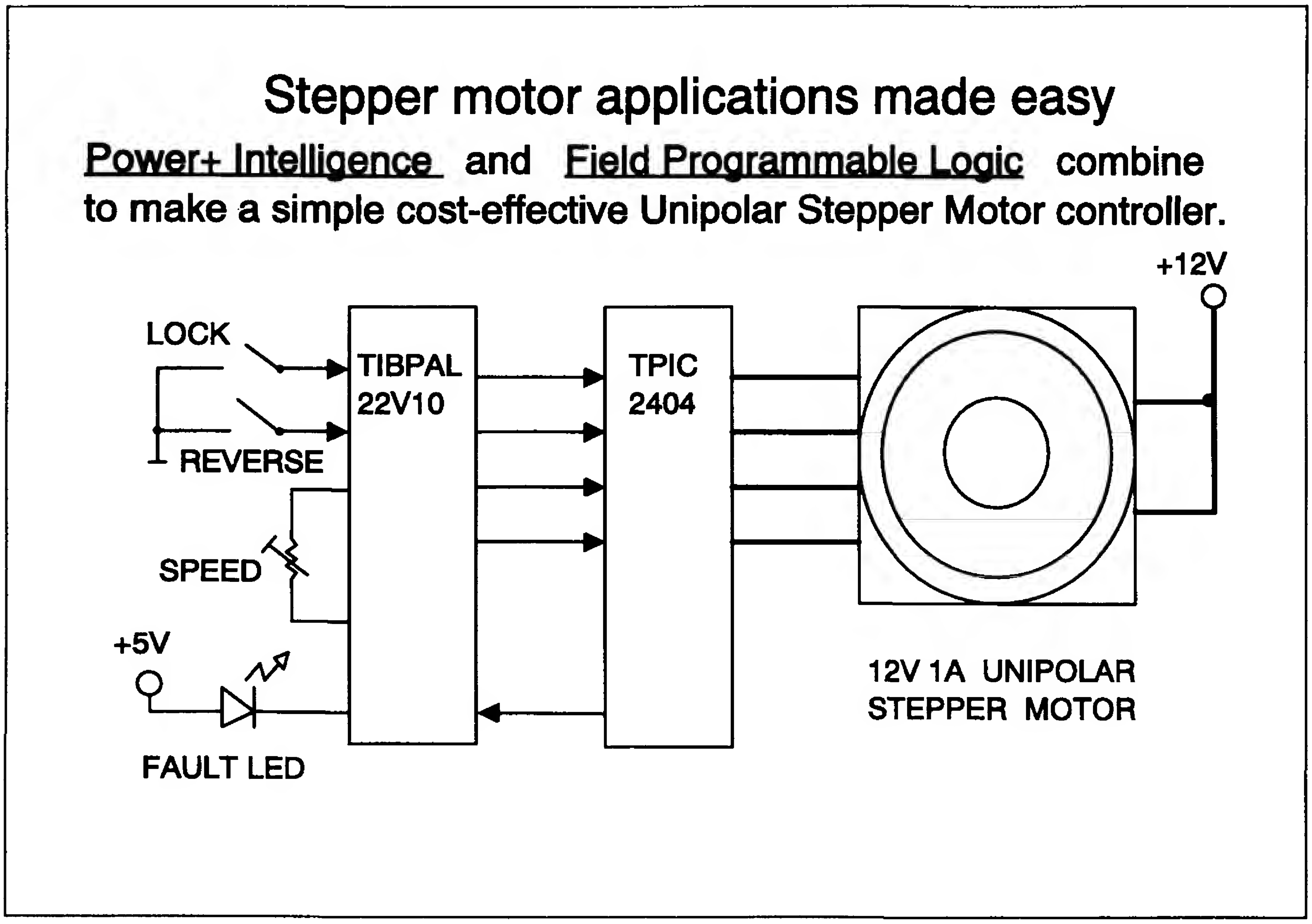
When using the TPIC6595, or any of the Power+ Logic devices, there are several PCB layout considerations which should be kept in mind. High frequency layout rules should be used when designing any power switching systems as mutual inductance (i.e. coupling between the drive circuit and load circuit) can cause erroneous signals that result in false operation. In figure 5.3.8, the "Incorrect" sketch shows an undecoupled mutual inductance in the power and logic ground. This is not a separate inductor - it represents the inductance of the common ground trace, to illustrate the nature of the problem. The following precautions are offered:

- Use of a heavy duty power ground buss on the PCB to eliminate crosstalk between the power loads and input logic.
- Addition of a 0.1 µF bypass capacitor between V_{CC} and the logic ground line, placed close to the device to dampen any stray signals experienced by the drive circuit.
- Separate power and logic ground circuits.

Figure 5.3.8 shows an example implementation of these board layout considerations using the TPIC6595.

3.2 Stepper Motor Applications made easy with TPIC2404

TPIC2404 is a monolithic quad intelligent-power 45 V 1 Amp low-side switch in a small 15-pin zig-zag in-line power package. Its switching efficiency means most applications avoid a heat sink, saving power and board space. Comprehensive error circuitry detects overvoltage, open load (or short to ground), short to Vcc and thermal sensing. This shuts down the power devices and produces a FAULT output.



Stepper motor applications made easy

Power+ Intelligence and Field Programmable Logic combine to make a simple cost-effective Unipolar Stepper Motor controller.

Figure 5.3.9 - Power+ Intelligence with Field Programmable Logic

The TPIC2404 is a candidate for driving relays, solenoids, lamps and motors - and in particular, unipolar stepper motors, which require four low-side drivers. It has clamp diodes that are specified to deal with the spikes generated by switching inductive loads.

The application brief **"Stepper motor applications with TPIC2404"** introduces the TPIC2404 in a simple stepper motor system. Programmable logic is used to generate the waveforms, respond to error conditions and provide a clock oscillator and LED buffer. Protection, decoupling and PCB layout is described. PAL files and a PCB master are included, with component overlays for minimum and maximum configurations. The upgrade path to PLD and FPGA control is discussed.

Motor speed is adjustable, with push switches for hold and reverse. Shorting outputs to the supply or ground, or disconnecting them will stop the motor driver and light the LED. It is possible to generate new logic functions within the PAL that will serve both stepper motors and other types of power control system on the same PCB.

The TPIC2404KN integrates Linear, Logic, and Bipolar power devices on one die. It will tolerate power supply transients and battery reversals of up to 13 V, and it's outputs are specified to 45 V for switching inductive loads; the output clamp diodes are rated at 2.5 A. It is recommended for 9 to 16 V power supplies, but will tolerate -13 V to +24 V as an absolute maximum. For critical applications that push the dissipation limit, the package has a grounded heat sink tab. The TPIC2404 is specified for operation in the -40 deg C to +125 deg C temperature range.

Simple equations define the stepper motor driver

Field programmable logic solution is portable to FPGA and ASIC

```
EQUATIONS

o1 := updown * LEDI * /Q1 * /Q0
    + /updown * LEDI * Q1 * /Q0
    + /updown * LEDI * /Q1 * Q0
    + updown * LEDI * Q1 * Q0

o2 := /updown * LEDI * /Q1 * /Q0
    + updown * LEDI * Q1 * /Q0
    + updown * LEDI * /Q1 * Q0
    + /updown * LEDI * Q1 * Q0

o3 := LEDI * Q1

o4 := LEDI * /Q1
```

```
LEDO := LEDI

Q2 := GND

Q1 := Q1 * /Q0
    + /Q1 * Q0

Q0 := en * /Q0

CKO = CKI

CKF = /CKO
```

Figure 5.3.10 - PAL equations illustrate the simplicity of the code

A more detailed description of this code is given in the application brief SLDTE01; this is shown here to illustrate how few lines of code are needed to implement a stepper motor driver with on-board oscillator, Fault response (the driver is turned off), re-start and re-try, and an LED driver. The same code will compile to run in larger PLDs, FPGAs, and ASICs, and can be extended to include the stepping complexity required. This can substantially reduce system costs compared with a proprietary stepper motor controller.

4 Applications - DC Motor drivers

4.1 Bi-directional Motor Drive Application

DC motors play an important role in a wide variety of electronic systems. Efficient control of motor speed and torque is an important issue for many system designers. Motor controllers are proliferating with the increase of automation in the home, industry, office and car.

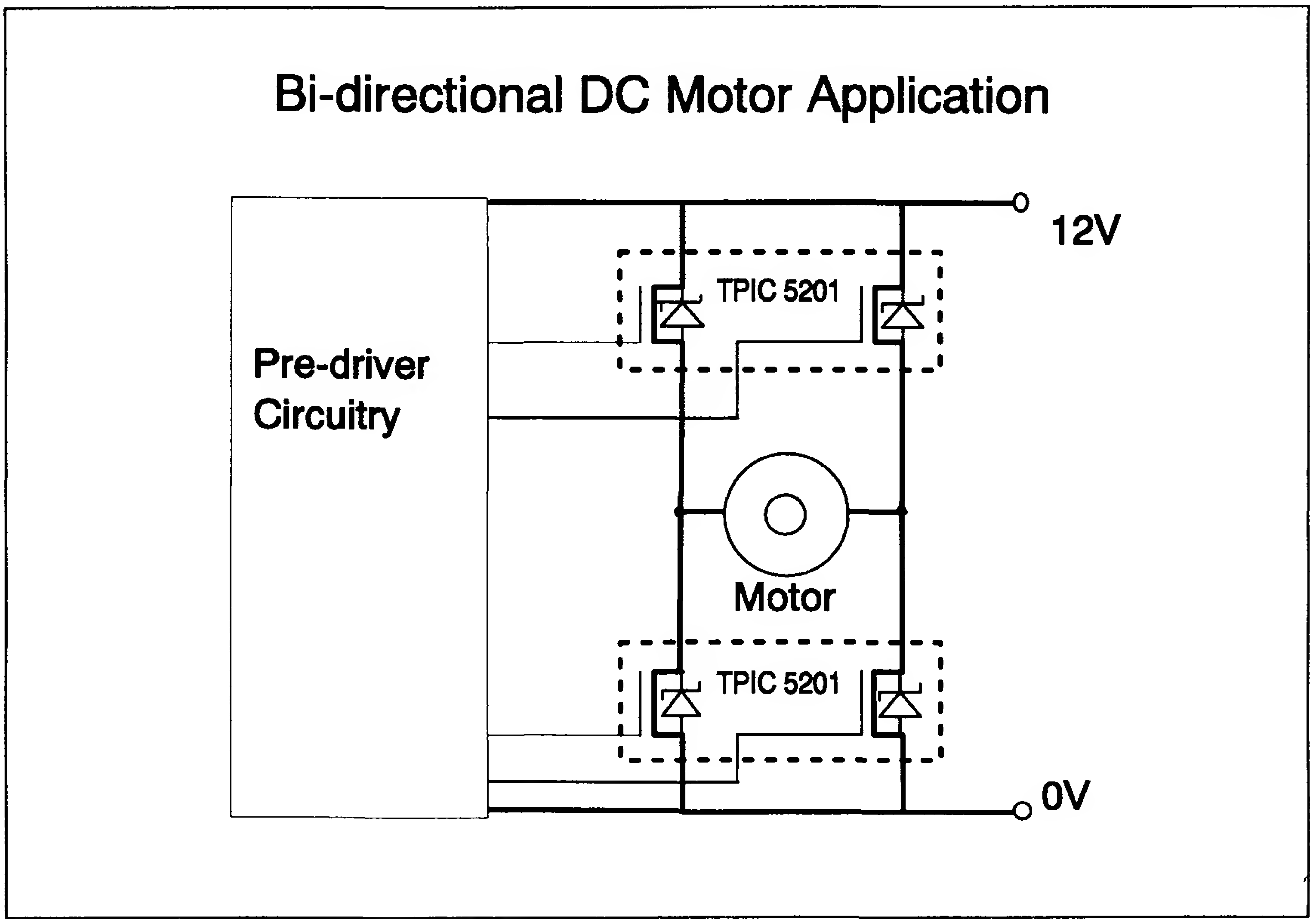
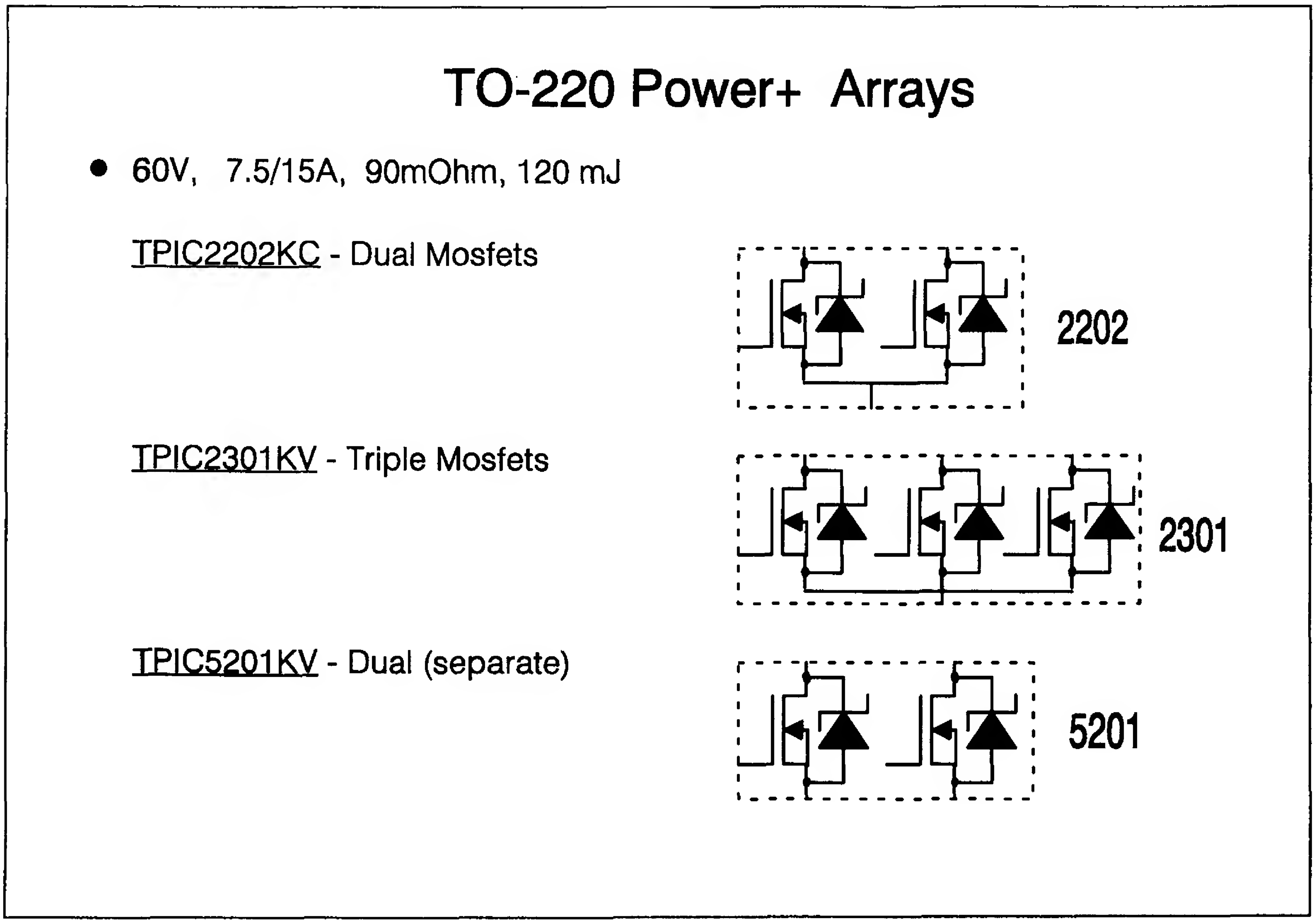

Bi-directional DC Motor Application
Pre-driver Circuitry
TPIC 5201
12V
Motor
TPIC 5201
0V

Figure 5.4.1 - Bi-directional DC Motor Drive

Figure 5.4.1 shows a bi-directional DC motor being driven from a 12 V supply by two dual DMOS switch devices arranged in a full H-bridge configuration. This circuit uses either logic levels to set the direction of rotation of the motor, or PWM signals that can control both direction and speed. In most systems, these signals would be supplied by a micro controller or field programmable logic device.

In the PWM case, a 50% duty cycle on both input signals produces a net zero voltage across the motor, creating a stall condition. Control of the motor's speed and direction of rotation is achieved by varying the duty cycle of one of the input signals while keeping the other fixed at 50% duty cycle. This variation between the input signals results in a net DC voltage across the motor, providing the drive current needed to meet the torque requirements of the motor.



TO-220 Power+ Arrays

- 60V, 7.5/15A, 90mOhm, 120 mJ

TPIC2202KC - Dual Mosfets

TPIC2301KV - Triple Mosfets

TPIC5201KV - Dual (separate)

Figure 5.4.2 - Power+ Arrays

4.2 System power considerations

The motor drive current has a peak value of slightly less than 6 A with a minimum value of 4 A. Energy calculations must be based on the condition when one of the input signals is at the minimum duty cycle.

4.2.1 Choosing an Output Switch

The device required for this application must be capable of conducting at least 5 A continuous (6A pk) and must be configurable as an H-Bridge.

TPIC 5201 KV

- 60V, 7.5/15A, 90mOhm, 120 mJ
  Dual (separate) MOSFETs in a
  TO-220 7-lead package

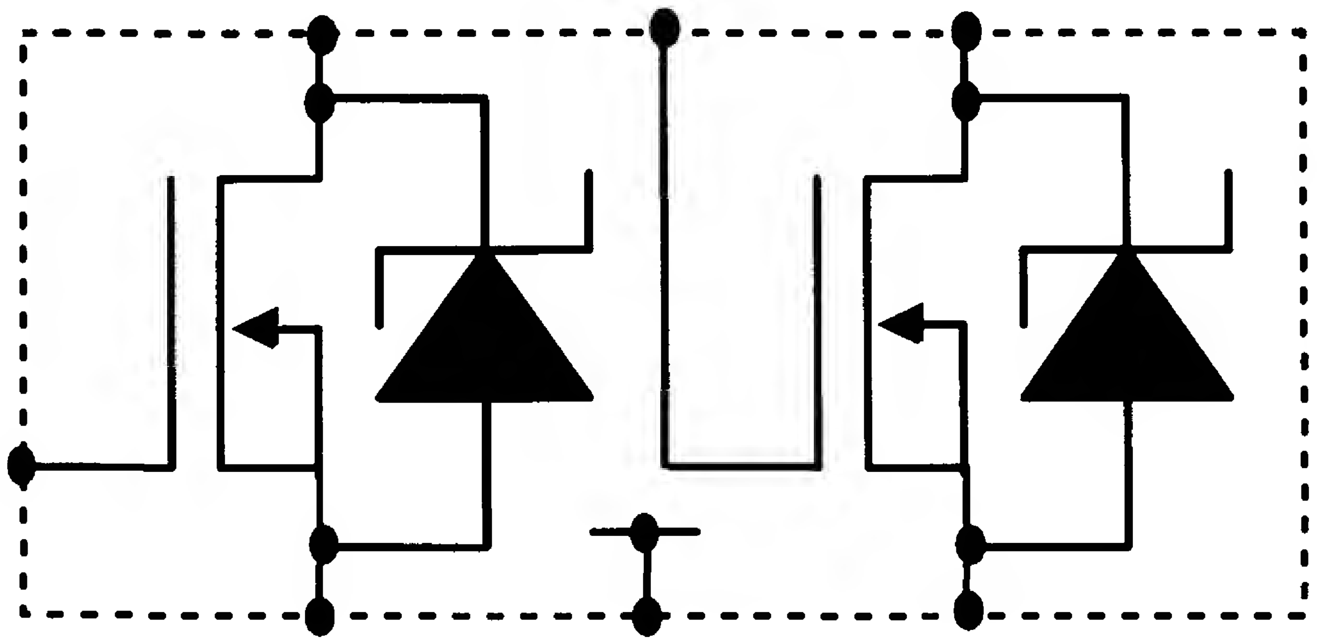


Figure 5.4.3 - TPIC5201 Power+ Array

The device chosen for this application is a TPIC5201 Power+ Array. This device contains two uncommitted high performance DMOS transistors in a single power package. The uncommitted transistors allow for an H-Bridge configuration. The low $r_{DS(on)}$ minimizes the device dissipation.

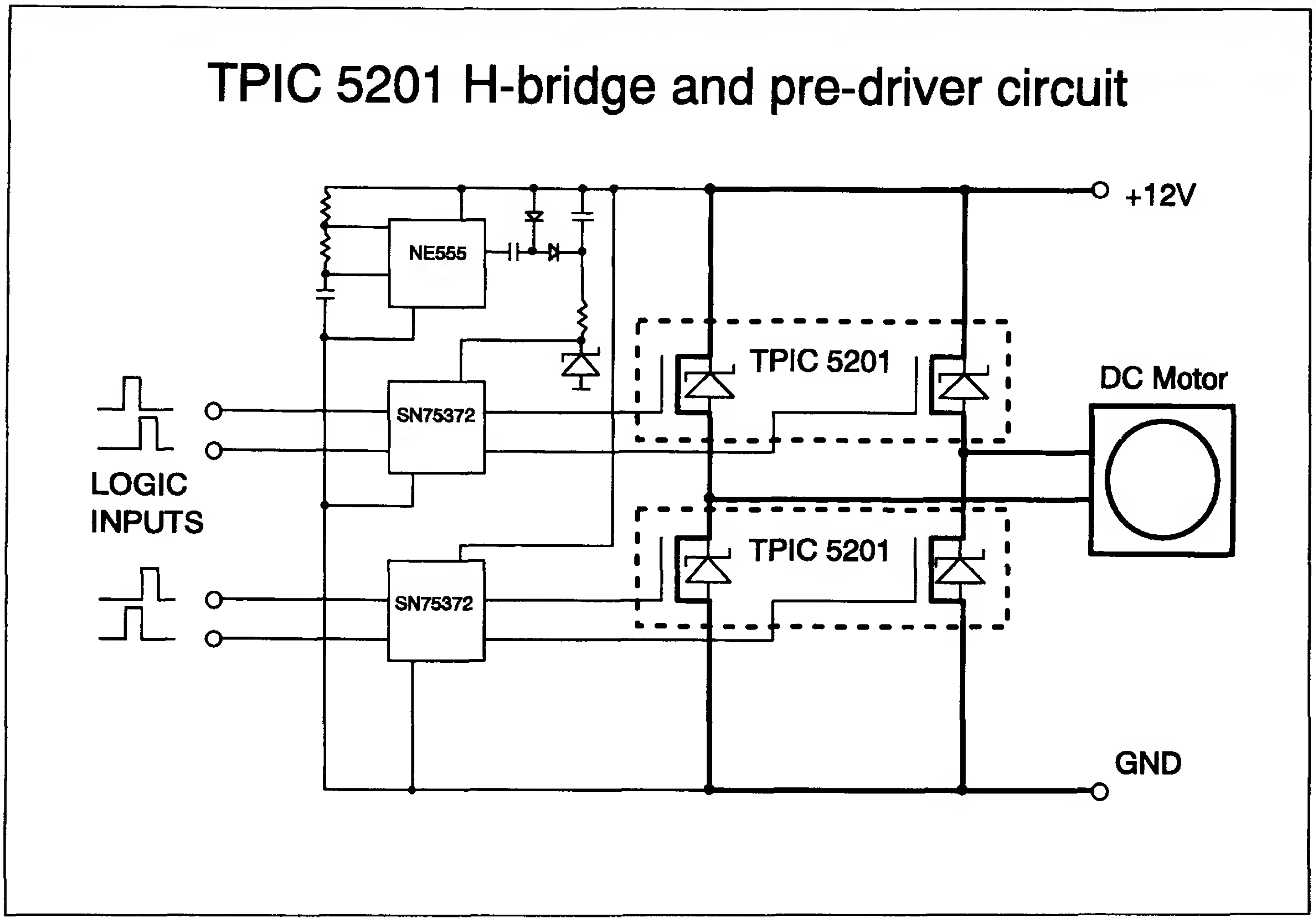

TPIC 5201 H-bridge and pre-driver circuit
+12V
NE555
SN75372
SN75372
TPIC 5201
TPIC 5201
DC Motor
LOGIC INPUTS
GND

Figure 5.4.4 - A system suitable for DC or PWM control, with charge pump

The system shown uses a pair of TPIC 5201 arrays with a pair of SN75372 dual MOSFET drivers and a 555 charge pump to cater for the DC drive condition, where the gate of the upper mosfet needs to be enhanced above the positive rail in order to turn the device on.

The charge pump output voltage is clamped by a zener, to prevent overdriving the gates of the upper devices, which see close to the full charge pump voltage at the instant of turn-on. The drivers are dedicated parts designed for the task, and can source/sink 500mA peak. This allows the TPIC 5201 array devices to turn on and off very fast - as covered earlier in the switching speed section.

Using integrated drivers with integrated arrays ensures excellent matching and minimum skew. This can be used to minimise the dead time between PWM transitions to prevent cross conduction, and can therefore permit higher operating frequencies for a given system.

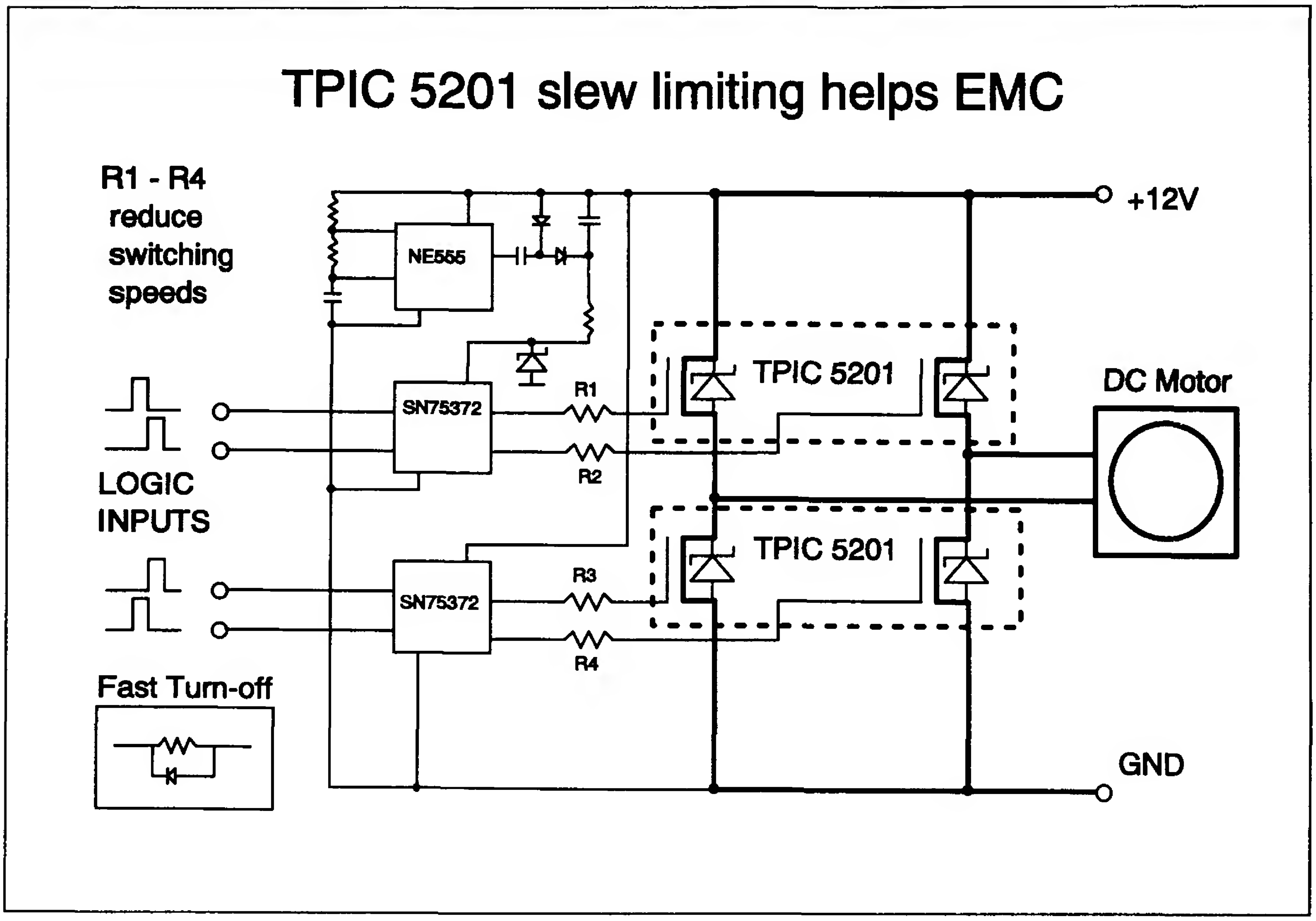

TPIC 5201 slew limiting helps EMC
R1 - R4 reduce switching speeds
LOGIC INPUTS
Fast Turn-off
NE555
SN75372
SN75372
R1
R2
R3
R4
TPIC 5201
TPIC 5201
+12V
DC Motor
GND

Figure 5.4.5 - Slew Limiting the TPIC5201 array

Slew limiting can be a vital part of ensuring Electro-Magnetic Compatibility (EMC). By reducing the rise (and fall) times of the output device to a value that is just fast enough to serve the purpose required, RF energies can be greatly reduced, and their spectrum constrained.

For asymmetrical slew control, two resistors and a steering diode may be used on each gate. Thus the rise and fall times may be controlled independently. This may prove beneficial when designing a PWM system, since a delay is needed between enable pulses that allows for one device to turn off before the other turns on. This prevents the two series devices connecting power to ground, causing a "shoot-through" current to flow. Although this can be beneficial in some cases, it is vital that it be controlled tightly.

A diode/resistor combination could delay turn-on, with a rapid turn-off. If enough margin is allowed for, it is possible to use an input signal waveform without any delay between turn-on and turn-off, thus simplifying system design.

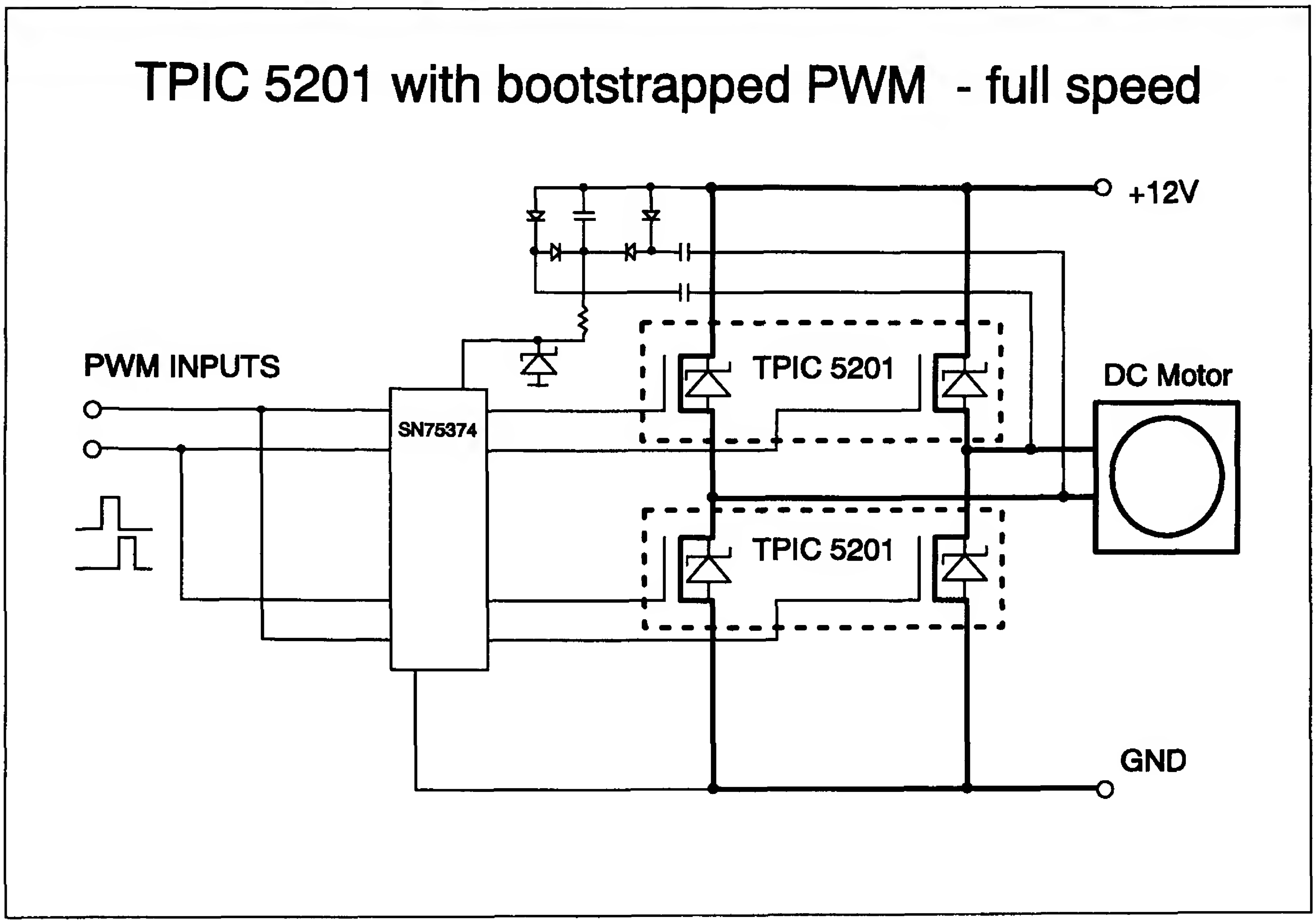


Figure 5.4.6 - Dedicated PWM solution needs no external charge pump

Here the arrays are driven by a PWM source as described above. The charge pump can now be bootstrapped from the PWM output of the arrays, reducing the parts count. An SN75374 quad mosfet driver has been used to further reduce components. Slew limiting is optional, but this system is shown without it.

The PWM waveforms need to take account of the delays inherent in switching the devices off and on. The possibility of turning on an upper and lower device simultaneously exists if care is not taken. Although there are circumstances where this "Shoot-through" current is beneficial, it is vital that its duration be guaranteed to be very short. In either event, a good understanding of the turn-on and turn-off times of the TPIC 5201 output devices is essential. A method of estimating these was detailed earlier in this seminar.

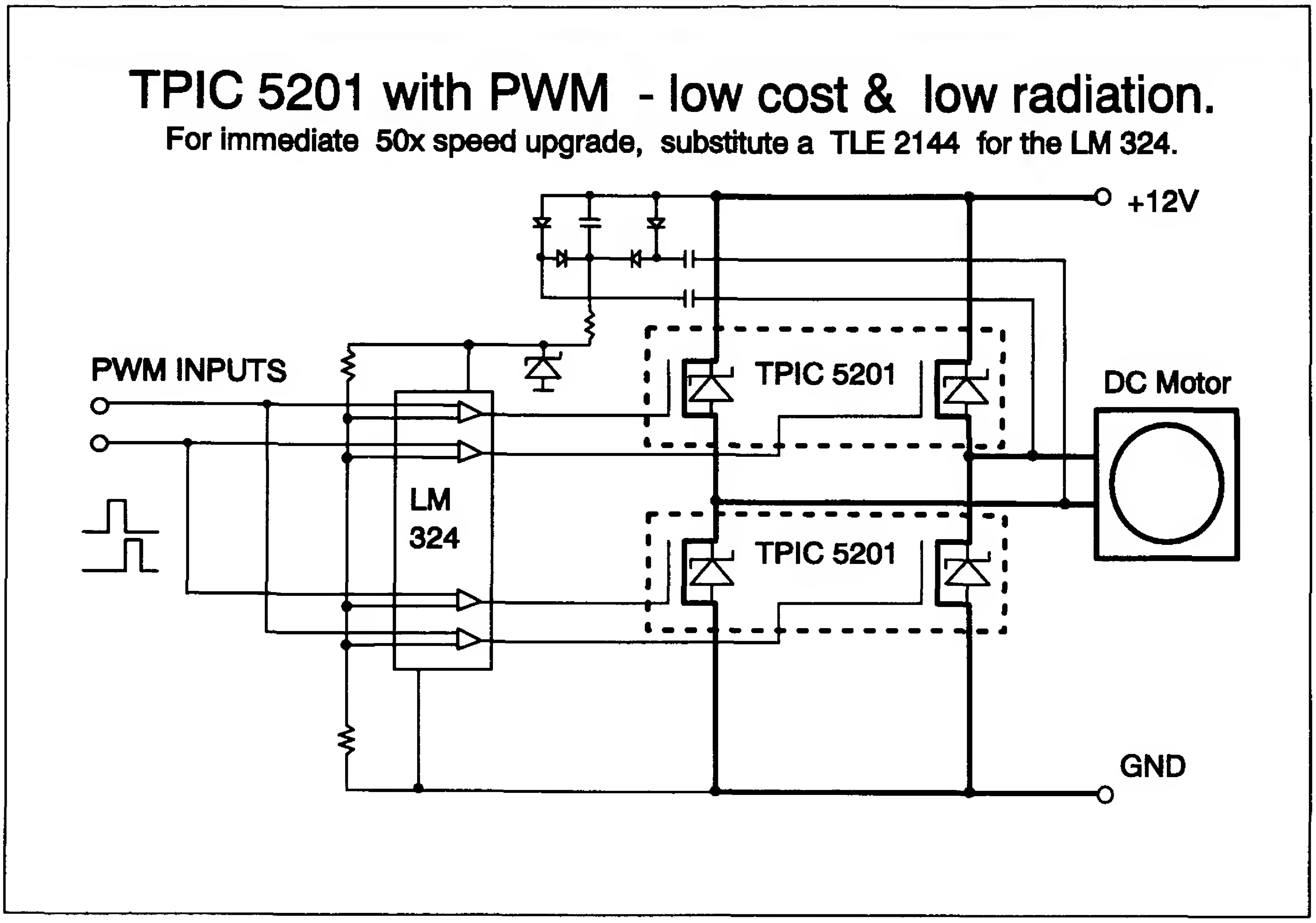

TPIC 5201 with PWM - low cost & low radiation.
For immediate 50x speed upgrade, substitute a TLE 2144 for the LM 324.
+12V
PWM INPUTS
LM
324
TPIC 5201
TPIC 5201
DC Motor
GND

Figure 5.4.7 - Low RF emissions with Op-Amp driver

This simple design makes use of the slow edges from an LM324 quad op-amp to ensure that RF emissions are controlled. If accuracy is critical, limiting resistors could be used to pad the gates so that variations in the (unspecified) slew rate of the LM 324 do not cause significant output slew variations. This solution is best applied to systems where the PWM frequency is below 400 Hz, and is consequently audible to the human ear.

For a better compromise, the TLE2144 is a good choice, with a higher slew rate that allows the PWM frequency to go supersonic, reducing audible noise. The two devices are pin-compatible, so the possibility exists to design a system that is configurable for differing applications.

4.2.2 Advantages Over Discrete Transistors

Since the two power MOSFETs of each TPIC5201 are fabricated monolithically, the FETs within each device are inherently well-matched. As a result, there is little variation in the switching times and transconductance of the transistors. This device-matching aids in system design by significantly reducing the need for feedback circuitry to compensate for potential switching time mismatches. As a result, the necessary pre-drive circuitry can be greatly simplified.

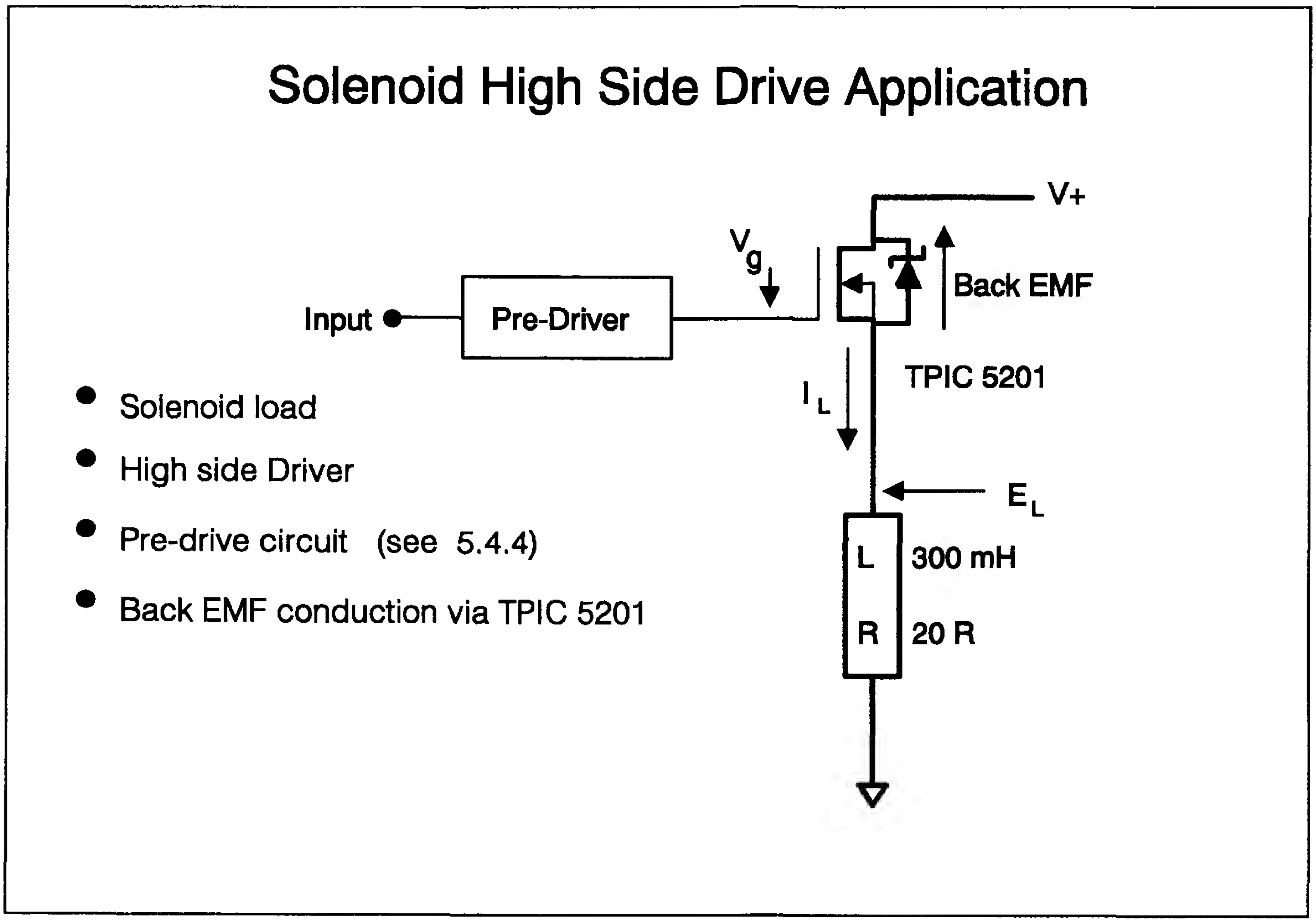
Each power transistor in the TPIC5201 feature a low on-resistance of 90 mΩ. By minimizing on-resistance, the power consumption of the H-bridge is reduced, increasing the power available to the motor. Motor control systems built with low on-resistance power switches allow more efficient motor performance, and reduce heat build-up in the controller.

The energy capabilities of the TPIC5201 have been characterized over its entire range of operation. The specifications for the TPIC5201 include peak avalanche current versus avalanche time rating curves. Unlike the single point energy specifications typical of discrete MOSFETs, designers using the TPIC5201 can accurately monitor compliance with active safe operating area design constraints.

5 Applications - Solenoid driver

5.1 Solenoid Application

Solenoids are used to provide linear motion. Solenoid applications include electric locks on automobiles, mechanism actuators in tape recorders, and air control valves.



Solenoid High Side Drive Application

- Solenoid load
- High side Driver
- Pre-drive circuit (see 5.4.4)
- Back EMF conduction via TPIC 5201

Figure 5.5.1 - Solenoid Application

Figure 5.5.1 shows a solenoid with a high side driver. The high side drive places the control switch between V_{CC} and the load. Selection of a switch device for this application must include an energy evaluation and a device which can operate as a high side switch. The solenoid load is inductive like the stepper motors, however instead of having cross coupled signals the solenoid has a dynamically changing impedance.

When the current reaches a level sufficient to cause the solenoid to operate, the armature begins to move, and the coil inductance changes. The amount of change is a function of the solenoid design. Conventional relays also exhibit this change in inductance since they are solenoids which operate switches.

Energy and power considerations are similar to the stepper motor. The interface circuit must drive an inductive load with a peak current. The solenoid winding inductance and resistance must be considered to evaluate the avalanche energy. Just as with any inductive load the total avalanche energy must be considered as well as the peak avalanche current.

5.1.1 Choosing an Interface Device

The voltage and current waveforms for the solenoid were shown in Figure 5.2.3. This particular solenoid was shown because of the drastic inductance change during operation. The inductance change causes the discontinuity seen in the inductor current during t_{on}.

Vg, the output from the predrive circuit, is at -5 V during toff. The circuit as shown relies on the DMOS transistor to provide the conduction path for the back e.m.f. current from the inductor when drive is turned off (t_{off}). This was described in the stepper motor application in Section 5.3. When the switch is turned off the solenoid voltage goes negative until it reaches approximately -7.5 V (V_g - 2.5 V) when the DMOS transistor is turned on, effectively clamping the inductor voltage. If V_g = 0 V at t_{off} then the solenoid voltage would be clamped at 2.5 V and the time required for the solenoid current to reach zero would be longer.

Using the current waveforms from device tests the energy dissipated in the switch can be calculated. A TPIC5201 Power+ Array has been chosen as the switch for this application.

Energy Calculations:

Using the calculations presented in section 5.2

$$E_T = 3(L_H * I_P^2 * V_{CL})/[6(V_{CL}-V_{SS}) + R * I_P]$$
$$= 113 \text{ mJ}$$

$$P_{off} = E_T * f$$
$$= 0.94 \text{ W}$$

$$Pon = 1/3\ I_{PK}^2 * r_{DS(on)} * d$$
$$= 7.5 \text{ mW}$$

$$P_{T(av)} = P_{off} + P_{on} + P_{quies}$$
$$= 0.94 \text{ W}$$

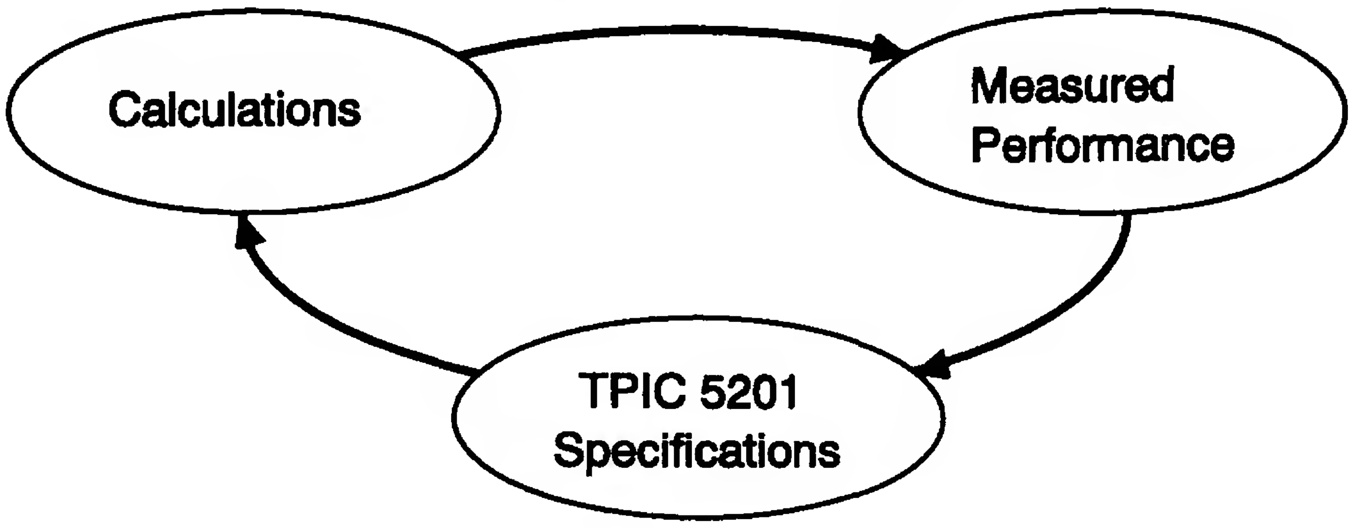
Assuming that the solenoid could be turned on for an extended period of time, the power dissipated in the switch would be :

$$P_T = I^2 * r_{DS(on)}$$

$$\begin{aligned} I &= V_{CC}/R \\ &= 0.6\ \text{A} \end{aligned}$$

$$\begin{aligned} P_T &= 0.6^2 * 0.09\ \text{W} \\ &= 32.4\ \text{mW} \end{aligned}$$

Closing the Loop


Calculations

Measured Performance

TPIC 5201 Specifications

$T_A = 25\ C$	TPIC 5201	Solenoid Application
I_{PK}	15 A	0.5 A
I_{CONT}	7.5 A	0.6 A
E_{AS}	120 mJ	113 mJ
P_{CONT}	2 W	0.94 W

- The critical value is the returned energy - E_{AS}

Figure 5.5.2 - Closing the Loop

Closing the design loop and comparing calculations, results and specifications will verify the design and indicate changes when necessary.

The results of this comparison are not what would be expected. The avalanche energy is high (113 mJ) while the Power dissipation is quite low (0.9 W). This indicates that no heat sinking is required and that a device with a lower power and current rating might be used in this application. It also illustrates the importance of doing thorough energy calculations.

In this case a quick look at current handling alone might suggest the device chosen is over-specified, but when avalanche energy is considered we can see the TPIC5201 is a good match for the application.

A similar device rated at a lower peak current value would probably not be able to handle the avalanche energy, possibly resulting in repeated "mysterious" device failures! This is not unknown, particularly when using unprotected bipolar devices without an adequate snubber network.

6 Applications - Incandescent Lamp driver

Incandescent lamps are found in many industrial applications as well as automotive, marine and aeronautical applications. Incandescent lamps can provide high output energy with rugged construction.

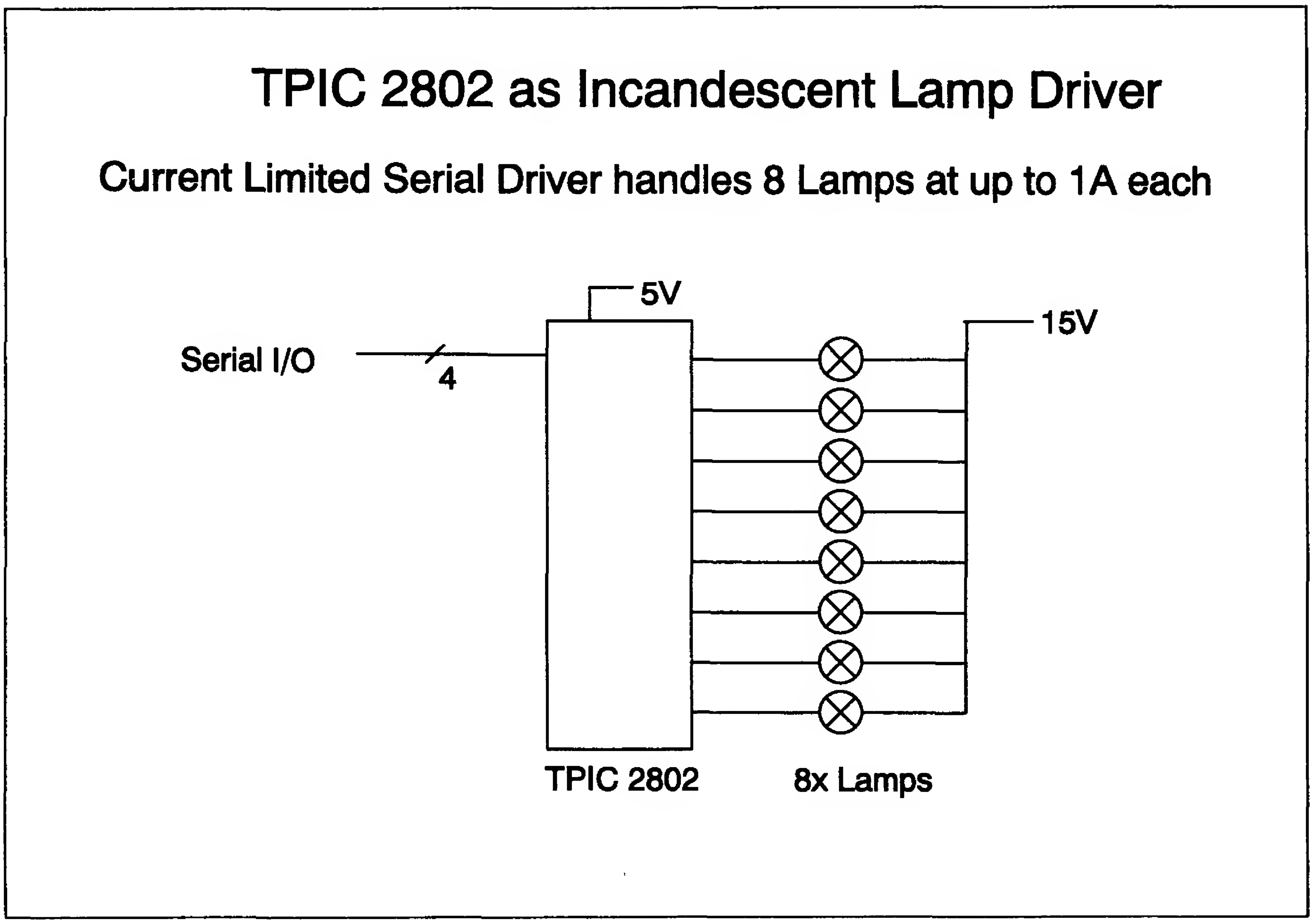

TPIC 2802 as Incandescent Lamp Driver
Current Limited Serial Driver handles 8 Lamps at up to 1A each
5V
15V
Serial I/O
4
TPIC 2802
8x Lamps

Figure 5.6.1 - Incandescent Lamp Application

The circuit in figure 5.6.1 shows an application driving eight automotive lamps from a 15V source. Incandescent lamps present a unique resistive load. The filament resistance increases dramatically as the lamp warms up to operating temperature.

Incandescent lamps are often operated with extended on time which results in a very low duty cycle time for the inrush current. If inrush current duty cycle is very low then the power dissipation could be ignored. If the high peak current is ignored premature failure of the switch transistor is likely. If the switch transistor is selected to accommodate the lamp peak current then circuit size and cost are sacrificed.

One solution is to current limit the inrush current. A conventional linear current limiting circuit would require dissipation of a large amount of heat during the warm up time. The choice of an Intelligent-Power device such as the TPIC2802 allows the output circuit to be implemented with a single integrated circuit. The TPIC2802 contains eight 1A/30 V low-side switches packaged in a 15 pin ZigZag-In-Line package (ZIP). The eight switches are controlled with a single input, SI (Serial Input), by an 8-bit serial word. Diagnostics are also provided through the output, SO (Serial Output). Independent over-voltage and over-current protection is provided to all eight switches.

6.1 Circuit Operation

The rising edge of the -SIOE pulse following the data word is when shift register data is latched into the parallel latch and the output switches are activated by the new data. However to allow the part to overcome high in-rush current, such as the lamp cold filament current an internal 100 us delay timer is started at the -SIOE pulse rising edge during which time the switch over voltage fault shutdown circuit is inhibited. During this 100 us interval the switch is protected by an internal current limiter, which is set to regulate the current to approximately 1.5 A. Once the 100 us timer period has elapsed, the output voltages are sensed by comparators and any output switch with output voltage greater than 1.5 V is latched off. It is important to note that these current-limited, 100 us, soft start bursts of power not only protect the TPIC2802, but also protect the lamp filament from an otherwise filament degrading high in-rush current.

The initial lamp in-rush current decreases from a value slightly greater that 1.5 A to a value of less than 0.5 A during a period of approximately 120 ms. The current initially presented to the lamps is a series of pulses. The first pulse is a 1.5 A/100 us pulse that is coincident with the rising edge of the first -SIOE pulse that follows the data word.

Calculation of the switch power dissipation for continuous duty:

Output Switches Y0...Y7: I = 0.5 A , duty cycle = 1.0

From figure 5.6.3

P(Y0...Y7) = 0.15W x 1.0 x 8 = 1.2 W

$P_{(QUIES)}$ = 0.25 A x 5 V = 1.25 W (per TPIC2802 data sheet)

$P_{T(AV)}$ = P(Y0...Y7) + $P_{(QUIES)}$

= 2.45 W

The maximum power dissipation for the TPIC2802 at T_A = 25 °C is 3.45W

The self-protection capability of the TPIC2802 along with the power handling capability make this a good selection for this design .

Additional features include the ability to switch high currents and inductive loads. This device is well suited to switching high energy unclamped inductive loads since each of the eight power switches is equipped with an internal 35-V collector-to-base voltage clamp. The current capability of a single switch can be extended by parallel switch operation. This application utilized one of a series of intelligent power devices.

Other Intelligent Power devices are available with different configurations and feedback features providing effective system solutions for output systems.

7 Power+ Product Futures

Power+ Futures.....

Arrays: more choice - quads and other multiples, all in SO packages
more range - on resistances to 300 mOhm and other variants
more detail - better data specs, Optional Zeners, Logic drive.

Logic: Less power, more value, targetted at HC + ULN array solutions
EE programmable PWM devices later in the year, a totally new approach to power control.

Intelligence: State-of-the-art 7.5A 125 mOhm H-bridge with full motor logic control, protection, and fault reporting. It can replace a half-eurocard of devices with a 7-lead TO-220 package.

Figure 5.7.1 - Future road map

7.1 Power+ Arrays

Future trends will include multiple devices (dual, triple, quad etc) in the 300 mOhm range, with both standard MOSFET gate drive and 5V logic level drive. Options include gate protection Zeners and a choice of DIL and SMT packages for some devices. All new devices will be available in SO package. The quad device is particularly suited to H-bridge applications, comprising a common source pair with an uncommitted pair of MOSFETs. This means that all the devices needed for an H-bridge are fabricated on one die, and enjoy exceptionally close tracking. This ensures good control over switching times, and can help control shoot-through currents with a minimum of external components.

7.2 Power+ Logic

A new family of low-cost devices is due later this year, these are targeted directly at the ULN-plus-HC logic solutions on a cost and performance basis. This contrasts with the existing TPIC6xxx series that offer a substantial performance improvement over the ULN 200x solutions when all outputs are driven simultaneously. EE-programmable power devices are also expected this year. These feature EE-programmable PWM current limit and frequency.

7.3 Power+ Intelligence

A state-of-the-art 7.5 A, 125 mOhm H-bridge with full motor control logic, in a single TO-220 package. This part compacts a sophisticated DC motor controller and four protected power MOSFETs in its compact 7-lead package. System benefits include slew-limited drivers for minimum EMC problems, automatic motor braking, logic level inputs, and a FAULT output that provides full diagnostics. All with a quiescent current of less than 20 microamps.

8 Power+ Product Summary

Power+ Intelligence

Seminar Apps Examples:

Stepper Motors Made Easy.

Incandescent Lamp Driver

....and anywhere that you need to have feedback from the O/Ps.

- TPIC 2404 - Quad LSS (Low Side Switch) with diagnostics & Fault O/P.

  45V, 1A, 1.5A limit, 0.8V Sat, 40 mJ, in a 15-pin ZIP (Zigzag inline)
  Output diode clamps are provided, with overvoltage, thermal, and over-current shutdown.
  This part is featured in "Stepper motor Applications" SLDTE01

- TPIC 2802 - Octal SIPO (Shift Register) with diagnostics and PISO.

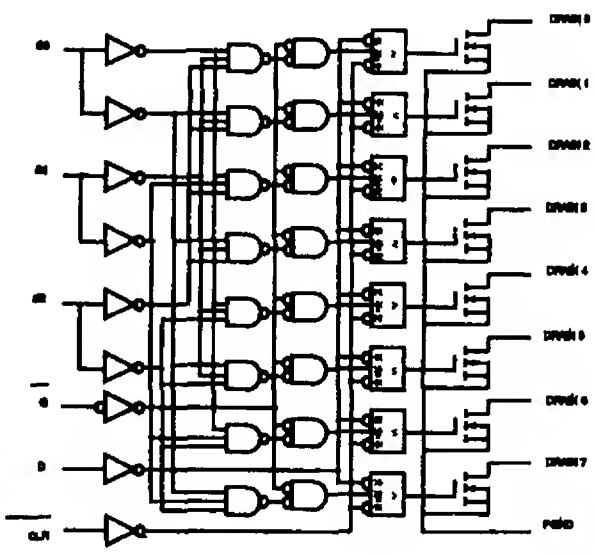
  35V, 1A, 1.8A limit, 1.4V Sat, 40 mJ, in a 15-pin ZIP
  45V transient clamps on-chip, 20 mW standby power,
  PWM and *absolute value current limit*.
  This part replaces TPIC2801, which is featured in the application report SLDA002

Figure 5.8.1 - Summary of Power+ Intelligence

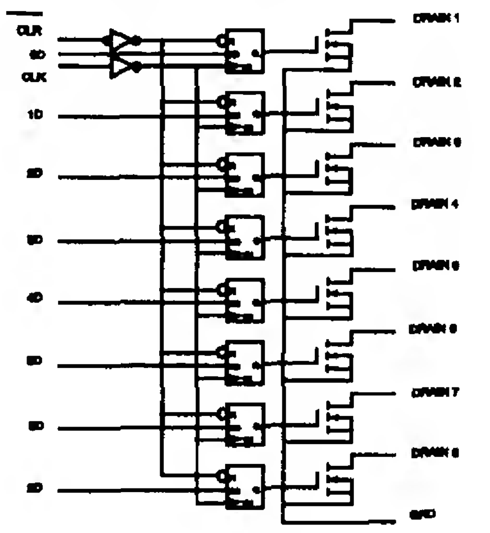
The Power+ section of this seminar has introduced power systems, discussed Resistive, Capacitive and Inductive loads singly and in combination, and provided equations that enable a first-time user to effect a good design using the device data sheet. Switching time prediction was covered, enabling the gate charge characteristic of a device to be used to estimate the switching time of a MOSFET array device. Application examples were given, including two stepper motor applications, an incandescent lamp driver and a number of DC motor applications, including PWM controlled bridge drivers.

TPIC6xxx and 6Axxx Power+ Logic Family

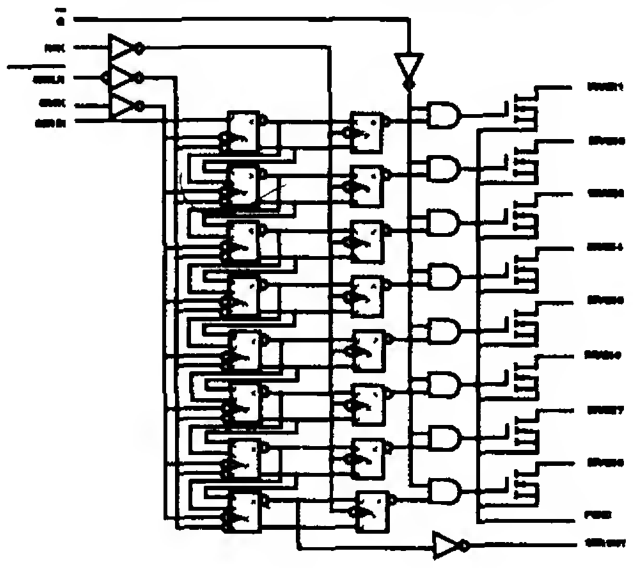
TPIC6259 & 6A259
Addressable Latch



TPIC 6273
Octal D-type



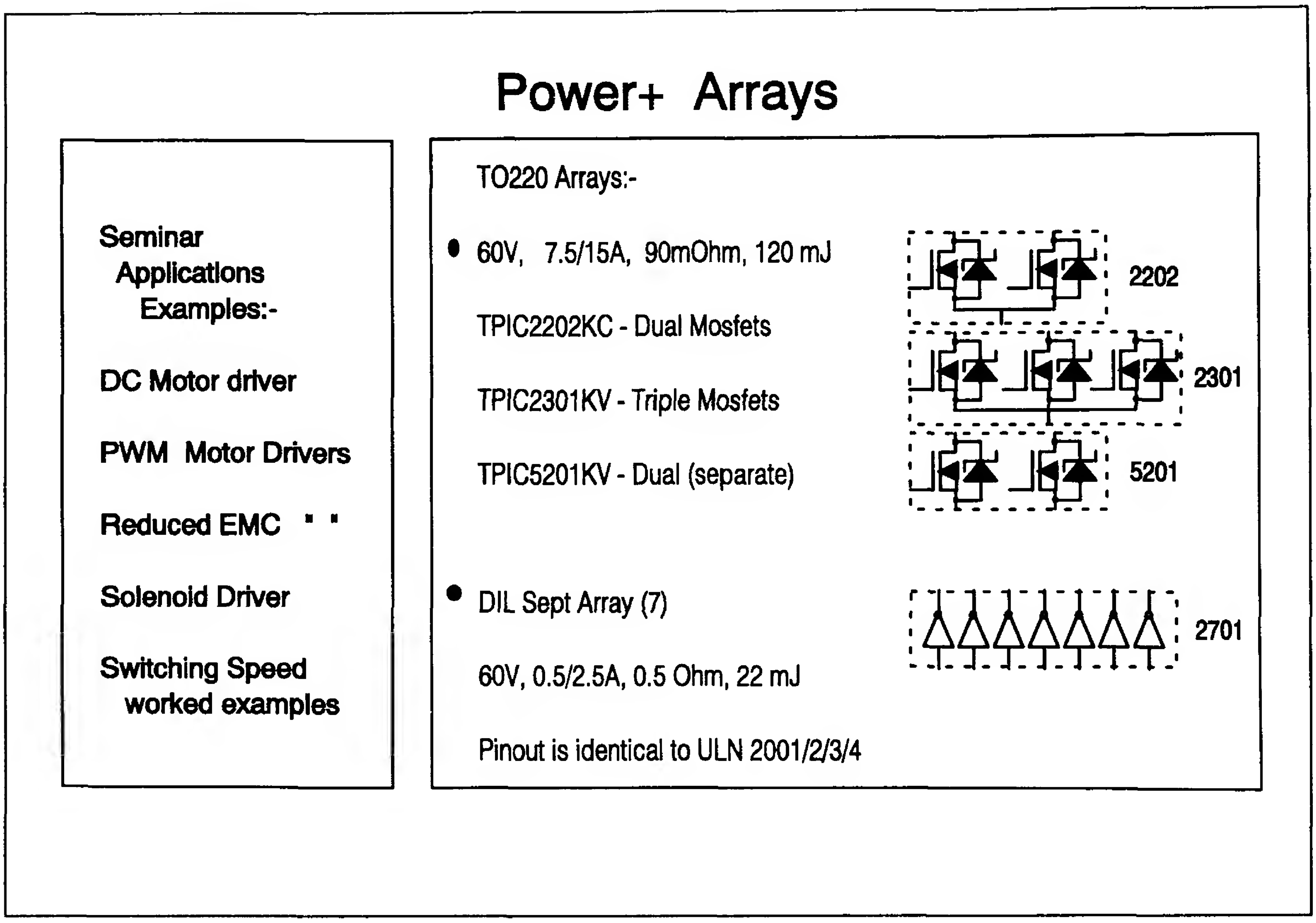
TPIC 6595 & 6A595
8-bit Shift Register



Featured in Serial Stepper Motor Driver Application, Ideal for Video Speed Arrays (14 MHz), and everywhere a logic device is paired with power O/P.

Figure 5.8.2 - Summary of Power+ Logic

The three parts of the Power+ product family were introduced: the Arrays of MOSFETs, the Logic devices with two levels of power output (TPIC6 and TPIC6A), and the Intelligent devices that sense and report on their own output state(s). The families' characteristics and specifications were examined in an application context, and the benefits of having a data sheet with properly-specified gate charge and avalanche energy were covered. Applications briefs were referenced for further reading, and medium term future trends discussed.



Power+ Arrays

Seminar
Applications
Examples:-

DC Motor driver

PWM Motor Drivers

Reduced EMC " "

Solenoid Driver

Switching Speed
worked examples

TO220 Arrays:-

- 60V, 7.5/15A, 90mOhm, 120 mJ

TPIC2202KC - Dual Mosfets

TPIC2301KV - Triple Mosfets

TPIC5201KV - Dual (separate)

- DIL Sept Array (7)

60V, 0.5/2.5A, 0.5 Ohm, 22 mJ

Pinout is identical to ULN 2001/2/3/4

2202
2301
5201
2701

Figure 5.8.3 - Summary of Power+ Arrays

NOTES

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